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Effects of thin oxide in metal–semiconductor and metal–insulator–semiconductor epi-GaAs Schottky diodes

Mantu Kumar Hudait [a,b], S.B. Krupanidhi [a,*]

[a] *Materials Research Centre, Indian Institute of Science, Bangalore 560 012, India*
[b] *Central Research Laboratory, Bharat Electronics, Bangalore 560 013, India*

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Abstract

The current–voltage (I–V) and capacitance–voltage (C–V) characteristics of metal–insulator–semiconductor (MIS) GaAs Schottky diodes are investigated and compared with metal–semiconductor (MS) diodes. The MIS diode showed nonideal behavior of I–V characteristics with an ideality factor of 1.17 and a barrier height of 0.97 eV. The energy distribution of interface states density was determined from the forward bias I–V characteristics by taking into account the bias dependence of the effective barrier height, though it is small. The reduction in the saturation current in the MIS case is caused by a thin oxide layer and is due to the combination of increased barrier height and a decrease in the Richardson constant. The carrier concentration anomaly observed between the MIS and MS diodes measured from reverse bias C–V measurements is explained via oxide (β-Ga_2O_3) traps due to the Ga-vacancy by deep level transient spectroscopy (DLTS) measurement.

1. Introduction

The electrical transport across Schottky diodes on epi-GaAs surface has been of considerable interest in the recent years for the widespread applications in microwave field effect transistors (FETs), radio frequency (RF) detectors and solar cells. In general, being a Schottky contact configuration, its performance and reliability is drastically determined by the interface quality between the deposited metal and the semiconductor surface. It is well known that, unless specially fabricated, a Schottky barrier diode (SBD) possesses a thin, interfacial, native oxide layer between the metal and the semiconductor. The existence of such an insulating layer converts the metal–semiconductor (MS) devices into metal–insulator–semiconductor (MIS) diodes [1–9] and can have a strong influence on the diode characteristics as well as the interface states [1–7]. The barrier height of MIS diode is greater than that of Au–GaAs MS Schottky barrier [10–15]. The performance and reliability of Schottky microwave devices depend on the interface states density and distribution. The effect of the presence of an interfacial layer and interface states on the current–voltage (I–V) and capacitance–voltage (C–V) characteristics of Schottky diodes have been studied by several authors [1–7,9–12,16–22].

Ashok et al. [10] studied the Au-GaAs MIS Schottky barrier diodes and found that there is a reduction in reverse saturation current caused by the interfacial layer and an increase in barrier height and a considerable decrease in the value of the effective Richardson constant, A^{**} compared to that of the MS diode. The reduced effective Richardson constant of the MIS diode relative to that of the MS device is directly attributable to the attenuation of I_S due to tunneling through the interfacial layer or electron transport by hopping via oxide traps [10]. The native oxide on GaAs is presumably conductive due to a high trap density, while retaining charge [16]. It is considered more probable that the attenuation caused by the interfacial layer in GaAs MIS Schottky barriers is due to recombination through traps in oxide rather than tunneling. A number of

* Corresponding author. Tel.: +91-80-3311330; fax: +91-80-3341683.

E-mail addresses: mantu@mrc.iisc.ernet.in (M.K. Hudait), sbk@mrc.iisc.ernet.in (S.B. Krupanidhi).

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theories have been put forward to explain the decrease in saturation current and the corresponding increase in photo-voltage of MIS solar cells. These theories [23,24] invoke a number of factors governing barrier height modification and transport control including surface states, fixed charges, traps, tunneling or hopping conduction through the insulator and asymmetrical tunneling probabilities for majority and minority carriers. Even the reduction in carrier concentration was observed between the MS and MIS GaAs Schottky diodes, although the same epitaxial GaAs film was used for the fabrication of MS and MIS diode [10]. The reduction in carrier concentration is explained by traps in the depletion layer, effective contact area variation, interfacial layer, and charge in surface states. However, there is no direct proof of traps inside the depletion layer, which can reduce the carrier concentration.

The homomorphic dielectrics on III–V semiconductors, such as GaAs and InP, suffer from several disadvantages [25]. The native oxide, which is present on the surface of the semiconductor prior to dielectric deposition, can act as a source of traps [26]. The presence of interface states can give rise to trapping, scattering and nonradiative recombination, all of which are deleterious to device performance. Fig. 1 shows, schematically, the presence of surface and interface states, which can trap charge carriers in a MIS device [27]. The well-known deep level transient spectroscopy (DLTS) technique [28] is a useful technique for determining [29–31] surface or interface states in MIS structures.

This work is an attempt to investigate the detailed electrical transport properties of GaAs Schottky diodes with and without an interfacial oxide layer using forward bias I–V characteristics and reverse bias C–V measurements. Finally, the interface states of density was evaluated for the GaAs MIS and MS structures. The DLTS technique was used to determine the trap carrier concentration and activation energy of trap in the GaAs MIS Schottky diodes. Here, we show some evidence of traps due to the oxide layer, which in turn reduces the carrier concentration, although the same epitaxial wafer was used for MS and MIS structural fabrication. The carrier concentration anomaly in both GaAs MS and MIS Schottky diodes is explained via oxide (β-Ga_2O_3) trap due to the gallium vacancy inside the film.

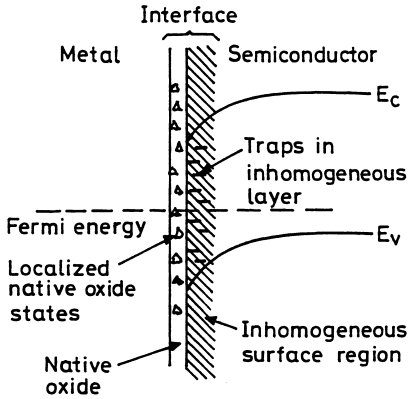

Fig. 1. Schematic band diagram illustrating the potential sources of surface and interfacial trapping to be expected in an MIS GaAs device (qualitatively followed to that suggested in Ref. [27]).

2. Experimental procedure

The Au/n-GaAs Schottky diodes were fabricated on $HCl:H_2O_2$ etched undoped GaAs epitaxial film ($N_D \cong 2.5 \times 10^{15}$ cm^{-3}) and without $HCl:H_2O_2$ etched GaAs epitaxial films, grown by low-pressure metal-organic vapor-phase epitaxy (LP-MOVPE) on n^+-GaAs substrates (1 0 0) 2° off-oriented towards the [1 1 0] direction. The thickness of the grown GaAs undoped epitaxial film was 3.0 μm. The details of the growth procedure can be found elsewhere [32–35]. The back ohmic contact was made using Au:Ge and an overlayer of Au and annealed at 450°C for about 2 min in an ultra-high pure (UHP) N_2 flow. The epi-GaAs wafer was cut into two pieces. The two pieces were cleaned using the organic solvents, and one of them (hereafter called $D2$) was kept in a laminar flow station for one day to obtain an oxide layer of the order of ~30 Å [8,14], and to observe the contribution of the interfacial layer thickness together with the semiconductor bulk thickness (the neutral region of the Schottky diode) to the series resistance. Next day, the piece of epi wafer, which was not kept inside the laminar flow station (hereafter called $D1$), was etched by using $HCl:H_2O_2$ (rinsed with DI water) and both the pieces were inserted into the evaporation chamber to form Schottky contacts. It is well known that a layer-by-layer growth of the native oxide layer, which is inevitably present on the chemically prepared semiconductor surface, occurs when it is exposed to clean room air [1–3,6,7,9]. The Schottky contacts were formed by evaporating Au as dots with a diameter of about 400 μm onto mirror smooth surfaces of these pieces. Thus, the samples $D1$ and $D2$ were obtained without and with an interfacial layer, respectively. All evaporation processes were carried out in a vacuum-coating unit at a pressure of about $2–3 \times 10^{-6}$ mbar. The dark I–V and C–V measurements of the samples were performed at 300 K. The DLTS measurement of the samples were performed using a computer controlled commercial system made by Lab-Equip, India in the temperature range of 77–397 K.

3. Methods of analysis

When a MS contact with an interfacial layer is considered, it is assumed that the forward bias current in a Schottky barrier is due to thermionic emission current corrected by tunneling and is expressed [7] as

$$I = aA^{**}T^2 \exp(-\chi^{0.5}\delta) \exp\left(-\frac{q\Phi_{b0}}{kT}\right) \exp\left(\frac{qV}{nkT}\right), \tag{1}$$

where A^{**} is the Richardson constant (8×10^4 $Am^{-2}K^{-2}$ for GaAs), a, the diode area, Φ_{b0}, the zero bias barrier height and χ, the mean barrier height presented by the thin interfacial layer. The term $\exp(-\chi^{0.5}\delta)$ is commonly known as the transmission coefficient across the thin interfacial layer. Eq. (1) is valid only for forward biases $V > 3kT/q$ as the reverse current contribution (due to metal electrons tunneling into the semiconductor) has been neglected.

The voltage dependence of the effective barrier height, Φ_e is contained in the ideality factor, n through the relation [17]

$$\frac{d\Phi_e}{dV} = \beta = 1 - \frac{1}{n}, \tag{2}$$

where β is the voltage coefficient of Φ_e. The effective barrier height is given by [17]

$$\Phi_e = \Phi_{b0} + \beta V. \tag{3}$$

For an MIS diode having interface states in equilibrium with the semiconductor, the ideality factor, n becomes greater than unity as proposed by Card and Rhoderick [7] and is given by

$$n = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{W} + qN_{ss}\right) \tag{4}$$

where W is the space charge width, N_{ss} is the density of the interface states; ε_s and ε_i are the permittivities of the semiconductor and the interfacial layer, respectively.

In an n-type semiconductor, the energy of the interface states, E_{ss} with respect to the bottom of the conduction band at the surface of the semiconductor is given by [5,9,17,36–38]

$$E_c - E_{ss} = q(\Phi_e - V). \tag{5}$$

Eqs. (2)–(5), along with the I–V characteristics can be used for the determination of interface states density as a function of interface states energy E_{ss} with respect to the bottom of the conduction band.

4. Results and discussion

4.1. Current–voltage (I–V) characteristics

Fig. 2 shows the experimental forward bias I–V characteristics of the sample $D1$ and the sample $D2$ diodes with the interfacial layer. The values 1.16, 0.912 and 1.17, 0.970 eV for the ideality factor, n and zero bias barrier height, Φ_{b0} of diodes MS and MIS, respectively, were obtained from the linear regions of the forward bias I–V plots indicating that the effect of series resistance in linear regions is not significant. At room temperature and above, where pure thermionic emission dominates, both the MIS and MS diodes exhibit constant and nearly equal values of n [10]. The value of ideality factor 1.17 for sample $D2$ shows that the device obeys an MIS configuration rather than the ideal Schottky diode. As we had etched the film ($D1$) before making Schottky contact, it will be considered as having a nonoxidized film of thickness of about 5 Å [9] at the MS interface and 30 Å [8,14] for the oxidized ($D2$) film, respectively, for the calculation of interface states energy density distribution. It has been reported [2,6,7,9,14] that an effective interfacial layer of nonzero thickness must exist between the metal and semiconductor even when both are in intimate atomic contact. Films of

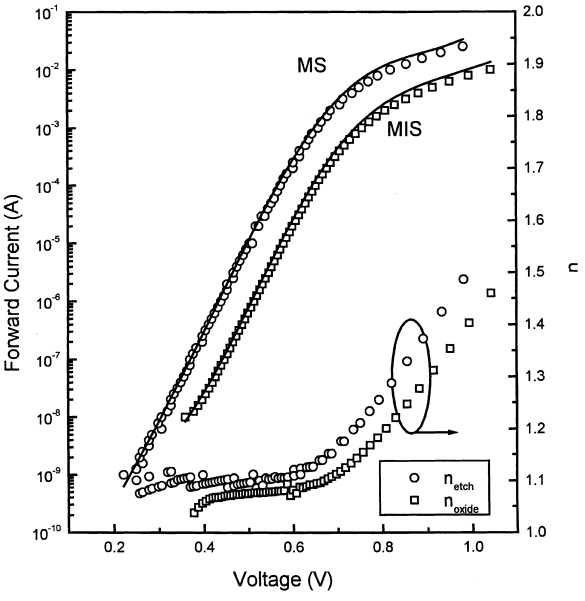

Fig. 2. The current and ideality factor vs. voltage characteristics of the Au/n-GaAs MS and MIS diodes at 300 K. The solid line represents the best fit of the experimental values of I to Eqs. (7) and (8) with the reverse saturation current $I_0 = 2\times10^{-13}$ and 1×10^{-14} A for the MS and MIS diodes, respectively. The voltage dependence of the ideality factor of both the diodes are also shown.

thickness of 10–25 Å usually lead to values of the ideality factor in the range 1.18–1.30 [2,7,9]. Again, the higher value of barrier height of diode $D2$ compared with the barrier height of diode $D1$ obtained from the forward bias linear region of I–V characteristics indicates that diode $D2$ obeys the MIS configuration [10].

At high currents, there is always a deviation which has been clearly shown to depend on the interface states density and bulk series resistance, as one would expect. The lower the interface states density and the series resistance, the greater the range over which I–V curve does in fact yield a straight line [17]. As the linear part of the forward I–V plots is reduced, the accuracy of the determination of Φ_{b0} and n becomes lower. The ideality factor and the series resistance were evaluated using a method developed by Cheung [39] in the higher current range (over which the I–V characteristics is not linear). The ideality factor and the series resistance were found to be 1.81 and 7.3 Ω for diode $D1$ and 1.925 and 18.32 Ω for diode $D2$, respectively, by using the formula

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right). \tag{6}$$

Thus, it is clearly seen that the value of 1.925 for n from the downward curvature region which results from the series resistance and interface effects is greater than the value of 1.17 obtained from the linear region of the I–V characteristics.

The downward curvature in the I–V characteristics at high forward bias values is attributed to a continuum of surface states. In this region, the ideality factor is controlled by the interface states. Therefore, the I–V data of diodes $D1$ and $D2$ shown in Fig. 2 fits well to the equations:

$$D1 \quad I = 2 \times 10^{-13} \exp\left(\frac{qV}{nkT}\right), \tag{7}$$

$$D2 \quad I = 1 \times 10^{-14} \exp\left(\frac{qV}{nkT}\right), \tag{8}$$

with the n values given in Table 1, where 2×10^{-13} and 1×10^{-14} A are the saturation currents of diodes $D1$ and $D2$, respectively. The reduction in saturation current in the MIS device compared to MS device caused by the interfacial layer is due to a combination of an increase in barrier height (0.97 eV vs. 0.912 eV) and a considerable decrease in the value of A^{**}. A number of theories [23,24] have been proposed for explaining the reduction of saturation current by considering the factors governing barrier height modification and transport controlled including surface states, fixed charges, traps, tunneling or hopping conduction through the insulator and asymmetrical tunneling probabilities for majority and minority carrier. The native oxide on GaAs (β-Ga_2O_3) is presumably conductive due to a high trap density [16] and the reduction of A^{**} may be due to electron transport by hopping via oxide trap [10].

Table 1
Typical parameters of GaAs MIS and MS diodes

Parameter	MIS	MS
Oxide thickness, δ (Å)	30	5
Ideality factor, n	1.17	1.16
Saturation current, I_s (A) from forward bias I–V characteristics	1×10^{-14}	2×10^{-13}
Reverse saturation current (A) from reverse bias I–V characteristics	1×10^{-10}	1×10^{-8}
Barrier height, Φ_{b0}^{I-V} from I–V characteristics	0.97	0.912
Barrier height, Φ_{b0}^{C-V} from C–V characteristics	1.125	0.961
Zero-bias capacitance (pF)	13.67	20.72
Diode contact area (cm^2)	1.25×10^{-3}	1.25×10^{-3}
Depletion layer width (μm)	1.04	0.68
Slope of C^{-2} vs. V plot ($F^{-2}\,V^{-1}$)	5.641×10^{21}	2.783×10^{21}
Apparent doping concentration (cm^{-3})	1.25×10^{15}	2.50×10^{15}
C^{-2} vs. voltage intercept, V_0 (V)	0.946	0.80
Trap density, N_T (cm^{-3}) from the DLTS experiment	1×10^{14}	2.97×10^{13}
Activation energy, E_T (eV)	0.70	–

Fig. 3 shows the reverse bias I-V characteristics of the MIS and MS Schottky diodes. The curves of the two devices are roughly parallel and the attenuation in current caused by the interfacial layer. Hence, the reverse current of the MIS diode is still contact limited, rather than oxide-bulk limited [10]. The extrapolated reverse current of the MIS and MS diodes is higher than the forward bias saturation current of each device.

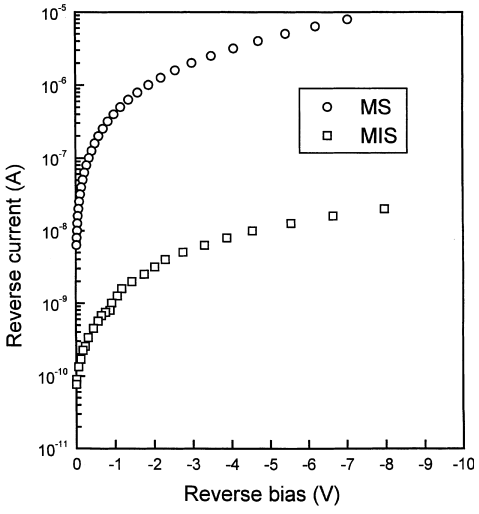

Fig. 3. The reverse I–V characteristics of the MIS and MS diodes.

4.2. Capacitance–voltage (C–V) characteristics

The reverse bias capacitance measurements are made at a very high frequency (1 MHz), so that the interface states are unable to respond to the AC signal. The C–V characteristics of the MS and MIS diodes at 1 MHz frequency are shown in Fig. 4. The zero bias capacitance is seen to drop from 20.72 to 13.67 pF, due to the interfacial layer. As the reverse voltage is increased, the difference in capacitance between the two devices decreases, and it is appreciable even at the highest applied voltage. In order to assess the doping concentration and barrier height, C^{-2} vs. V_R, plots (Fig. 5) were obtained from the C–V data of Fig. 4. The C–V relationship applicable to intimate MS Schottky barriers on uniformly doped materials, can be written as [2]:

$$\frac{1}{C^2} = \frac{2(V_R + V_0)}{q\varepsilon_s N_D a^2}, \tag{9}$$

where V_R is the reverse bias voltage, V_0, the built-in voltage, q, the electronic charge, and N_D, the doping concentration. The diffusion potential or built-in potential is usually measured by extrapolating C^{-2}–V plot to the V-axis. An insulating film can modify these characteristics if the potential across the film changes with bias. The zero bias barrier height from C–V measurement is defined by

$$\Phi_{b0} = V_0 + \frac{kT}{q} + \Phi_n, \tag{10}$$

where Φ_n is the Fermi energy measured from the conduction band edge.

For the MS Schottky barrier, the doping concentration and the zero bias barrier were 2.50×10^{15} cm^{-3} and

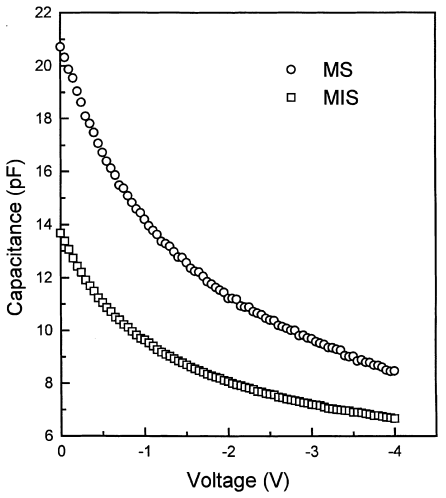

Fig. 4. 1 MHz capacitance–voltage characteristics of the MIS and MS diodes.

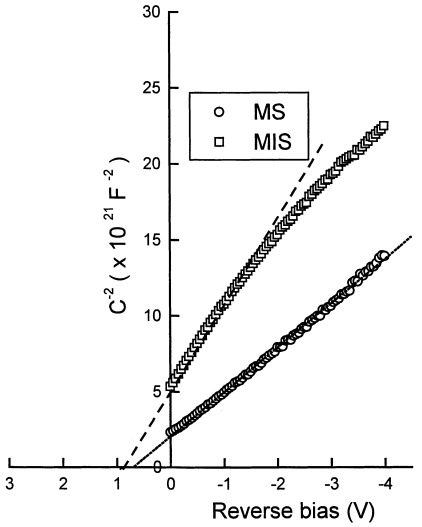

Fig. 5. C^{-2} against the voltage for the MIS and MS diodes (shows a straight deviation at higher voltages).

0.961 eV, respectively. The zero bias barrier height obtained from I–V characteristics is less compared to that from C–V measurement, as expected. As shown in Fig. 5, the MS diode exhibits a perfectly linear C^{-2} vs. V_R plot up to 3 V, with a deviation from linearity at higher voltages. The linearity of C^{-2}–V plot at this frequency indicates that the interface states, and the inversion layer charge cannot follow the AC signal at this high frequency and consequently do not contribute appreciably to the diode capacitance. For an MIS device (thick or thin oxide), the functional form of Eq. (9) still holds as long as the device is operated in depletion or deep-depletion mode. However, in this case, V_0 includes additional terms involving flat-band voltage and oxide capacitance, while the slope of C^{-2} vs. V_R plot should be the same as that given by Eq. (9) [40]. The C^{-2} vs. V_R plot of the MIS diode also shows linearity up to 1 V reverse bias, with only a straight deviation at higher voltages. From the slope of the C^{-2} vs. V_R plot of the MIS diode, the doping concentration of 1.25×10^{15} cm^{-3} and the zero bias barrier height of 1.125 eV were obtained. A 50% reduction of the carrier concentration of the MIS diode from the MS diode was obtained. Such a discrepancy cannot be attributed to carrier concentration variations as both the MS and MIS diodes were made on GaAs cut from the same wafer. The carrier concentration of the epi GaAs wafer was also measured by using electrochemical capacitance voltage (ECV) profiler and the carrier concentration variation was less than $\pm 5\%$. It is interesting to note that we did not observe any frequency dispersion in the frequency range from 1 KHz to 1 MHz in either MS or MIS diode. Ashok et al. [10] found a similar discrepancy of carrier

concentration in both the GaAs MS and MIS diodes, and they also did not observe the frequency dispersion in the frequency range from 10 Hz to 1 MHz. But the frequency dispersion was obtained by Hirose et al. [41] in GaAs MIS Schottky diodes with an Al_2O_3 interfacial. In this case, the frequency dependence has been shown to be due to the GaAs–Al_2O_3 interface and not due to the Al_2O_3 film.

The deviation of the C–V data from that expected for the ideal Schottky barrier on uniformly doped semiconductor can be attributed to a number of factors including traps in depletion layer, effective contact area variation, interfacial layer and charge in surface states [7,42]. However, most of the theories cannot explain the apparent decrease in doping concentration as seen from the C^{-2} vs. V_R plot of the MIS diode. One possible theory [7] that accounts for the apparent low doping obtained for the MIS diode invokes interface states in equilibrium with the semiconductor. Another possible explanation for the decrease in electron concentration could be traps associated with the oxide. This can be confirmed after considering the DLTS experiment. The salient parameters of the MIS diode and the reference MS diode are listed in Table 1.

4.3. Determination of interface states density (N_{ss})

Substituting the values of the voltage dependence of n from Table 2 in Eq. (4), using $\varepsilon_s = 12.8\varepsilon_0$ [2], $\varepsilon_i = 3.5\varepsilon_0$ [10], $\delta = 30$ Å [8,14], and $W = 1.04$ μm (from C–V measurements) for the MIS diode and $\delta = 5$ Å [9], $W = 0.68$ μm from C–V measurements (Fig. 4) for MS diode, the values of N_{ss} as a function of V were obtained and is given in Table 2. The resulting dependence of N_{ss} was converted to a function of E_{ss} using Eq. (5). N_{ss} vs. $E_c - E_{ss}$ is also shown in Table 2 and Fig. 6. In the forward bias case, the increase in the effective barrier height, Φ_e of both the diodes with bias can be understood as follows: when the diode is forward biased, the quasi-Fermi level (imref) for the majority carriers rises on the semiconductor side. Thus, most of the electrons will be injected directly into the metal forming a thermionic emission current, while some of them are trapped by the interface states. This charge capture process results in an increase in the effective barrier height, thereby reducing the diode current [2,17,43].

From Fig. 6, it can be seen that an exponential increase in the interface states' density exists from midgap towards the bottom of the conduction band. This rise is less significant for the MIS diode compared to that of the MS diode. At any specific energy, the interface states' density of MIS diode is less compared to that of the MS diode. This case can be ascribed to the fact that MIS diode has a thicker oxide layer than that of the MS diode [2,3,5,17], because of which the dangling bonds on the GaAs surface saturate. The shape of the density

Table 2
Interface states energy distribution obtained from the forward bias I–V characteristics at 300 K, Φ_{b0} (C–V) = 0.961 eV for MS and Φ_{b0} (C–V) = 1.125 eV for MIS diodes

Voltage (V)	n	Φ_e (eV)	$E_c - E_{ss}$ (eV)	$N_{ss} \times 10^{16}$ ($eV^{-1}m^{-2}$)
MIS				
0.38	1.038	1.139	0.762	0.176
0.40	1.056	1.146	0.750	0.290
0.42	1.066	1.151	0.732	0.358
0.44	1.068	1.153	0.714	0.373
0.46	1.070	1.155	0.696	0.387
0.48	1.072	1.157	0.680	0.400
0.50	1.074	1.16	0.660	0.411
0.52	1.076	1.161	0.643	0.43
0.54	1.077	1.164	0.625	0.432
0.56	1.08	1.166	0.607	0.441
0.58	1.08	1.168	0.589	0.45
0.60	1.081	1.170	0.571	0.457
0.62	1.086	1.174	0.553	0.487
0.64	1.092	1.179	0.543	0.527
0.66	1.096	1.182	0.523	0.55
0.68	1.103	1.188	0.5116	0.600
0.70	1.112	1.196	0.500	0.658
0.72	1.125	1.205	0.488	0.740
0.74	1.143	1.218	0.476	0.856
0.76	1.154	1.226	0.470	0.925
0.79	1.183	1.247	0.458	1.110
0.83	1.221	1.275	0.446	1.36
0.88	1.277	1.316	0.434	1.716
0.95	1.353	1.373	0.422	2.21
1.04	1.46	1.453	0.410	2.90
MS				
0.26	1.075	0.979	0.723	2.80
0.28	1.082	0.982	0.705	3.07
0.30	1.088	0.985	0.687	3.308
0.32	1.116	0.994	0.675	4.40
0.34	1.1015	0.9924	0.6514	3.82
0.36	1.1056	0.995	0.6335	3.97
0.38	1.0904	0.993	0.6097	3.39
0.40	1.0945	0.996	0.592	3.55
0.42	1.097	0.998	0.58	3.65
0.44	1.10	1.001	0.562	3.786
0.46	1.1048	1.005	0.54	3.95
0.48	1.094	1.0024	0.5204	3.534
0.50	1.0972	1.0055	0.5025	3.657
0.52	1.0853	1.0016	0.485	3.20
0.54	1.105	1.012	0.474	3.96
0.56	1.107	1.052	0.4562	4.05
0.58	1.1053	1.0162	0.4362	3.968
0.60	1.1095	1.0203	0.420	4.133
0.63	1.126	1.031	0.4013	4.763
0.66	1.14	1.0414	0.383	5.287
0.68	1.1518	1.050	0.371	5.768
0.70	1.175	1.066	0.360	6.695
0.75	1.211	1.0917	0.3417	8.069
0.80	1.255	1.122	0.33	9.76
0.90	1.373	1.203	0.312	14.32
1.00	1.486	1.282	0.300	18.694

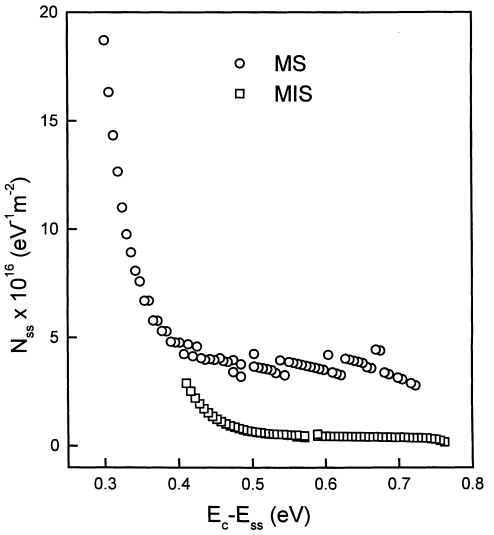

Fig. 6. Density of interface states as a function of E_c-E_{ss} of the Au/n-GaAs MIS and MS diodes.

distribution of the interface states in the range from $E_c-0.30$ to $E_c-0.70$ eV, especially for the MS diode is in close agreement with those obtained by a method based on AC-admittance measurement [44] and by Schottky capacitance spectroscopy [45] for Au/n-GaAs Schottky barrier diodes.

4.4. Deep level transient spectroscopy study of GaAs MS and MIS diodes

In the C–V measurement, we find that there is a discrepancy in the carrier concentration determined from the MS and MIS diodes. This reduction could be due to the traps associated with the oxide. DLTS measurements were used to find out the trap carrier concentration and the activation energy of the trap in MS (if any present) and MIS diode, which could reduce the carrier concentration in the MIS diode.

The concentration of the trap (N_T) can be obtained from the capacitance range corresponding to completely filling the trap with a large enough pulse. The relationship for an electron trap in a Schottky barrier diode is given by [28]

$$N_T = 2N_D \frac{\Delta C}{C}, \tag{11}$$

where N_T is the trap concentration, ΔC, the capacitance change due to a saturating injection pulse, C, the capacitance of the diode under quiescent reverse-biased condition and N_D, the donor concentration on the n-GaAs film, where the trap is observed.

The thermal activation energy, E_T of electron trap was determined from the thermal emission rate, e_n for electron from the deep level into the conduction band [28]

$$e_n = \sigma_n v_{th} N_c \exp\left(-\frac{E_T}{kT}\right), \tag{12}$$

where σ_n is the capture cross-section of the deep level for electrons, v_{th} is the thermal velocity of electron in the conduction band, N_c is the effective density of states of the conduction band. Plotting $\ln(e_n/T^2)$ vs. $1000/T$, the activation energy and capture cross-section of the deep level can be obtained.

A typical DLTS spectrum from 77 to 397 K shows only one peak from the Au/n-GaAs MIS diode for different rate windows and is shown in Fig. 7. The Arrhenius plot, $\ln(e_n/T^2)$ vs. $1000/T$ is shown in Fig. 8, which gives an activation energy of 0.700 ± 0.038 eV. This deep level is known as the ML2, and it has rarely been observed in as-grown GaAs grown by any technique, except molecular beam epitaxy (MBE). Until recently, it was thought that EL2 was the only midgap trap. The ML2 (0.71 eV) defect has been proposed to be a double gallium vacancy, [V_{Ga}] [46–48], and an increase in V/III ratio during MOVPE process increased the 0.71 eV defect concentration by increasing [V_{Ga}]. The capture cross-section of the ML2 level was determined from the y-intercept of the Arrhenius plot of $\ln(e_n/T^2)$ vs. $1000/T$ and is 2.33×10^{-15} cm^2. There is very little information on the energy structure of the native oxide on GaAs. The oxide layer β-Ga_2O_3 [49] on epi-GaAs surface was formed during the time when we kept the wafer in the clean air environment inside the laminar flow station. The [V_{Ga}] vacancy was formed during the formation of β-Ga_2O_3 oxide layer on epi-GaAs film, and the oxide layer creates a deep majority carrier trap center. The trap carrier concentration, N_T from the MIS

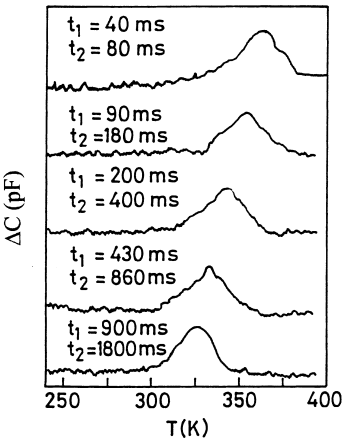

Fig. 7. DLTS spectra for electron traps in the Au/n-GaAs MIS diode for several sampling times. t_1 and t_2 represent the sampling times.

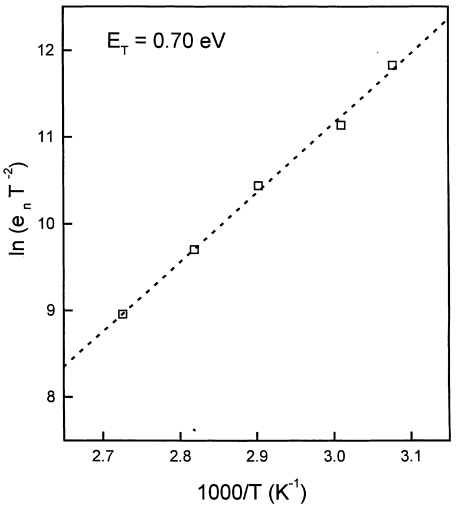

Fig. 8. Arrhenius plot for deep level state observed in the Au/n-GaAs MIS diode. The activation energy of this deep level peak is 0.70 ± 0.038 eV.

diode ($D2$) is $\sim 1 \times 10^{14}$ cm^{-3}. The decrease in carrier concentration in MIS diode as compared to MS diode is because the oxide layer creates Ga vacancies and hence reduces the carrier concentration.

It may also be seen from Table 1 that the trap carrier concentrations obtained from DLTS on MIS and MS structure, are 2.97×10^{13} and 1×10^{14} cm^{-3}, respectively. In the case of the MIS structure, trap carrier activation energy of 0.70 eV was estimated. However, such an estimation for MS diodes was not possible, as there was no appreciable shift in the DLTS peak.

5. Conclusions

The MIS Schottky diodes were fabricated on epitaxial (1 0 0) n-GaAs at a donor concentration of 2.5×10^{15} cm^{-3}, with a thin 30 Å oxide layer. The MS GaAs Schottky diodes were made on etched epitaxial n-GaAs films for the reference sample. The current conduction mechanism across both the MS and MIS diodes was determined by using I–V, C–V and DLTS measurement techniques. The forward bias I–V characteristics of MIS and MS diode indicate classical thermionic emission. The nonideal forward bias I–V behavior observed in the Au/n-GaAs Schottky diodes were attributed to a change in the MS barrier height due to the interface states and the interfacial layer. The bias dependent barrier height, though small, is considered for determination of interface states density distribution from the forward bias $\ln(I)$–V characteristics. The reduction in the saturation current in the MIS case is caused by the thin oxide layer and is due to a combination of increased barrier height and reduced velocity of charge carriers. The barrier height increase is ascribed to a negative charge at the interface, while recombination in the oxide is presumed to be the cause of the latter. Unlike the MS diode, an excess current is seen at low forward voltages, and this arises from recombination in the space charge layer. The carrier concentration anomaly observed between the MIS and MS diodes measured from the reverse bias C–V measurement was discussed via oxide (β-Ga_2O_3) traps due to the Ga vacancy by DLTS measurements.

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