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Electrical transport characteristics of Au/n-GaAs Schottky diodes on n-Ge at low temperatures

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Abstract

The current–voltage characteristics of Au/n-GaAs Schottky diodes grown by metal-organic vapor-phase epitaxy on Ge substrates were determined in the temperature range 80–300 K. The zero-bias barrier height for current transport decreases and the ideality factor increases at low temperatures. The ideality factor was found to show the T_0 effect and a higher characteristic energy. The excellent matching between the homogeneous barrier height and the effective barrier height was observed and infer good quality of the GaAs film. No generation–recombination current due to deep levels arising during the GaAs/Ge heteroepitaxy was observed in this study. The value of the Richardson constant was found to be 7.04 A K^{-2} cm^{-2}, which is close to the value used for the determination of the zero-bias barrier height. © 2001 Elsevier Science Ltd. All rights reserved.

Keywords: GaAS; Schottky diodes; MOVPE; Ge

1. Introduction

The electrical transport through Schottky diodes on epi-GaAs grown on Ge substrates has been of considerable interest due to potential widespread applications in microwave field effect transistors, radio-frequency detectors, phototransistors, heterojunction bipolar transistors, quantum confinement devices, and space solar cells. The performance and reliability of a Schottky contact is drastically determined by the interface between the deposited metal and the semiconductor surface. When GaAs is grown as an epitaxial film on Ge either by metal-organic vapor-phase epitaxy (MOVPE) or by molecular beam epitaxy some problems may arise, such as antiphase domains (APDs) surrounded by antiphase boundaries (APBs), misfit dislocations in the grown film, and cross-diffusion across the GaAs/Ge heterointerface [1–3]. Unless the MOVPE growth parameters are precisely controlled, the above-mentioned problems may deteriorate the device performance.

It is known that the presence of a large density of dislocations in GaAs on Ge substrates poses a major problem. It is necessary to understand the electrical activity of these defects and to find ways to control them. The defects can act as generation–recombination centers. Precipitation or clustering of impurities around the defects may act like random metallic paths, or may generate local regions of electric fields, causing a large leakage current and premature breakdown of the device. Hudait and Krupanidhi [4] studied Au/n-GaAs Schottky diodes on n-Ge substrates at 300 K and found that the epi-grown films showed a high ideality factor and a soft breakdown voltage. They concluded that the high ideality factor was due to either tunneling or generation–recombination current and the low breakdown voltage was due to the dislocations present inside the GaAs film. Such a situation in turn produces electrically active defects which results in a higher ideality factor at lower biases. There has been no report on the electrical transport characteristics of Au/n-GaAs on n-Ge substrates at low temperatures.

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GaAs/Ge heterostructures are finding applications in space under conditions of low intensity and low illumination, such as the Mars pathfinder mission and Rosetta, where the solar cells experience a very low temperature [5]. In geo-stationary orbit satellite applications, the solar cells experience a temperature of about 93 K for a short time [6], when the satellite is coming out of the eclipse. Hence, it is of technological importance to study and understand the current transport mechanisms of GaAs/Ge heterostructures at low temperatures. It is believed to offer a better picture of the nature of the barrier formed at the metal–semiconductor interface, which in turn can give insight into the various aspects of the conduction mechanisms. Although the GaAs/Ge heterostructure is of great importance in GaAs device technology, details are currently not available regarding the current transport mechanisms and the other properties of Au/n-GaAs on n-Ge over a wide range of temperatures. Therefore, an attempt has been made to study the current transport characteristics of Au/n-GaAs Schottky diodes on Ge in the temperature range of 80–300 K.

2. Experimental procedure

Si-doped n-type GaAs film of 3 μm thickness was grown on a (1 0 0) n^+-Ge substrate off-cut 2° towards the [1 1 0] direction. The film was grown using low-pressure MOVPE. The source materials were trimethylgallium, 100% arsine (AsH_3), 104 ppm silane (SiH_4) as an n-type dopant, and palladium purified H_2 as the carrier gas. The details of the growth procedure can be found elsewhere [4,7–9]. After the growth of GaAs on the Ge substrate, ohmic contacts were deposited using a thermal evaporator on the back side using a Au–Ge eutectic alloy with an over layer of Au. The contacts were annealed at 450°C for 2 min in an ultra-high-pure N_2 atmosphere. Au contacts were made on the front side of the GaAs epitaxial film using physical a mask having dots of area 1.25×10^{-3} cm^2, again using the thermal evaporation technique. The epitaxial film was cleaned using organic solvents and the oxide layer was removed using $HCl:H_2O_2$ (1:1) prior to the deposition of the Au front contact.

The current–voltage (*I–V*) characteristics of the diodes were measured at room temperature using an automated arrangement [10] consisting of a Keithley source measuring unit SMU 236, an IBM PC486, and a probe station. Diodes showing similar *I–V* characteristics and high reverse break down values were selected and mounted on a TO-39 header using silver paste and a thin gold wire. The TO-39 headers were mounted on a LN_2 cryostat and, using the above-mentioned setup, the low temperature *I–V* characteristics from 80 to 303 K were measured, in steps of 10 K. The temperature was maintained within ±1 K during the data acquisition. Capacitance–voltage (*C–V*) measurements were performed at room temperature using a capacitance meter at a frequency of 1 MHz; the carrier concentration of the grown n-type epitaxial layer was determined to be 1.3×10^{17} cm^{-3}. This carrier concentration is further confirmed by means of electrochemical *C–V* measurement. The diode was further characterized using deep level transient spectroscopy (DLTS), supplied by M/s Lab-Equip, India, in order to determine the properties of any deep levels present in the grown epi-GaAs film.

3. Results and discussion

3.1. *I–V* characteristics

Fig. 1 shows the forward semi-log *I–V* characteristics of Au/n-GaAs Schottky diodes grown on n-Ge at different temperatures, ranging from 80 to 300 K. These plots clearly depict the linearity over three to four decades of current magnitude. The gradual shift of the *I–V* curve towards a higher voltage is observed with decrease in temperature, which is in agreement with the following equation [11] governing the current transport across a Schottky diode by the thermionic emission–diffusion theory and is given by

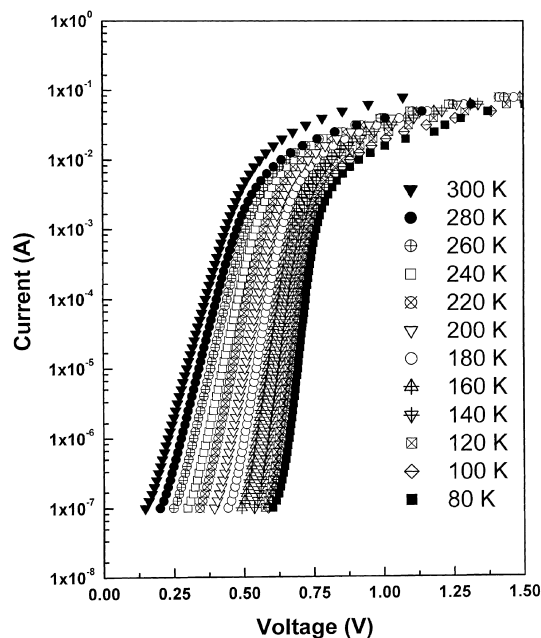

Fig. 1. The current versus voltage characteristics of the n-GaAs Schottky diode on the n-Ge substrate at various measurement temperatures.

$$I = I_s \exp\left(\frac{qV}{nkT}\right) \quad \text{for } V > 3kT/q \tag{1}$$

where V is the applied voltage drop across the semiconductor surface depletion layer. Further, n is the ideality factor, k is the Boltzmann constant, T is the temperature, q is the electronic charge and I_s is the saturation current, which is expressed by

$$I_s = aA^{**}T^2 \exp\left(-\frac{q\Phi_{b0}}{kT}\right) \tag{2}$$

where a is the diode area, A^{**} is the Richardson constant ($8.16\ \mathrm{A\,K^{-2}\,cm^{-2}}$), Φ_{b0} is the zero-bias barrier height.

Using Eq. (1), the values of the ideality factor n of the diode at different temperatures were calculated from the slopes of the linear regions of the semi-log forward bias curves. Using Eq. (2), the zero-bias barrier height, Φ_{b0} was determined from the extrapolated experimental saturation current, I_s. The zero-bias barrier height and the ideality factor at different temperatures are plotted versus temperature in Fig. 2. From Fig. 2, it is observed that the ideality factor increases with a decrease of temperature. This increase is very slow from 300 K down to 120 K and then increases steeply down to 80 K. The zero-bias barrier height decreases slowly with temperature down to 120 K and the further decrease is very steep down to 80 K. For an ideal Schottky diode, the zero-bias barrier height should increase as temperature is decreased, in accordance with the band gap variation with temperature [10,12,13]. Here, the zero-bias barrier height is showing an inverse behavior to the ideality factor variation.

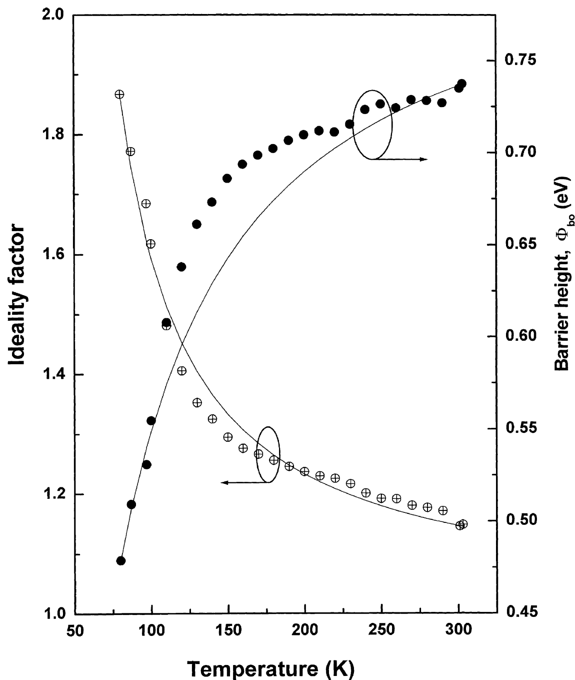

Fig. 2. The variation of the zero-bias barrier height and the ideality factor with temperature, calculated using Eqs. (1) and (2), for the Au/n-GaAs on n-Ge Schottky diode. The zero-bias barrier height decreases with decreasing temperature down to 120 K and the further decrease is very step down to 80 K.

To assess the quality of the grown GaAs film on Ge, several models of conduction mechanisms have been applied to the observed low temperature I–V data of Au/n-GaAs/Ge Schottky diodes. According to Werner–Gütler model [14], the barrier height has a Gaussian distribution with a mean barrier height. The decrease in barrier height with reduction in temperature has been explained by the lateral distribution of the barrier height [14]. The Gaussian distribution of the barrier height yields the following equation for the barrier height:

$$\Phi_{b0} = \Phi_{b\,\mathrm{mean}} - \frac{\sigma_s^2 q}{2kT} \tag{3}$$

where Φ_{bmean} is the mean barrier height, σ_s is the standard deviation of the barrier distribution, and the other symbols have their usual meanings. The zero-bias barrier height has been simulated using Eq. (3) and re-plotted along with the experimentally observed barrier heights in Fig. 2. The detailed experimental and simulated barrier height and ideality factor are shown in Table 1. From the experimental and simulated zero-bias barrier heights, one can find that there is a large deviation between these two values. The Werner–Gütler model has been used by several authors [10,15–18] to fit the theoretical and experimental zero-bias barrier heights and in general there has been very good agreement between these two values. However, the experimentally observed zero-bias barrier height does not closely match with the value predicted from Werner–Gütler model (Eq. (3)) and one can also find from Fig. 2 that there is a large deviation between the theoretical and experimental values from 120 to 260 K. Only in the high and low temperature regions does this model fit with the experimental data.

In order to explain the observed variation of ideality factor with temperature in the present case, Werner–Gütler's potential fluctuation model [14] has been considered. According to this model, the variation of ideality factor with the temperature is given by

$$\frac{1}{n} = 1 - \gamma + \frac{q\zeta\sigma_s}{kT} \tag{4}$$

where γ and ζ are the voltage coefficients of barrier height. Using the experimentally determined values of n at different measurement temperatures and the value of σ_s obtained from Eq. (3), values of γ and ζ were obtained. The experimentally determined values and the continuous curve representing a fit to these values using

Table 1
The experimental and simulated barrier height and the ideality factor at different temperatures[a]

T (K)	n_{expt}	$\Phi_{b0\,expt}$ (eV)	Werner and Güttler Equ.		Φ_b^f (eV)
			n_{simu}	$\Phi_{b0\,expt}$ (eV)	
80	1.867	0.480	1.867	0.479	0.885
87	1.773	0.509	1.746	0.507	0.893
97	1.684	0.531	1.623	0.540	0.885
100	1.617	0.555	1.594	0.549	0.889
110	1.480	0.608	1.513	0.575	0.893
120	1.405	0.638	1.452	0.596	0.890
130	1.352	0.661	1.404	0.614	0.887
140	1.325	0.673	1.365	0.629	0.886
150	1.295	0.686	1.333	0.642	0.882
160	1.276	0.694	1.307	0.654	0.879
170	1.266	0.699	1.284	0.664	0.878
180	1.256	0.702	1.264	0.674	0.876
190	1.46	0.707	1.247	0.682	0.874
200	1.237	0.709	1.233	0.689	0.871
210	1.230	0.712	1.220	0.696	0.869
220	1.225	0.711	1.208	0.702	0.865
230	1.216	0.715	1.197	0.708	0.863
240	1.200	0.723	1.188	0.713	0.861
250	1.191	0.726	1.179	0.717	0.859
260	1.190	0.724	1.171	0.722	0.855
270	1.180	0.729	1.164	0.726	0.853
280	1.176	0.728	1.158	0.730	0.850
290	1.170	0.727	1.152	0.733	0.844
301	1.145	0.735	1.146	0.736	0.836
303	1.148	0.737	1.144	0.737	0.804

[a] $\sigma_s = 69.6$ mV, $\Phi_{bmean} = 0.83$ eV, $\gamma = 0.0051$, $\zeta = -0.0455$.

the parameters obtained using Eq. (4) are shown in Fig. 2. From Fig. 2 it is observed that there is a deviation between the experimental and simulated ideality factors. Therefore, the small discrepancies between the experimental and theoretical values of the barrier height and ideality factor could be due to deviations in the barrier height distribution from the Gaussian model assumed by Werner–Gütler.

According to Tung's model [17,18], the ideality factor of an inhomogeneous Schottky barrier diode with a distribution of low Schottky barrier heights may increase when the measurement temperature is lowered. As per Sullivan et al. [19] and Tung's model of lateral inhomogeneities [17,18], the Schottky barrier consists of laterally inhomogeneous patches of different barrier heights. The patches with lower barrier height have larger ideality factors and vice versa. Using Tung's theoretical approach, Schmitsdroff et al. [20] found a correlation between the zero-bias barrier height and the ideality factors. The extrapolation of the linear fit to the data gives a homogeneous barrier height an ideality factor of about 1.01. In the present case, the homogeneous barrier height obtained from the linear fit of the zero-bias barrier height versus ideality factor is 0.78 eV and is shown in Fig. 3. This homogeneous barrier height

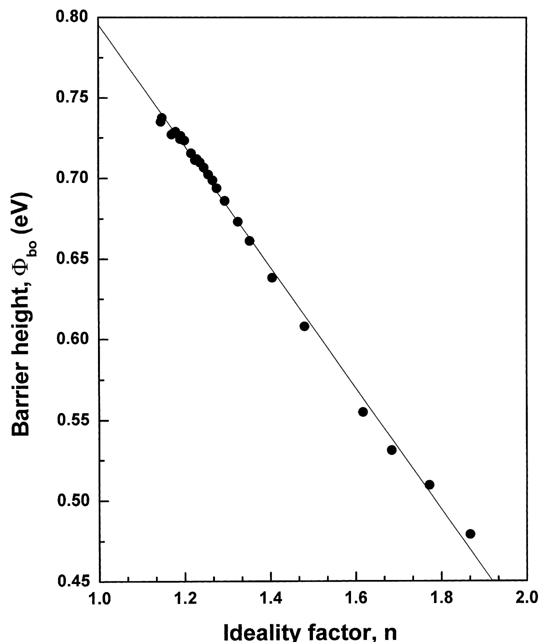

Fig. 3. The zero-bias barrier height versus ideality factor at different temperatures. The extrapolation of the linear fit yields a homogeneous barrier height value of 0.78 eV.

is in close agreement with the effective barrier height ($\Phi_{b0}^{cv} = 0.776$ eV) obtained from the C–V measurement. According to Schmitsdroff et al. [20], the larger the discrepancy between the homogeneous barrier height and the effective barrier height, the poorer the quality of the grown epilayer.

3.2. Effect of thermionic field emission

Mechanisms such as tunneling and generation–recombination are now considered to explain the observed variation of ideality factor and zero-bias barrier height. If the current transport is controlled by the thermionic field emission (TFE) theory, the relation between current and voltage can be expressed as [21]

$$I = I_s \exp\left(\frac{V}{E_0}\right) \tag{5a}$$

$$E_0 = E_{00} \coth\left(\frac{qE_{00}}{kT}\right) = \frac{nkT}{q} \tag{5b}$$

where E_{00} is the characteristic energy, which is related to the transmission probability of the carrier through the barrier given in the following equation:

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_D}{m_e^*\varepsilon_s}\right)^{1/2} = 18.5 \times 10^{-15}\left(\frac{N_D}{m_r\varepsilon_r}\right)^{1/2} \tag{6}$$

In the case of our Au/n-GaAs Schottky diode on Ge, with $N_D = 1.3 \times 10^{17}$ cm^{-3}, $m_e^* = 0.067m_0$, and $\varepsilon_s = 12.8\varepsilon_0$ the value of E_{00} turns out to be 7.2 meV. According to the transport theory, TFE dominates only when $E_{00} \approx kT$ and the value of E_{00} calculated using Eq. (6) is almost equal to the value of kT at 80 K. However, the barrier height lowering, $\Delta\Phi_{TFE}$, due to TFE can be determined using the following equation [21]:

$$\Delta\Phi_{TFE} = \left(\frac{3}{2}\right)^{2/3} (E_{00})^{2/3} (V_d)^{1/3} \tag{7}$$

where V_d is the built in potential. For a built in potential of 0.78 V and a value of E_{00} 7.2 meV, the calculated barrier height lowering is 45 meV. This cannot account for the presently observed lowering of the barrier height.

Using the experimental values, the increase in ideality factor is further analyzed by considering the tunneling current as the cause for the variation of the ideality factor. Fig. 4 shows a plot of E_0 versus kT/q. The value of E_0 is determined from Eq. (5b). A linear fit to the data results in a y-intercept, which gives a value of E_0 as 5.63 meV. This fit is good down to a temperature of 120 K and deviates below this temperature. The experimentally observed E_0 value of 5.63 meV is less than the theoretically calculated value of 7.2 meV. If the curvature is considered at 120 K, it gives a very high characteristic energy, which explains the conduction mechanism as TFE.

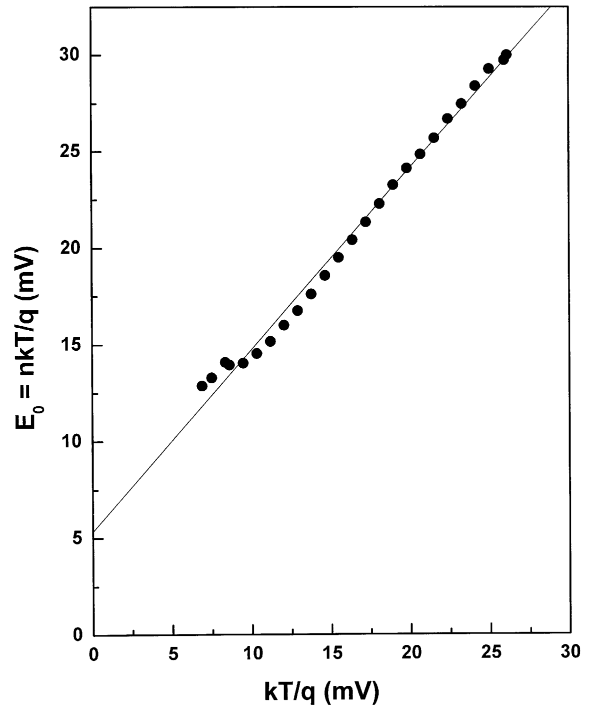

Fig. 4. Plot of E_0 versus kT/q using Eq. (5b) assuming TFE. The slight curvature near 120 K indicates the possibility of a higher characteristic energy than which is predicted by the theory and estimated using Eq. (6).

Values of $1/n$ were theoretically calculated using the following equation [22]:

$$\frac{1}{n} = \frac{KT(1-\beta)}{qE_0} \tag{8}$$

where β indicates the bias dependence of the barrier height. The experimentally observed values of $1/n$ were superimposed on theoretically generated $1/n$ versus $1000/T$ plots in Fig. 5, in order to confirm the higher value of the characteristic energy. This plot provides a good check to know whether the conduction mechanism is TFE or TE. By analyzing the experimental values, a characteristic energy E_{00} of 12 meV and β of 0.02 were obtained for a temperature range of 80–160 K. The characteristic energy is around 17 meV in the temperature range of 160–300 K. At high temperature the E_{00} is 17 meV as observed from Fig. 5. The higher value of E_{00} confirms that at lower temperature the diode conduction mechanism is TFE, while at higher temperature it is TE-diffusion, although it has high base doping (1.3×10^{17} cm^{-3}). The high characteristic energy has been related to several effects such as the density of states and the electric field present on the surface of the

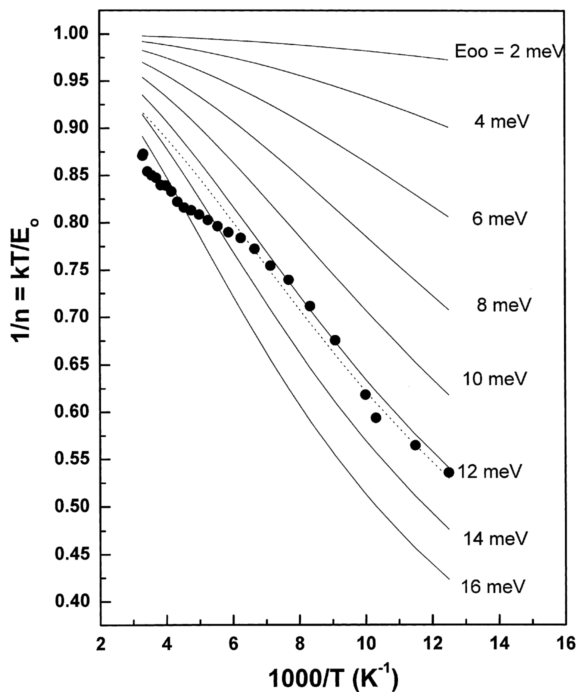

Fig. 5. Plot showing $1/n$ versus $1000/T$ curves (—) with E_{00} as the parameter ranging from 2 to 16 meV in steps of 2 meV generated using Eq. (8) and $\beta = 0$. The experimental points are also superimposed on the theoretically generated plot. The dotted line shown on the plot represents a curve with the value of $E_{00} = 12$ meV and $\beta = 0.02$ in the temperature range of 80–160 K and $E_{00} = 17$ meV in the temperature range of 160–300 K.

semiconductor [22]. The electric field near the semiconductor surface can be increased by mechanisms such as surface roughness at the periphery, local pile-up of dopants, geometrical inhomogeneities due to crystal defects, and the presence of relatively a thick interfacial insulating layer between the deposited metal and the semiconductor surface [22]. Multi-step tunneling through interface states also yields a high characteristic energy [23].

3.3. Effect of generation–recombination

One more reason for higher ideality factors at low temperatures could be due to generation–recombination centers. Recombination–generation current may arise from the defects such as antiphase boundaries, misfit dislocations in the epilayer, deep levels in the forbidden gap, defects arising due to the out diffusion of dopants from the substrate into the epilayer, series resistance effects, and the interface state density distribution.

The measured values of n at 300 and 80 K are 1.14 and 1.80, respectively. The generation–recombination centers could be due to the presence of misfit dislocations, which arise during the heteroepitaxy of GaAs on Ge by the MOVPE growth process. This type of generation–recombination center gives rise to an ideality factor of around 2 at room temperature, as observed in our previous paper [4]. At low temperatures, the defects arising during the MOVPE growth of GaAs on Ge may not be active enough to contribute to the larger value of n. At room temperature, a value of 1.14 matches with the experimental curve and a series resistance of 7 Ω is obtained using Cheung's approach [24].

In general, the quality of the homoepitaxial films is very excellent in comparison with the heteroepitaxial films. Unless the heteroepitaxial MOVPE growth parameters are precisely controlled, there might be some misfit dislocation at the GaAs/Ge heterointerface, which deteriorate the device performance [25]. It is known from the literature [26–28] that 2° off-oriented Ge substrates often give rise to APBs, APDs and misfit dislocations during the growth of GaAs on Ge substrates. The epitaxial films used for the transport studies were characterized by a number of techniques, namely atomic force microscopy, low temperature photoluminescence spectroscopy, secondary ion mass spectroscopy, cross-sectional transmission electron microscopy, and electrochemical capacitance voltage (ECV) profiling, all performed prior to fabricating the Au Schottky diodes. From these techniques, it was observed that the quality of the film was good. Chand et al. [29] studied the I–V characteristics of GaAs on Si and concluded that a minimum number of electrical defect centers caused the higher ideality factor, even though the quality of the film was excellent based on structural and optical results. However, in our case, the GaAs on Ge lattice mismatch is only about 0.07% at room temperature and 0.12% at growth temperature. GaAs on Si, in contrast, is ~4%. Even, this small lattice mismatch, as well as the thermal expansion coefficient mismatch between the GaAs epitaxial layer and the Ge substrate, may create misfit dislocations, which in turn increase the number of generation–recombination centers, unless the growth parameters are precisely controlled.

3.4. C–V characteristics

Fig. 6(a) shows the C–V characteristics at room temperature measured at frequency of 1 MHz and Fig. 6(b) shows the C^{-2}–V characteristics. The voltage intercept gives the value 0.72 eV and the barrier height measured by this method is 0.776 eV. The measured carrier concentration by this method is 1.3×10^{17} cm^{-3}, which is in close agreement with the value obtained by ECV polaron profiler measurements. The difference in the carrier concentration between the two methods was within $\pm 5\%$. The DLTS technique was employed for the determination of the deep levels present inside the GaAs epitaxial film. No noticeable DLTS peaks were observed

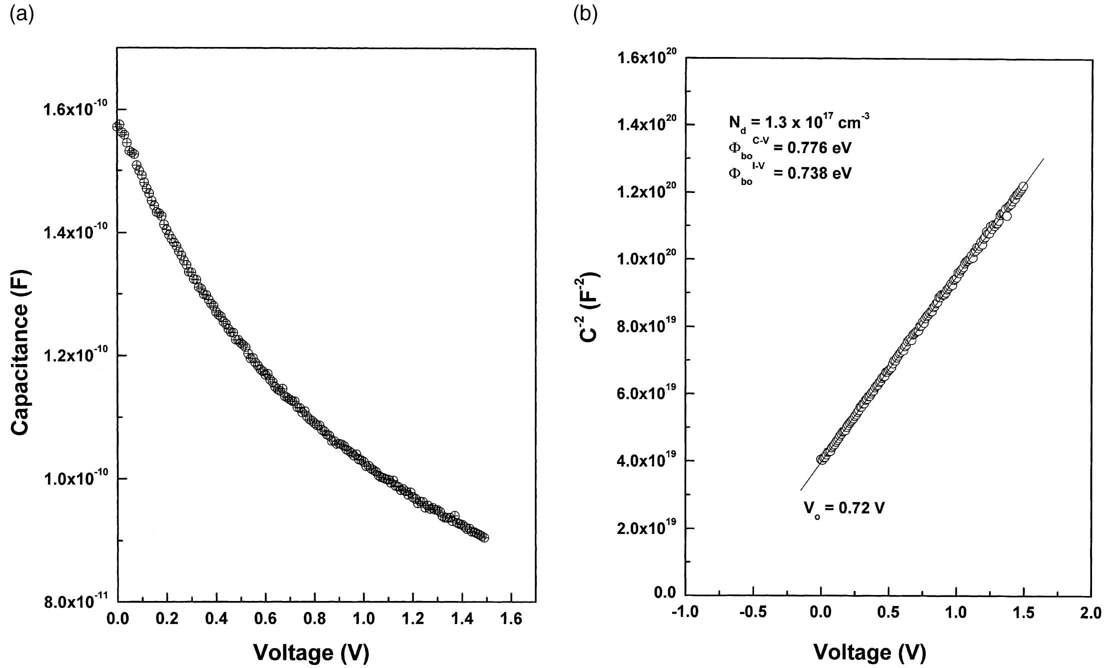

Fig. 6. (a) 1 MHz capacitance–voltage characteristics of Au/n-GaAs/n-Ge Schottky diode, (b) C^{-2} versus V characteristics of the Au/n-GaAs on n-Ge Schottky diode.

in the present studies. Though this may not rule out the possibility of the presence of deep traps, their concentration must be less what the system is sensitive to. Nevertheless, these observations further establish the device quality of epi-GaAs films.

3.5. T_0 effect

The ideality factor of a diode increases as the temperature decreases, which is generally known as the T_0 effect. At many metal–semiconductor interfaces, the observed Schottky barrier height and the ideality factors are found to vary with the measurement temperature. The variation of the ideality factor with temperature is [30,31]

$$n = 1 + \frac{T_0}{T} \tag{9}$$

where T_0 is a constant. Demonstration of the T_0 effect is usually accomplished by plotting nT versus T and observing a straight line with a slope of unity, which does not extrapolate through the origin. This can be seen from Fig. 4; and the slope is 0.95 and the value of T_0 is 60.9 K. The value of T_0 can vary between 10 and 100 K for diodes on the same slice of GaAs [32]. Tung [17] explained the T_0 effect using the barrier height inhomogeneity in the Schottky barrier diode.

3.6. Flat-band barrier height

The barrier height as obtained from TE theory decreases with decreasing temperature. The barrier height obtained from Eq. (2) is called the apparent barrier height or the zero-bias barrier height. The barrier height obtained under flat-band condition is called the flat-band barrier height and is considered as the real fundamental quantity. Unlike the case of the zero-bias barrier height, the electric field in the semiconductor is zero under the flat-band condition. The flat-band barrier height, Φ_b^f is given by

$$\Phi_b^f = n\Phi_{b0} - (n-1)kT \ln\left(\frac{N_c}{N_D}\right) \tag{10}$$

where N_c is the density of the states in the conduction band and N_D is the doping concentration of the film studied here.

The variation of the Φ_b^f as a function of temperature is shown in Fig. 7. The Φ_b^f increases with decreasing temperature in the temperature range of 80–300 K. A linear fit is used to fit the points. The linear fit yields a slope, $d\Phi_b^f/dT$ equal to $-(2.6 \pm 0.052) \times 10^{-4}$ eV K^{-1} and an intercept, $\Phi_b^f(0)$ equal to 0.922 eV. The value of $d\Phi_b^f/dT$ is close to the value obtained by assuming that the variation in the value of $\Phi_b^f(0)$ is entirely due to the variation in the band gap.

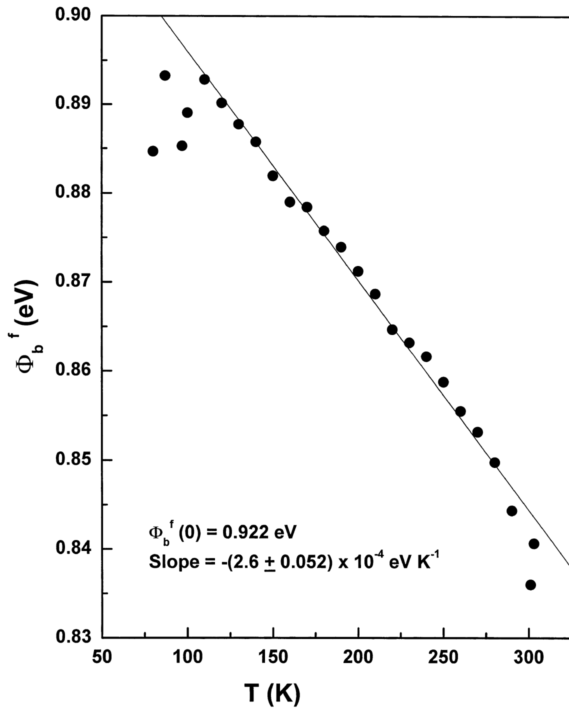

Fig. 7. The flat-band barrier height, calculated using Eq. (10), as a function of temperature. The continuous line represents the best fit to the points in the temperature 80–300 K. The slope and the barrier height at 0 K are shown in the figure.

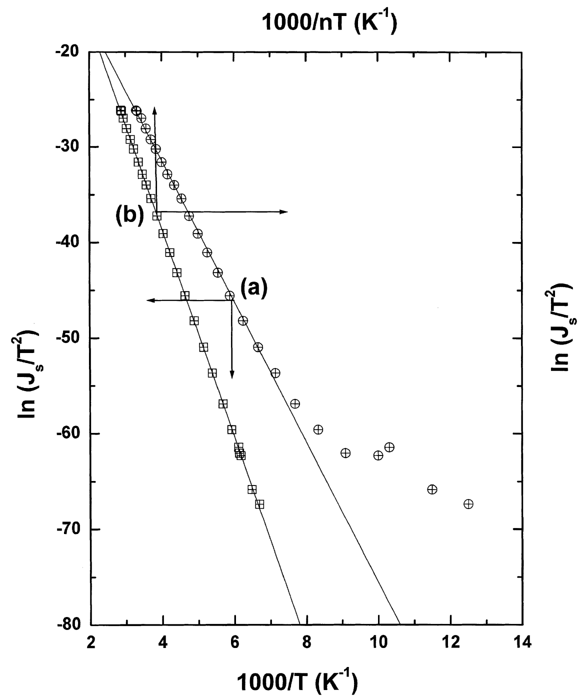

Fig. 8. Activation energy plots of (a) $\ln(J_s/T^2)$ vs $1000/T$ and (b) $\ln(J_s/T^2)$ versus $1000/nT$. The values using (a) show deviation from linearity below the operating temperature of 160 K. The values of A^{**} and the zero-bias barrier height, Φ_{b0} using (a) and (b) are $A^{**} = 0.136$ A cm^{-2} K^{-2}, $\Phi_b = 0.634$ eV using a linear fit to the values in the 160–300 K range and $A^{**} = 143.7$ A cm^{-2} K^{-2}, $\Phi_{b0} = 0.94$ eV, respectively.

3.7. Richardson plots

The Richardson constant A^{**} was usually obtained from $\ln(J_s/T^2)$ versus $1000/T$ plot and the slope gives the barrier height at 0 K. This plot is shown in Fig. 8 and it is linear only in the temperature range of 160–300 K. The obtained Richardson constant and the zero-bias barrier height values are 0.136 A K^{-2} cm^{-2} and 0.634 eV, respectively. Since, if the ideality factor is a strong function of temperature, a modified Richardson plot has been proposed by several authors [10,12,15,33] and is shown in Fig. 8. The modified Richardson plot, which is $\ln(J_s/T^2)$ versus $1000/nT$, gives $A^{**} = 143.7$ A K^{-2} cm^{-2} and $\Phi_{b0} = 0.94$ eV (which is in close agreement with the flat band barrier height, 0.922 eV). The normal A^{**} value is 22 times lesser than the theoretical value of 3 A K^{-2} cm^{-2} [34]. The modified A^{**} value is 48 times higher than the theoretical value and this has been explained in terms of variation of barrier height with the temperature [35,36]. It has been reported in the literature that the Richardson constant varies from 3 to 100 A K^{-2} cm^{-2} [35]. From the observed A^{**} value, the corrected A^{**} value can be obtained from the following equation [35]:

$$A^{**}_{\text{Corrected}} = A^{**}_{\text{observed}} \exp\left[\frac{q}{k}\left(\frac{\mathrm{d}\Phi_b^f}{\mathrm{d}T}\right)\right] \quad (11)$$

where Φ_b^f is the flat band barrier height. The corrected A^{**} value is 7.04 A K^{-2} cm^{-2} which is close to the theoretical value considered (8.16 A K^{-2} cm^{-2}) for extracting zero-bias barrier height values from Eq. (2).

4. Conclusions

The current–voltage characteristics of Au/n-GaAs Schottky diodes on n-Ge substrates were studied in the temperature range of 80–300 K. The zero-bias barrier height decreases and the ideality factor increases with decreasing temperature; the changes are quite significant at lower temperatures. The small discrepancies between the experimental and theoretical values of the barrier height and ideality factor could be due to deviations in the barrier height distribution from the Gaussian model assumed by Werner–Gütler. According to Tung's approach of lateral inhomogeneities, the homogeneous barrier height and the effective barrier heights are closely matched, which shows the good quality of the GaAs film grown on the Ge substrate. There are no effects due to recombination–generation centers, deep levels, or active dislocations present inside the GaAs epitaxial films,

which can in turn increase the ideality factors. The ideality factor was found to show the T_0 effect and a high characteristic energy. The value of the Richardson constant after applying the approximate corrections was found to be 7.04 $A K^{-2} cm^{-2}$, which is close to the value used for the determination of the zero-bias barrier height. The quality of the grown n-GaAs film on the Ge substrate is good, based on the results of electrical characterization; hence, the GaAs/Ge heterojunction can be used in space applications at low temperatures.

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