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Growth and characterization of metamorphic InAs/GaSb tunnel heterojunction on GaAs by molecular beam epitaxy

Jheng-Sin Liu,[1] Michael B. Clavel,[1] Rahul Pandey,[2] Suman Datta,[3] Michael Meeker,[4] Giti A. Khodaparast,[4] and Mantu K. Hudait[1,a)]
[1]*Advanced Devices and Sustainable Energy Laboratory (ADSEL), Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, Virginia 24061, USA*
[2]*Electrical Engineering, The Pennsylvania State University, University Park, Pennsylvania 16802, USA*
[3]*Electrical Engineering, University of Notre Dame, Notre Dame, Indiana 46556, USA*
[4]*Department of Physics, Virginia Tech, Blacksburg, Virginia 24061, USA*

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The structural, morphological, optical, and electrical transport characteristics of a metamorphic, broken-gap InAs/GaSb *p-i-n* tunnel diode structure, grown by molecular beam epitaxy on GaAs, were demonstrated. Precise shutter sequences were implemented for the strain-balanced InAs/GaSb active layer growth on GaAs, as corroborated by high-resolution X-ray analysis. Cross-sectional transmission electron microscopy and detailed micrograph analysis demonstrated strain relaxation primarily *via* the formation of 90° Lomer misfit dislocations (MDs) exhibiting a 5.6 nm spacing and intermittent 60° MDs at the GaSb/GaAs heterointerface, which was further supported by a minimal lattice tilt of 180 arc sec observed during X-ray analysis. Selective area diffraction and Fast Fourier Transform patterns confirmed the full relaxation of the GaSb buffer layer and *quasi-ideal*, strain-balanced InAs/GaSb heteroepitaxy. Temperature-dependent photoluminescence measurements demonstrated the optical band gap of the GaSb layer. Strong optical signal at room temperature from this structure supports a high-quality material synthesis. Current–voltage characteristics of fabricated InAs/GaSb *p-i-n* tunnel diodes measured at 77 K and 290 K demonstrated two bias-dependent transport mechanisms. The Shockley–Read–Hall generation–recombination mechanism at low bias and band-to-band tunneling transport at high bias confirmed the *p-i-n* tunnel diode operation. This elucidated the importance of defect control in metamorphic InAs/GaSb tunnel diodes for the implementation of low-voltage and high-performance tunnel field effect transistor applications. *Published by AIP Publishing.*
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I. INTRODUCTION

Broken-gap InAs/GaSb heterostructures have been used for tunable infra-red imaging and low-power tunnel field-effect transistors (TFETs) due to the ability to tune the structure's bandgap by altering the layer thicknesses[1,2] and the presence of negative differential resistance (NDR) in *p-i-n* (or *p-n*) tunnel diode configurations.[3,4] For over six decades, such tunnel diodes have been extensively studied in several material systems[5–10] and have been utilized in numerous device applications, including energy-efficient transistors,[11,12] multi-junction solar cells,[13,14] quantum-cascade lasers,[15,16] and resonant tunneling diodes.[17] Elemental and compound semiconductors, such as tensile-strained germanium (ε-Ge),[18] germanium-tin alloys (GeSn),[19] and III-V binary[20] and ternary alloys,[21] have shown high tunneling efficiency due to their small effective tunneling barrier heights (E_{beff}), low effective tunneling mass, and direct bandgap nature. In particular, InAs/GaSb tunnel junctions exhibiting a broken-gap energy band alignment provided the highest-reported tunnel transistor drive current.[22] The high ON-state tunneling current in the InAs/GaSb material system is attributed to several factors: (i) the absence of a tunneling barrier height (E_{beff} of −0.15 eV at the tunneling heterointerface), (ii) the low bandgap InAs source, (iii) a high source doping, and (iv) a low tunneling effective mass. However, the abruptness and quality of the InAs/GaSb interface is difficult to control due to atomic flux (arsenic and antimony) intermixing[23] as well as the different surface *ad-atom* mobilities of gallium (Ga) and indium (In) during growth. Thus, during the growth of an InAs/GaSb heterostructure, two forms of interfacial layers can be formed at the heterointerface: (i) GaAs-like and (ii) InSb-like terminating layers. The former introduces additional lattice mismatch (6.7%) to the 0.62% tensile-strained InAs-on-GaSb interface, thereby increasing the likelihood of interfacial misfit dislocation (MD) generation by strain relaxation. In the latter case, an InSb-like interfacial layer at the InAs-on-GaSb interface compensates the 0.62% tensile strain and prevents strain relaxation. Therefore, strain-balanced InAs/GaSb heterostructures can be achieved only by utilizing proper switching sequences between arsenic (As), antimony (Sb), In, and Ga atomic fluxes during growth.

Tunnel field-effect transistors (TFETs) are promising devices for ultra-low supply voltage operation due to their high ON-state current, low subthreshold swing (SS) characteristics, and low OFF-state leakage, all of which result from the band-to-band tunneling (BTBT) generation of carriers at the source/channel (or channel/drain) heterointerface.

a)E-mail: mantu.hudait@vt.edu. Tel.: (540) 231-6663. Fax: (540) 231-3362.

Consequently, the relationship between material and electrical quality in InAs/GaSb heterojunction *p-i-n* tunnel diodes is an important design consideration for high-performance TFET devices. Heterointerface roughness is an additional factor that will affect the InAs/GaSb TFET device performance for metamorphic TFET architectures integrated on GaAs substrates. The lattice mismatch between InAs and the GaAs substrate is 7.2%, which requires a metamorphic buffer architecture to bridge the lattice constant from the GaAs substrate to InAs epilayer. This will further enable to offer a larger total active layer (*p-i-n)* thickness of the InAs/GaSb heterostructure. Moreover, a metamorphic buffer architecture is also essential in mitigating lattice mismatch-induced defects and dislocations and achieving a sharp InAs/GaSb heterointerface, low interface roughness, and an overall strain-balanced active region. *This work* focuses on the growth and characterization of a metamorphic InAs/GaSb tunnel heterojunction grown by molecular beam epitaxy (MBE) on a GaAs substrate. Reflection high energy electron diffraction (RHEED) patterns were recorded at every stage of epilayer growth in order to understand the correlation between *in-situ* surface analysis by RHEED and *ex-situ* surface and interface measurements. The strain relaxation properties of the InAs/GaSb *p-i-n* tunnel diode structure were characterized using high-resolution X-ray diffraction (XRD). The defect properties at the heterointerface between each epilayer were investigated using cross-sectional high-resolution transmission electron microscopy (HR-TEM). The surface morphology was measured by atomic force microscopy (AFM). The optical properties of the *p-i-n* diode structure were evaluated using temperature dependent photoluminescence (PL) spectroscopy. Finally, *p-i-n* tunnel diodes were fabricated and characterized at 77 K and 290 K to validate the material synthesis quality and correlate materials metrology with device-level electrical data.

II. EXPERIMENTAL

Figure 1 shows cross-sectional schematics of the (a) as-grown InAs/GaSb material stack and (b) fabricated InAs/GaSb *p-i-n* tunnel diodes investigated in this work. The InAs/GaSb tunnel diode structure was grown by solid-source MBE on a semi-insulating (100) GaAs substrate offcut 2° toward the ⟨110⟩ direction. A 511 nm GaSb metamorphic buffer layer was grown at 500 °C with an Sb_2/Ga flux ratio of 5 and a growth rate of ~0.43 μm/h (as determined by RHEED intensity oscillations). The growth temperature referred to here is the thermocouple temperature. The GaSb metamorphic buffer was grown to mitigate the defects and dislocations resulting from the large (~8%) lattice mismatch between GaSb and GaAs. Surface oxide desorption of the GaAs substrate was performed at 735 °C under a constant As_2 flux of $\sim 10^{-5}$ Torr. A (2 × 4)-fold GaAs surface reconstruction was achieved prior to the growth of the GaSb layer and was monitored by *in-situ* RHEED. The (2 × 4)-fold RHEED pattern indicated that the residual surface oxides had been successfully removed at this temperature. Beryllium (Be) and silicon (Si) were used to obtain *p*-type GaSb and *n*-type InAs, respectively. Heavily doped contact layers (5×10^{18} cm^{-3}) were incorporated into the device structure in order to reduce device series resistance and provide high-quality ohmic contacts to the InAs/GaSb tunnel junction. A 10 nm InAs capping layer was grown to prevent the unintentional etching of GaSb by photoresist developer during tunnel diode fabrication. The InAs layers were grown at 500 °C at a growth rate of ~0.2 μm/h. A 500 °C growth temperature was selected for both materials as a compromise between the growth temperatures of InAs, where a higher As_2/In ratio is required, and GaSb, where the Sb_2/Ga ratio and temperature are critical, in order to maintain an uninterrupted InAs/GaSb growth. Too high of a growth temperature resulted in poor crystalline quality GaSb and loss of interface abruptness. Strain-balanced structures were achieved utilizing our previously reported shutter sequencing.[20] The As, Sb, Ga, and In shutter sequencing was precisely controlled to ensure atomically smooth, strain-engineered heterointerfaces at the InAs/GaSb and GaSb/InAs junctions, as demonstrated by high-resolution X-ray diffraction and cross-sectional TEM measurements.

The strain relaxation properties of the InAs/GaSb heterojunction were characterized by high-resolution X-ray diffraction. The symmetric (004) and asymmetric (115) reciprocal space maps (RSMs) and (004) X-ray rocking curve (RC, $\omega/2\theta$ scan) of the InAs/GaSb heterostructure were obtained using a PANalytical X'pert Pro system equipped with a Cu Kα-1

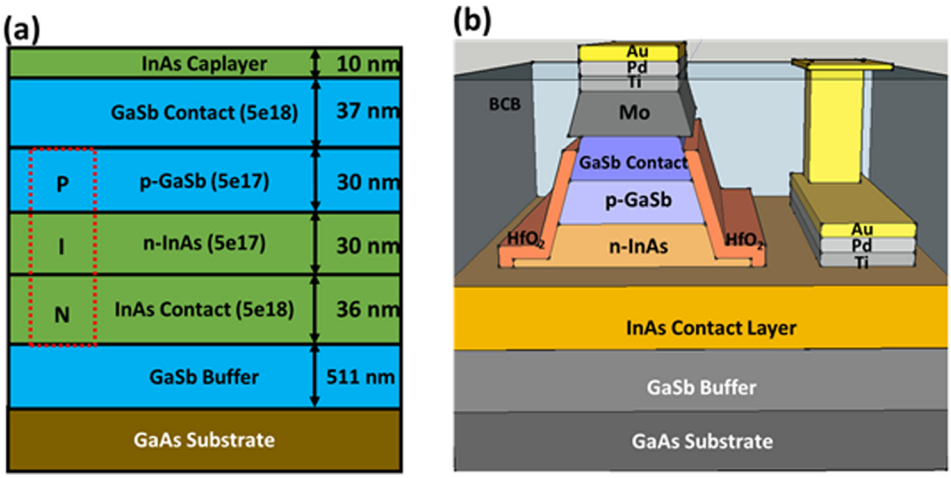

FIG. 1. Cross-sectional schematics of the (a) as-grown InAs/GaSb material stack and (b) fabricated InAs/GaSb *p-i-n* tunnel diodes integrated on to GaAs. The heavily-doped (5×10^{18} cm^{-3}) GaSb:Be and (5×10^{18} cm^{-3}) InAs:Si epitaxial layers act as low-resistance contact layers to the tunnel junction, while the InAs capping layer prevents unintentional GaSb etching during device fabrication.

X-ray source. High-resolution TEM measurements evaluated the epilayer structural quality as well as the defect properties of the tunnel heterointerface and were performed on a JEOL 2100 transmission electron microscope. Cross-sectional electron transparent foils were prepared by mechanical polishing, dimpling, and low-temperature (−120 °C) Ar^+ ion-milling. Ion-milling under vacuum (Fischione model 1010) in a low-temperature environment prevents potential thermal damage and re-deposition of milled material stemming from ion bombardment. Photoluminescence experiments were performed using a Ti:Sapphire laser with a repetition rate of 80 MHz. The excitation wavelength was 700 nm, with average powers of 12–50 mW and a spot size of ∼200 μm. The light was passed through a 0.55 m focal length spectrometer and collected by an enhanced InGaAs detector.

Tunnel diodes employing a vertical transport geometry were fabricated using the vertical heterojunction tunnel FET fabrication process described elsewhere.[11,24] In this process, 300 nm molybdenum (Mo) is sputter deposited on the material stack. The etch mask for the diode mesa was defined using electron-beam lithography (EBL) followed by a 30 nm Ti and 60 nm Cr e-beam evaporation and metal lift-off process. A chlorine (Cl_2)-based inductively coupled plasma dry etch process was used to etch the diode mesa until the GaSb/InAs tunnel-junction was exposed, whereas the mesa sidewalls were passivated using a 4 nm atomic layer deposited high-κ dielectric, i.e., HfO_2. The source contact was patterned using EBL on the bottom-most InAs layer with a subsequent 20 nm Ti, 20 nm Pd, and 30 nm Au deposition using e-beam evaporation. Benzo-chloro butane (BCB) was deposited as an inter-level dielectric and etched back to create the drain contact on top of the mesa structure. The drain contact was then patterned *via* EBL, followed by a 20 nm Ti, 20 nm Pd, and 60 nm Au metal evaporation. Finally, the remaining BCB was etched back to access the source pad. Electrical characterization was performed on an ARS Cryo temperature-dependent, ultra-high vacuum probe station in the temperature range of 77 K to 290 K. A Keithley 4200-SCS semiconductor characterization system, a modular, fully integrated parameter analyzer, was used for device testing and interfaced with the low temperature ARS Cryo probe station during measurement.

III. RESULTS AND DISCUSSION

A. RHEED studies on epitaxial GaSb/InAs/GaSb/GaAs heterostructures

To elucidate the surface morphologies of (i) GaAs, (ii) the GaSb buffer on GaAs, (iii) InAs on GaSb, and (iv) GaSb on InAs, RHEED patterns were recorded at different stages during growth at a fixed growth temperature of 500 °C. The (001) surface of compound semiconductors shows a variety of reconstructions depending on the growth conditions.[25] For example, (100) GaAs can exhibit As-stabilized (2 × 4) or Ga-stabilized (4 × 2) surface reconstruction patterns, which, upon exposure to Sb_2 flux, can transform to a (2 × 8) reconstruction,[26] indicating the incorporation of Sb atoms on the (4 × 2) reconstructed GaAs surface. Hence, the highly-sensitive RHEED technique was used in this work to observe the possible changes in surface reconstruction at each heterointerface, especially after the growth transitions between InAs on GaSb or GaSb on InAs. Figure 2 shows elongated, streaky RHEED patterns along the [100] azimuth for the growth sequence of top-GaSb/InAs/GaSb/(100)2°GaAs, including the: (a) (100)/2° GaAs substrate showing a (2 × 4) pattern, (b) GaSb buffer exhibiting (1 × 3)-fold surface reconstruction, (c) InAs layer showing (2 × 4)-fold surface reconstruction on top of the GaSb buffer, and finally (d) GaSb on InAs displaying a (1 × 3)-fold surface reconstruction. RHEED patterns were recorded after 1 min of GaSb growth on InAs or InAs growth on GaSb. The sharp RHEED patterns from the surface of InAs and GaSb are consistent with results from other researchers.[27,28] A 15 s exposure of Sb_2 flux was used prior to growth to prevent As_2 from escaping the initial GaAs growth surface at 500 °C growth temperature. Note that there was no exposure of Sb_2 flux while cooling down from the 735 °C GaAs oxide desorption, which instead was performed under As_2 flux. Once the GaAs surface temperature was stabilized at 500 °C following oxide desorption under the As_2 over pressure (As_2 flux of ∼10^{-5} Torr), the GaAs surface was exposed to Sb_2 flux (Sb_2/Ga = 5) for 15 s prior to opening the Ga shutter for GaSb growth. This sequence of flux exposures prevented volatile As_2 from escaping the growth surface and aided in evacuating the As_2 flux prior to the growth of the GaSb buffer layer. It is important to have a sufficient residence time for the Sb_2 atoms on the surface prior to the GaSb growth; hence a 15 s Sb_2 exposure time (after closing the As_2 flux) was selected for this work. Valved cracker sources for both Sb_2 and As_2 were used in this work, wherein the cracker temperatures (1000 °C and 900 °C for Sb_2 and As_2, respectively) were selected to provide both Sb_2 and As_2 flux during growth.

B. Strain relaxation properties via X-ray analysis

Figure 3 demonstrates the strain relaxation properties of the InAs/GaSb tunnel diode structure investigated by high-resolution X-ray diffraction. Figure 3(a) shows the symmetric (004) X-ray rocking curve (RC) of the InAs/GaSb heterostructure grown on a (100)/2° GaAs substrate. One can find from this figure that the GaSb layer is fully relaxed with respect to the GaAs substrate and the lower lattice constant InAs relative to GaSb is located on the right hand side of the GaSb layer peak, as expected. The broadening of the GaSb layer peak is due to lattice mismatch induced defects and dislocations generated *via* strain relaxation during growth. Figure 3(b) shows the symmetric (004) reciprocal space map (RSM) of the InAs/GaSb heterostructure grown on GaAs. The symmetric reciprocal space map allows for the determination of the out-of-plane lattice constant of each layer. One can find from Figure 3(b) that the reciprocal lattice point (RLP) for each epilayer is nearly vertically aligned with the RLP of the GaAs substrate, indicating a minimal lattice tilt in the InAs/GaSb heterostructure. Kang *et al.*[29] revealed that regular 60° misfit dislocations (MDs) with matching Burger vector orientations located at the GaSb/GaAs heterointerface introduce an asymmetric tilt to the final heterostructure. The elastic energy per unit area for the three possible MD

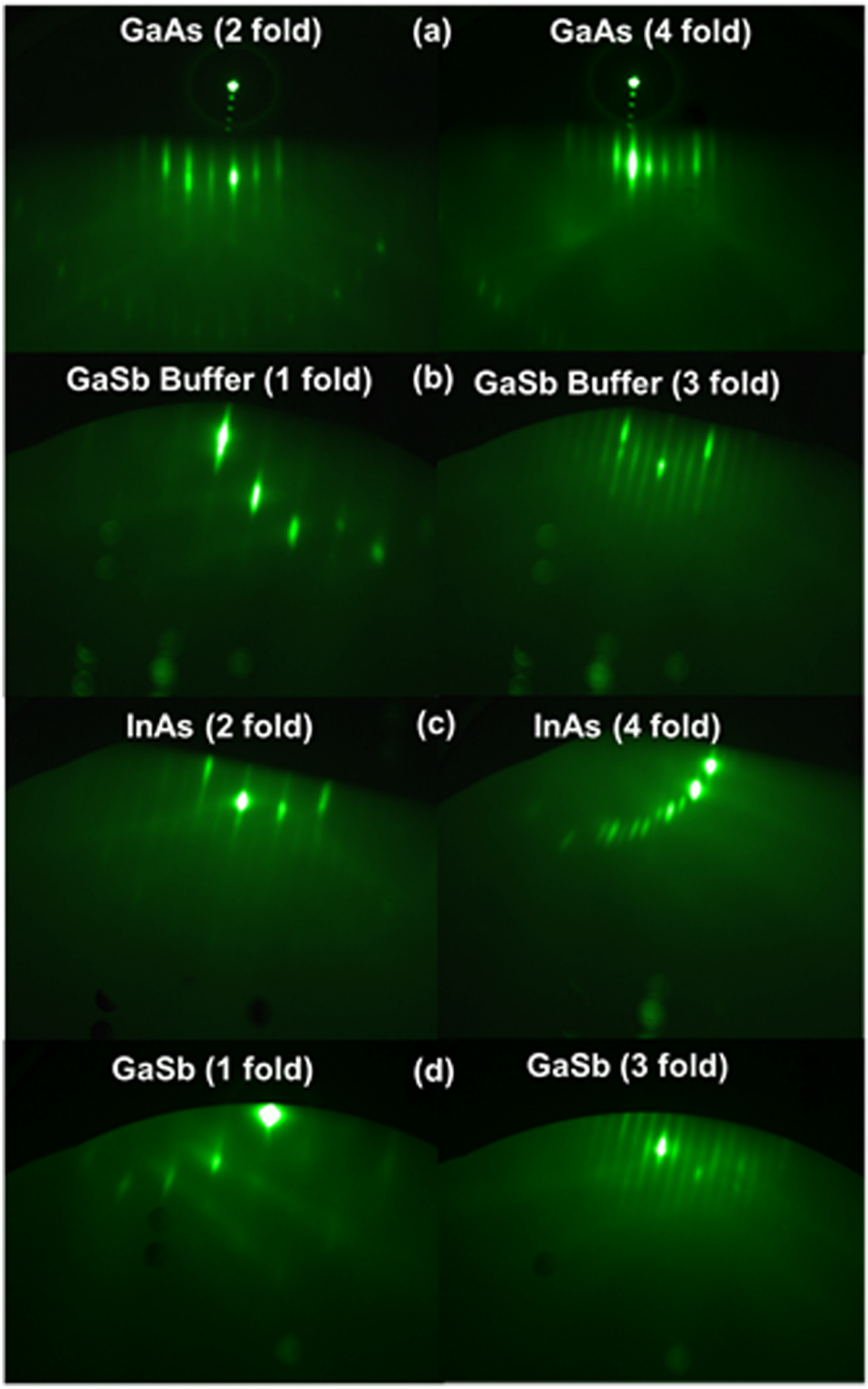

FIG. 2. RHEED patterns at 15 keV from the surface of (a) a representative (100) GaAs substrate, (b) the GaSb buffer on GaAs, (c) the InAs layer on GaSb buffer, and (d) the GaSb epilayer on InAs epitaxial layer, all along the [100] azimuth. These RHEED patterns were recorded for each layer throughout the heterostructure growth. The RHEED patterns exhibited streaky (2×4), (1×3), (2×4), and (1×3) surface reconstruction for the (100) GaAs substrate, GaSb epilayer, InAs epilayer, and upper GaSb layer grown on InAs, respectively. The surface reconstruction of each layer is included in the figure.

configurations,[29] i.e., 90° Lomer MDs, 60° MDs with opposing Burger vectors, and 60° MDs with matching Burger vectors, are 0.27 J/m^2, 0.63 J/m^2, and 0.42 J/m^2, respectively. Out of these three possible MDs distributions, 90° Lomer dislocations are the preferable strain relaxation mechanism due to their lack of a tilt component, in contrast to 60° MDs. Therefore, Figure 3(b) suggests the presence of pure-edge 90° Lomer dislocations along with minimal 60° MDs at the GaSb/GaAs heterointerface since the observed lattice tilt is approximately 180 arc sec. Further, it has been reported that a 2° substrate offcut can generate a lattice tilt on the order of 200 arc sec for mixed-anion InAsP layers (∼1.4% lattice mismatch) on InP substrates.[30] Although the substrate offcut effect was compensated for during the X-ray measurements, the 180 arc sec lattice could also be due to the combined effect of 60° MDs and substrate offcut, although the individual contributions could not be identified. Furthermore, 60° MDs with opposite Burger vectors, although not probable as suggested by Kang *et al.*,[29] could not be ruled-out from this figure. The distribution of MDs at the GaSb/GaAs interface,

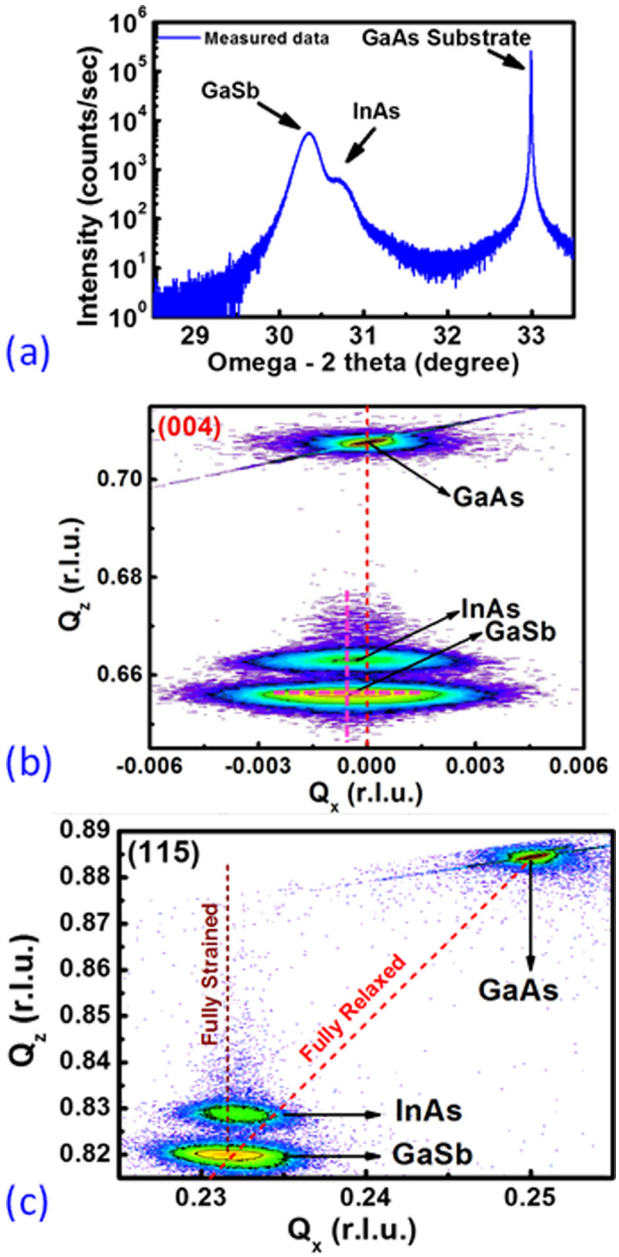

FIG. 3. (a) Experimental symmetric (004) rocking curve, (b) symmetric (004), and (c) asymmetric (115) reciprocal space maps of the InAs/GaSb tunnel diode heterostructure revealing a fully relaxed GaSb buffer and quasi-ideal strain transfer to the InAs epilayer. Minimal lattice tilt was observed in the (004) RSM, as denoted by the vertical line (pink) through the GaSb/InAs epilayers.

whether an array of 90° or 60° MDs, can be more thoroughly analyzed by high resolution TEM microscopy, discussed later in this paper.

Figure 3(c) shows the asymmetric (115) RSM for the InAs/GaSb heterostructure on GaAs. The in-plane lattice constant was measured from the (115) reciprocal space map, and using the out-of-plane lattice constant from the (004) RSM, the strain relaxation of the GaSb layer was determined. The strain relaxation for the 511 nm GaSb buffer layer with respect to the GaAs substrate was determined to be $\sim$ 98%. Moreover, the RLPs of the GaAs substrate and the GaSb epilayers lie along the relaxation line, indicating that the 511 nm thick GaSb metamorphic buffer was fully relaxed with respect to the GaAs substrate. Furthermore, the RLP of the InAs epilayer was found to be vertically aligned to the GaSb virtual substrate, indicating the quasi-ideal, strain-balanced growth of the InAs/GaSb heterostructures on GaAs. The nature of the strain relaxation in the InAs/GaSb heterostructures can be further confirmed by cross-sectional TEM analysis.

C. Structural analysis *via* transmission electron microscopy

Additional investigation into the InAs/GaSb structural and heterointerface quality was performed using cross-sectional TEM, as shown in Figure 4. Figure 4(a) shows a TEM micrograph of the entire InAs/GaSb heterostructure, consisting of *p*-type GaSb and *n*-type InAs epilayers as well as the metamorphic GaSb buffer grown on GaAs. Each layer material and interface has been labeled in addition to the epilayer thicknesses. The cross-sectional TEM image shows high contrast at the GaSb buffer layer/GaAs substrate interface due to misfit dislocations. Moreover, the GaSb metamorphic buffer was observed to confine the lattice mismatch-induced misfit and threading dislocations to within 100 nm of the GaSb/GaAs interface, indicating subsequent device-quality active region epitaxy. This conservatively suggests that the threading dislocation density (TDD) in the active InAs or GaSb layers is below 10^7 cm^{-2}.

1. Heterointerface analysis

Figures 4(a)–4(d) show high-resolution TEM micrographs of the active device region. One can find from Figure 4(b), which shows the lattice indexing of the heterointerface between the InAs capping layer and the *p*-type GaSb contact layer, that a smooth, uniform interface was observed, thus enhancing ohmic contact and reducing contact resistance. Likewise, Figures 4(c) and 4(d) demonstrate abrupt heterointerfaces between the GaSb (metamorphic buffer) and the InAs (heavily-doped contact) layers. The sharp junction and defect-free interfaces suggest the absence of GaAs-like interfacial layer formation due to the intentionally grown, ultra-thin InSb layers. Compared with the small lattice mismatched InAs-GaSb (0.62%) system, growth of a GaAs-like interfacial layer drastically reduces the critical layer thickness of subsequent epilayers by providing increased tensile strain (InAs-GaAs, 7.2% lattice mismatch). The intentional growth of an InSb-like interfacial layer, as discussed above, thus compensates the epitaxial strain in the system, ensuring high-quality InAs and GaSb growth and minimizing the creation of defects at the tunneling interface.

Figure 4(d) shows the Fast Fourier Transform (FFT) patterns representative of the regions denoted by arrows. The FFT patterns obtained from the *p*-type GaSb, GaSb/InAs tunneling heterointerface, and the *n*-type InAs layer are identical and absent of satellite peaks or diffraction spot splitting. Hence, Figure 4(d) indicates that the diffraction peaks (in reciprocal space) shown in the FFTs are representative of a singular lattice parameter, further validating the fully strained nature of the GaSb/InAs interface and reinforcing the XRD analysis presented earlier. Moreover, the absence of visible defects and

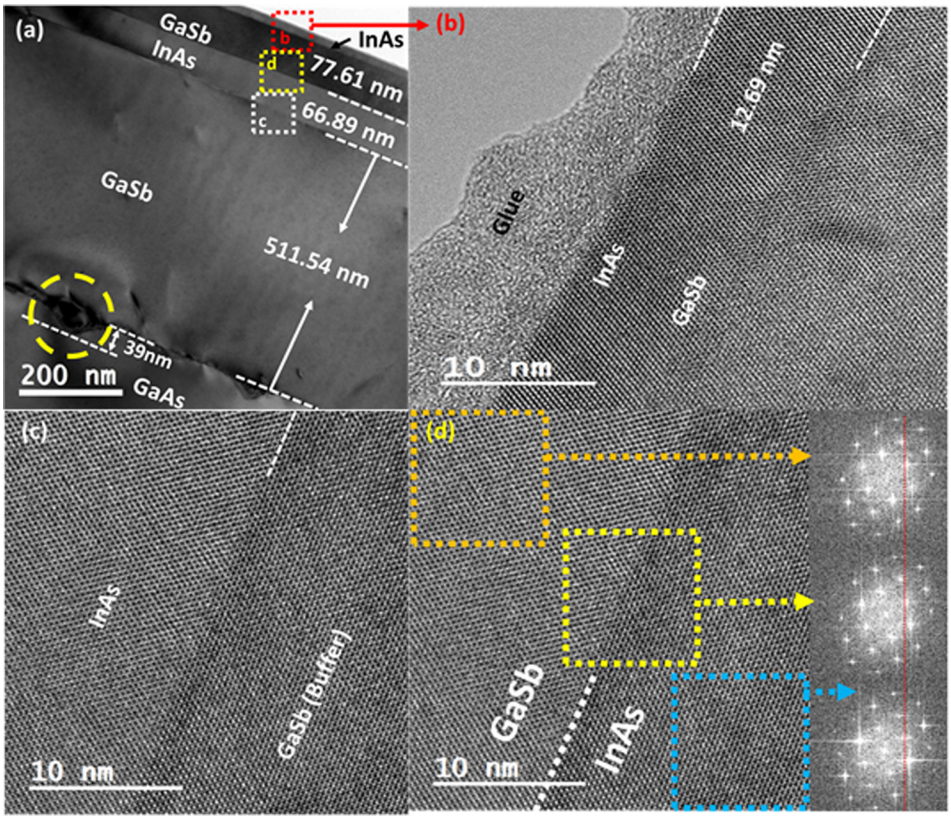

FIG. 4. (a) Cross-sectional TEM micrograph of the InAs/GaSb diode structure grown on GaAs using a metamorphic GaSb buffer. Lattice-mismatch-induced defects and threading dislocations were found to be confined to the GaSb/GaAs interface. High resolution micrographs of the (b) InAs etch-stop and *p*-type GaSb contact layer, (c) InAs/GaSb buffer heterointerface, and (d) *p*-type GaSb on *n*-type InAs active tunneling heterointerface. Fast Fourier Transform patterns obtained from the *p*-type GaSb (orange, top right), GaSb/InAs heterointerface (yellow, middle right), and the *n*-type InAs layer (blue, bottom right). No satellite peaks or diffraction spot splitting is observed, indicating internally lattice matched epitaxy across the critical GaSb/InAs tunnel heterojunction.

dislocations in the active region, as demonstrated by HR-TEM analysis, is expected to minimize traps in the bandgap and improve the transport characteristics of InAs/GaSb *p-i-n* tunnel diodes.

2. Interfacial-misfit dislocation array (IMF)

Due to the large lattice mismatch (~7.83%) between the GaSb epilayer and GaAs substrate, several buffer schemes have been developed[31–33] so as to mitigate the defects introduced by the differences in lattice constant and thermal expansion coefficient of GaSb and GaAs. One such approach, the interfacial misfit (IMF) array formation technique, has been reported to achieve highly-relaxed (~98%) GaSb layers with low dislocation densities ($\leq 10^6\,cm^{-2}$).[34] In the IMF array growth mode, a periodic array of Lomer MDs are formed at the GaSb/GaAs interface by careful control over the growth conditions. Huang *et al.*[34] and Jallipalli *et al.*[35] suggested that the generation of an IMF array can only be achieved by carefully monitoring the GaAs surface while creating As deficits (using a growth temperature of 510 °C), which lead to the direct formation of pure 90° Lomer dislocation networks at the GaSb/GaAs heterointerface. Furthermore, because 90° Lomer MDs are pure-edge dislocations, they can travel parallel to the growth plane.[36] Thus, the formation of such pure 90° Lomer MDs relieves strain energy much faster than the formation of 60° misfit dislocations[37] and does not generate TDD that can propagate into the relaxed GaSb layer.[38] Recent studies have indicated that 60° MDs also form, which create asymmetric tilt at the GaSb/GaAs heterointerface[29] and further complicate the nature of the generated dislocations (60° MDs, 90° Lomer, and mixed 60° MDs) formed between the GaSb and GaAs layers.[34]

In this work, we have analyzed the GaSb/GaAs heterointerface by cross-sectional TEM imaging, selective area diffraction (SAED) patterns, and filtered FFT analysis to identify the type of dislocations that can generate minimal lattice tilt and full relaxation. Figures 5(a), 5(b), and 5(d) show the high-resolution cross-sectional TEM micrographs of the GaSb buffer/GaAs substrate heterointerface and Figure 5(c) shows the selective area diffraction (SAED) pattern of the GaSb/GaAs heterointerface. One can find from Figure 5(c) that the SAED pattern demonstrated a complete relaxation of the GaSb/GaAs system, where the inner diffraction spot represents the GaSb lattice and the outer diffraction spot represents the GaAs lattice (in reciprocal space). The distance between the center diffraction spot to the inner diffraction spot can thus be related to the atomic plane spacing of GaSb. The atomic plane spacings obtained from the SAED pattern containing GaSb and GaAs diffraction peaks were ~6.009 Å and ~5.571 Å, respectively, within a 2% error of the reported literature values for GaSb and GaAs, respectively. No tertiary diffraction points were observed, indicating cubic GaSb and GaAs lattices (in reciprocal space) absent of stacking faults or micro-twins.

The interface between GaSb and GaAs was analyzed to identify the types of MDs at the GaSb/GaAs heterointerface. Figure 5(e) represents the filtered HR-TEM (reconstructed from an inverse FFT) image of misfit dislocations at the GaSb/GaAs heterointerface. The reconstructed HRTEM image from Figure 5(b) is used to clearly distinguish the interruption in the lattice lines at the interface, thereby allowing an easier identification of the types of dislocations at the

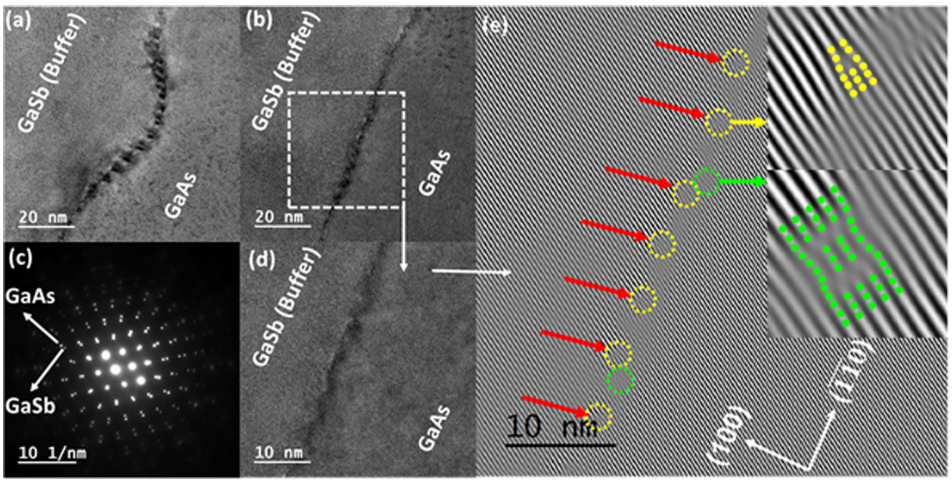

FIG. 5. (a) and (b) High resolution cross-sectional TEM micrographs of the GaSb buffer on GaAs substrate, (c) selective area diffraction patterns of the relaxed GaSb/GaAs interface showing the diffraction spots of relaxed cubic GaAs and GaSb lattices in reciprocal space, (d) high-resolution micrograph of (c), and (e) filtered FFT patterns of the GaSb/GaAs heterointerface showing 90° Lomer dislocations (red arrow, yellow circle) periodically separated every 5.6 nm, corresponding to a near-complete GaSb buffer relaxation.

interface. The MDs appear as linear defects in the plane of the GaSb/GaAs heterointerface and are considered as an insertion of an extra half-plane of atoms in the otherwise perfect crystal. In a compressively lattice mismatched material system, where the epitaxial layer lattice constant is higher than the substrate lattice constant, the MD is associated with an extra half-plane of atoms in the substrate (i.e., a negative edge dislocation). One can find from Figure 5(e) that the observed MDs were 90° Lomer dislocations periodically separated every 5.6 nm (highlighted by red arrows and yellow circles pointing to the 90° Lomer MDs), which is in agreement with the theoretical spacing between Lomer dislocations in a relaxed system.[34,39,40] As reported in the literature, if Lomer dislocations are the only MDs present in the GaSb on GaAs system, then threading dislocations (TDs) will be avoided.[29] Under certain reported growth conditions, the TD density was reduced by 3 orders of magnitude, but not entirely eliminated.[41] In such a situation, both 90° Lomer and 60° MDs must exist at the heterointerface between GaSb and GaAs. It has also been reported that two possible types of MDs, pure-edge and mixed, are typically formed in a metamorphic graded buffer, where the pure-edge dislocations are twice as effective in relieving lattice mismatch-induced strain.[41] After carefully investing the MDs at the heterointerface of GaSb/GaAs in this work, mixed 60° dislocations are observed (green circles). These mixed dislocations are anchored between the substrate and the epilayer lattice plane (highlighted in light green). In a III-V lattice mismatched material system, symmetric strain relaxation along the two orthogonal ⟨110⟩ directions occurs by the formation of an equal number of α [1$\bar{1}$0] and β [110] dislocations, in which minimal or zero lattice tilt was thought to be observed for equal numbers of α and β dislocations with opposing tilt vectors. Hence, the differences in α and β dislocations are responsible for the lattice tilt. Moreover, 90° pure edge dislocations do not have a tilt component; thus the 180 arc sec lattice tilt shown in Figure 3(b) are believed to be due to the formation of mixed 60° MDs. Therefore, the TEM microstructural analysis was corroborated by the X-ray analysis above.

D. Surface morphology *by* atomic force microscopy

The surface morphology of the InAs/GaSb heterostructure was characterized by AFM and is shown in Figure 6. Line profiles along the two orthogonal ⟨110⟩ directions were also taken from the 20 μm × 20 μm scan, also shown

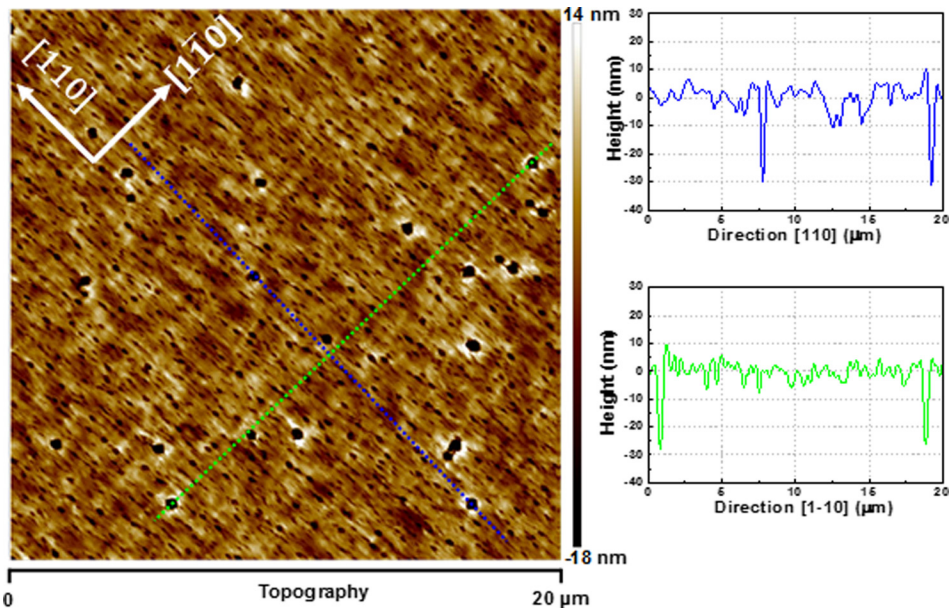

FIG. 6. AFM micrograph and line profiles in the two ⟨110⟩ directions of the broken-gap InAs/GaSb tunnel diode structure grown on a (001)/2° GaAs substrate.

in Figure 6. The uniform pattern from the surface of the InAs/GaSb metamorphic tunnel diode structure is an indication of full relaxation, in complete agreement with the X-ray results and analysis presented above. The root mean square (*rms*) surface roughness for the metamorphic InAs/GaSb tunnel diode structure is ~4.3 nm measured over an area of $20 \times 20\ \mu m^2$. This surface roughness value is comparable with reported results for metamorphic graded buffers of lattice mismatch ranging from 4% to 8%.[42,43] However, the presence of scattered dark regions observed in the AFM micrograph likely indicates the formation of pinholes, approximately 30 nm–40 nm in depth, as shown in the line height profiles. The formation of these pinholes is a result of interfacial roughness at the GaSb/GaAs heterointerface, and can be further linked to the formation of ~39 nm deep pits, as shown in Figure 4(a) (highlighted in yellow). Furthermore, the interfacial roughness observed at the GaSb/GaAs heterointerface may be due, in part, to increased adatom intermixing at elevated growth temperatures, which would have a significant impact on the planarity of the growing film(s). The difference in binding energies between Ga-As bonds (~1.55 eV) and Ga-Sb bonds (~1.3 eV)[44] leads to an exchange of Sb and As atoms at the GaSb/GaAs interface. Further, high temperature growth (relative to the material systems) provides increased kinetic energy to surface adatoms, making it difficult to maintain equilibrium growth conditions at the interface. Moreover, the large lattice mismatch between GaSb and GaAs enhances interfacial intermixing due to an increase in chemical potential with increasing strain, thus undermining interfacial stability and promoting interfacial diffuseness. As result, pinholes appeared on the sample surface after epitaxial growth on such a rough interface. Incidentally, the lattice mismatched-induced surface roughness cannot be eliminated for a metamorphic growth as compared with near lattice matched InAs-on-GaSb substrate or GaSb-on-InAs substrate growth. However, defect control within the GaSb buffer and at the active InAs/GaSb heterointerface of interest is an important design criterion for metamorphic broken-gap tunnel field effect transistor applications.

E. Optical studies *via* photoluminescence spectroscopy

Photoluminescence (PL) spectroscopy is one of the most powerful optical characterization techniques and has been widely recognized by the semiconductor industry for many years. This method can determine material quality, heterostructure interfaces, heterointerface band offsets, and optical bandgap, and also has the ability to determine impurity level(s) in semiconductors. Figure 7(a) shows the PL spectra for measurement temperatures in the range of 81 K to 300 K collected from the multi-layer structure described in Figure 1. The PL spectra were shifted vertically for clarity as well as to see the peak evolution as a function of temperature. The PL peak position at 0.73 eV measured at 300 K is attributed to the band to band optical transition from GaSb in which the peak position is related to the bandgap energy of GaSb. Although the diode structure has several GaSb layers with different doping levels, resolution of multiple peaks in the PL spectrum is not possible due to the thermal broadening of the GaSb emission spectra coupled with the resolution limit of the experimental measurement setup. Hence, our experimental results are in agreement with the previously reported results for a single layer GaSb material.[45,46] Moreover, the radiative efficiency of GaSb is sufficiently high so as to further broaden and merge any doping-dependent GaSb PL peaks such that

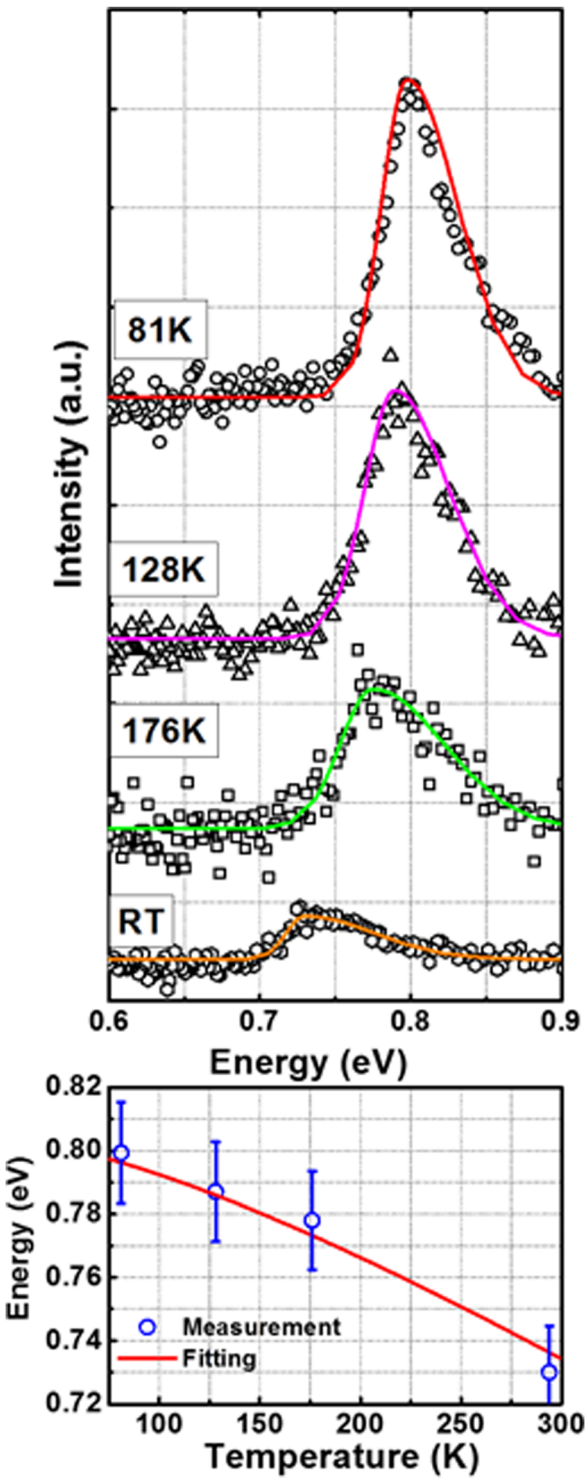

FIG. 7. (a) PL spectra of InAs/GaSb tunnel diode structure on (100)/2° GaAs as a function of temperature from room temperature to 81 K. (b) Band gap energy as a function of measurement temperature. The solid line (red) represents the fit to the measured data (blue circle with error bar) using Varshni coefficients of $\alpha = (4.2 \pm 0.5) \times 10^{-4}$ eV/K and $\beta = (234 \pm 15)$ K.

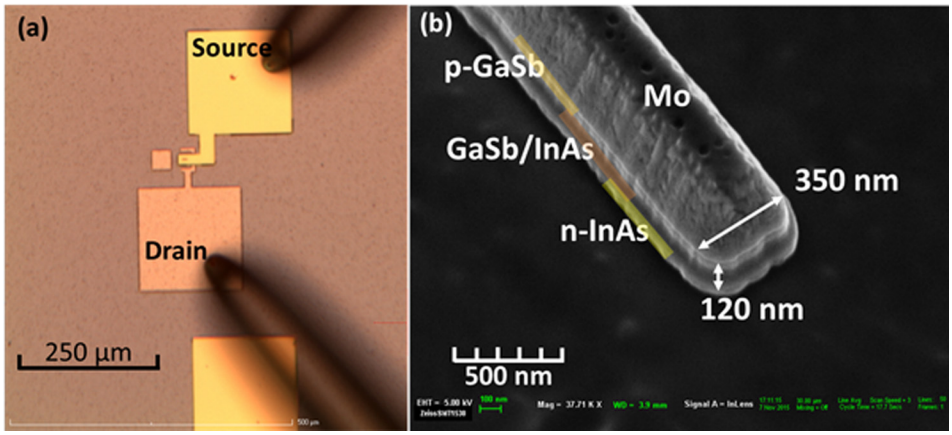

FIG. 8. (a) Optical image of a fabricated InAs/GaSb *p-i-n* tunnel diode showing the source (InAs) and drain (GaSb) contact pads (sample under test), and (b) tilted view scanning electron microscopy image showing the molybdenum (Mo) metal contacting the III-V hetero-layers and diode dimensions. The area of the fabricated diode is 0.875 μm^2.

experimental deconvolution of these two peaks is unlikely even at 4.2 K. The increase in PL intensity with decreasing measurement temperature is due to the minimization of the thermal ionization of defect centers and a reduction in the phonon assisted recombination process. The peak position at each temperature was determined by fitting a Gaussian line distribution to the experimental data. Moreover, the dependence of band gap energy on temperature is evident from the shift in the peak position with decreasing temperature. The peak position is shifted toward higher energy with decreasing temperature, which is expected due to the increase in bandgap energy of GaSb at lower temperatures. Further, the PL spectra are more symmetric at lower temperature than higher temperature. The electron energy follows a Fermi–Dirac distribution, i.e., at lower band gaps (or high temperatures), there is a larger density of states for a given energy; however, electrons are also more likely to have higher kinetic energy as the electronic temperature increases, thereby resulting in a high energy tail in the PL spectra. Due to the limitation of the detector wavelength range, the InAs layer peak could not be determined; however, the absorption lengths for GaSb and InAs were estimated to be 97 nm and 108 nm, respectively.[47]

The relationship between the bandgap energy and the temperature can be established using an empirical formula developed by Varshni:[48]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{\beta + T}, \quad (1)$$

where E_g (0) is the extrapolated bandgap energy at 0 K (0.805 eV), α and β are the Varshni coefficients, and T is the temperature. Figure 7(b) shows the bandgap energy as a function of temperature (blue circles, experimental) where the solid line (shown in red) represents the fit to the data using the above Equation (1). One can find from Figure 7(b) that there is an excellent fit to the experimental data for the entire range of investigated temperatures and bandgaps. From this fitting, the Varshni coefficients α and β are determined to be $\alpha = (4.2 \pm 0.5) \times 10^{-4}$ eV/K and $\beta = (234 \pm 15)$ K, respectively, which is in agreement with previously reported results for GaSb.[46,49] For several decades, this relationship has been utilized for different material systems in which the temperature dependence of E_g is believed to be due to (i) the change in bandgap energy by electron–phonon interaction, and (ii) the thermal expansion of the material at different temperatures.[50] The electron–phonon interactions are more pronounced at higher temperature than at lower temperature, which gives rise to the decrease in E_g as a function of increasing temperature. The strong PL intensity at 300 K, notwithstanding several interfaces in the active device region, provided an opportunity to guide and optimize the broken-gap GaSb/InAs tunnel diode structure as a part of the tunnel field-effect transistor.

F. Electrical transport characteristics of InAs/GaSb diodes

In order to validate the comprehensive materials analysis and investigate the electrical quality of the tunneling heterointerface, vertical nano-pillar tunnel diodes were fabricated using a previously established vertical heterojunction tunnel FET fabrication process.[11] Figures 8(a) and 8(b) show the optical image of a fabricated tunnel diode and the tilted view scanning electron microscope image of the diode mesa sidewall, respectively. Figure 9 shows the drain current density (J_{DS}) versus drain voltage (V_{DS}) characteristics of a fabricated InAs/GaSb *p-i-n* tunnel diode measured at 77 K and 290 K. One can find that the tunnel diode exhibits a significant temperature dependence in J_{DS}-V_{DS} characteristics at low V_{DS}. This can be attributed to the Shockley–Read–Hall (SRH)

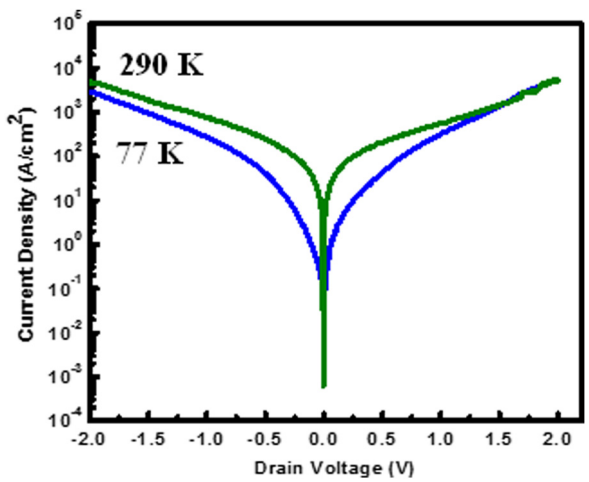

FIG. 9. Current density versus drain voltage characteristics of the fabricated *p-i-n* tunnel diode showing two regions with different transport mechanisms.

generation–recombination or trap-assisted tunneling mechanisms, which are dominant at low drain bias. At high drain bias, the drain current magnitude is governed by inter-band tunneling, which manifests as a steep rise in drain current density. Furthermore, similarity in reverse- and forward-bias current densities implies that the device exhibits a strong leakage current, and hence a high leakage current floor. In this work, the sources for the excess current are likely to be defects within the device layer.[51] These defects could arise from the pinholes discussed in the AFM section, which would introduce additional leakage paths and make it difficult to decouple the dominant leakage current mechanisms. This exemplifies the importance of the InAs/GaSb tunnel diode structure heterogeneously integrated on silicon for low-voltage and high-performance tunnel field effect transistor applications.

IV. CONCLUSIONS

In summary, strain-balanced InAs/GaSb multilayer tunnel heterostructures were integrated on (100)/2° GaAs substrates using solid source MBE by carefully monitoring the shutter sequences and the growth parameters. X-ray analysis confirmed the pseudomorphic nature of the strain-balanced InAs/GaSb tunnel diode heterostructure as well as the metamorphic nature of the fully-relaxed GaSb buffer on GaAs. Cross-sectional TEM micrographs revealed confinement of lattice-mismatch-induced misfit and threading dislocations well below the device active region, sharp heterointerfaces, and lattice lines extending from the top GaSb layer to the bottom InAs layer at the tunneling interface. Temperature dependent photoluminescence measurements demonstrated the optical quality of the multi-layer structure and strong optical signal at room temperature supports the structural analysis. The current–voltage characteristics of fabricated InAs/GaSb *p-i-n* tunnel diode measured at 77 K and 290 K demonstrated two transport mechanisms for different voltage ranges. Shockley–Read–Hall generation–recombination current at low bias and band-to-band tunneling transport at high bias confirmed the *p-i-n* tunnel diode characteristics of the InAs/GaSb heterojunction on GaAs. This elucidates the importance of the metamorphic InAs/GaSb tunnel diode structure heterogeneously integrated on silicon for implementation in low-voltage and high-performance tunnel field effect transistor applications.

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