An Energy-Efficient Tensile-Strained Ge/InGaAs TFET 7T SRAM Cell Architecture for Ultralow-Voltage Applications

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***Abstract*— In this paper, we benchmark the read/write performance and standby power of several static random access memory (SRAM) cell architectures utilizing 45-nm Si CMOS MOSFET and/or tensile-strained Ge/InGaAs tunnel FET (TFET) devices under low-voltage operation (0.2 V $\leq |V_{DD}| \leq$ 0.6 V). We then introduce a novel tensile-strained Ge/InGaAs TFET-based SRAM circuit using several access schemes and investigate the impact of cell access design on static and dynamic performance. SRAM cells utilizing outward access transistors exhibit wide read and write static noise margins, but suffer from increased read delay times. A 7T SRAM cell architecture is proposed in order to resolve the degraded read delay time. Cell standby energy was found to exhibit a strong dependence on operational voltage and Ge strain state. Variation of the Ge strain state from 1.5% to 3% resulted in an up to 98% reduction in cell standby energy ($|V_{DD}|$ = 0.6 V) as compared with similar CMOS-based SRAM cells. These results demonstrate the superior performance of the proposed 7T TFET SRAM design for operation in the low- and ultralow-voltage regime.**

***Index Terms*— Ge/InGaAs heterojunctions, static random access memory (SRAM), strained Ge, tunnel FETs (TFETs).**

I. Introduction

AGGRESSIVE transistor feature size scaling in order to maximize on-die functionality has had a significant detrimental impact on leakage-dominated OFF-state power dissipation. Although less severe, rising transistor counts have also corresponded to increased ON-state power consumption. In order to address these two limitations, the semiconductor industry has leveraged supply voltage (V_{DD}) scaling to realize quadratic and linear reductions in static and dynamic power dissipation, respectively. Moreover, whereas V_{DD} scaling seeks to reduce device-level power dissipation, additional improvements in chip-scale power consumption are realizable through circuit-level optimization. In particular, static random access memory (SRAM) provides a feasible platform for circuit-level optimization due to its wide-scale usage in microprocessor cache, occupying up to 70% of total die area. Accordingly, performance improvements in SRAM cell designs would correlate to considerable reductions in overall microprocessor power consumption. Recently, several circuit architectures have been proposed in order to maintain V_{DD} scaling from both the device and circuit perspective [1], [2]. However, an associated drawback to these approaches is the exponential increase in signal propagation delay. Current MOSFET designs, which rely on the thermionic injection of carriers in to the channel, exhibit reduced drive current (I_{ON}) and increased leakage current (I_{OFF}) at lower V_{DD}. This can also be observed as a limitation in MOSFET subthreshold slope (SS > 60 mV/decade) that ultimately restricts threshold voltage (V_{TH}) scaling. As a result, a tradeoff exists between the ability to operate in the subthreshold regime while simultaneously maintaining low-power dissipation.

In order to resolve these challenges, tunnel FETs (TFETs) have been suggested as an alternative to conventional MOSFETs for ultralow-voltage operation [3]–[9]. The intrinsic steep SS characteristics of TFET devices permit low voltage operation while reducing leakage-dominated power dissipation. Materials with narrow, direct bandgaps are viewed as promising candidates for the realization of TFETs. However, homogeneous device material systems can suffer from prohibitively low I_{ON} due to larger tunneling barrier heights (E_{beff}), thereby limiting their use in logic and memory applications [10]. Recently, tensile-strained Ge (ε-Ge)/InGaAs heterojunction TFETs have been reported [11], [12] to provide the low V_{TH} and SS properties of TFETs while maintaining high drive currents. In order to ascertain the feasibility of these devices for low-power circuit applications, we comprehensively investigate the design and evaluation of several SRAM configurations utilizing the ε-Ge/InGaAs TFET architecture.

II. Device Characteristics and SRAM Cells Design

A. Simulation Methodology

Fig. 1 outlines the simulation methodology used to investigate the performance of the proposed ε-Ge/InGaAs TFET SRAM architecture. Building on our previously reported results [11], this paper utilizes work function-tuning to realize a fixed OFF-state leakage current, I_{OFF}, of 100 pA/μ m at a $|V_{DS}|$ of 0.3 V. Due to the lack of a conventional TFET model

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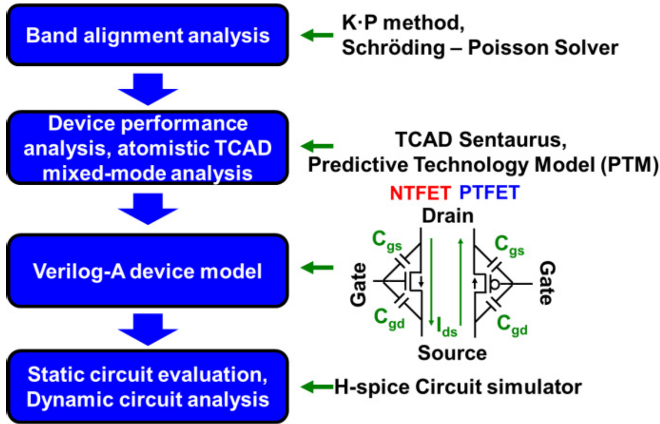

Fig. 1. Flowchart outlining the simulation methodology used in the design and modeling of the ε-Ge/In$_x$Ga$_{1-x}$As TFET-based memory circuit.

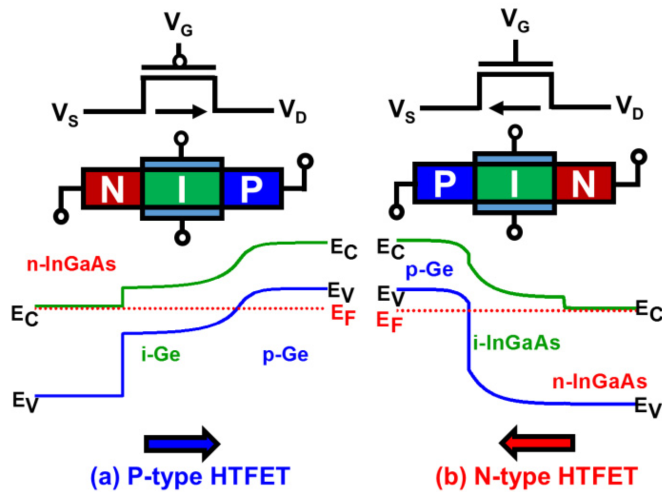

Fig. 2. Simulated band alignments and circuit representations. (a) p-type TFET (n-InGaAs/i-Ge/p-Ge). (b) n-type TFET (p-Ge/i-InGaAs/n-InGaAs).

for use in TCAD circuit-level simulation, we have implemented a Verilog-A device model as prescribed in [3]–[9]. The Verilog-A model used herein is comprised of three look-up tables tabulating I_{DS} (V_{GS} and V_{DS}), C_{gs} (V_{GS} and V_{DS}), and C_{gd} (V_{GS} and V_{DS}) characteristics of the ε-Ge/InGaAs TFET devices within the working bias range invested in this paper (*i.e.*, -0.6 V $< V_{\mathrm{DS}}$ and $V_{\mathrm{GS}} < 0.6$ V). Using this custom Verilog-A model, static and dynamic circuit analysis was then performed *via* HSpice circuit simulator.

B. TFET and MOSFET Operating Characteristics

In this paper, tunable tensile-strained Ge/In$_x$Ga$_{1-x}$As heterojunction TFETs (H-TFETs) were used to investigate the performance impact of strain state on SRAM operation in the sub-0.5 V supply voltage regime. Moreover, these results were benchmarked against matching Si CMOS-based SRAM cells (implemented using the 45-nm high-performance CMOS model provided by NIMO) in order to demonstrate the viability of the proposed SRAM design under continued supply voltage scaling [13]. Fig. 2 highlights the simulated p- and n-type TFET energy band diagrams, device structures,

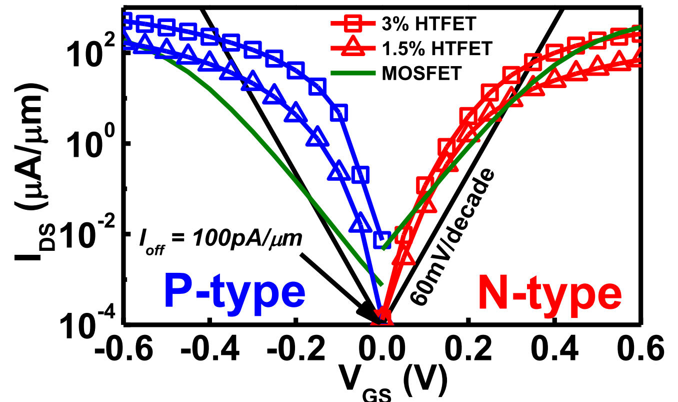

Fig. 3. $I_{\mathrm{ds}} - V_{\mathrm{GS}}$ characteristics ($|V_{\mathrm{DS}}| = 0.3$ V) for the p- and n-type ε-Ge/In$_x$Ga$_{1-x}$As H-TFETs using 1.5% and 3% ε-Ge strain states as compared with the MOSFET thermal limitation to SS and the 45-nm CMOS benchmark.

and circuit schematic symbols used in this paper. Correspondingly, Fig. 3 shows the $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ characteristics ($|V_{\mathrm{DS}}| = 0.3$ V) for the p- and n-type ε-Ge/In$_x$Ga$_{1-x}$As H-TFETs using 1.5% and 3% ε-Ge strain states. Also shown in Fig. 3 are the transfer characteristics for the 45-nm n and pMOSFETs as well as the thermionic emission limit to MOSFET SS, i.e., 60 mV/decade at 300 K. As previously discussed, the gate work function in the simulated ε-Ge/In$_x$Ga$_{1-x}$As H-TFETs was independently tuned in order to realize an I_{OFF} of 100 pA/μm for each strain configuration. Under these operating conditions, the ε-Ge/In$_x$Ga$_{1-x}$As H-TFETs exhibited a sub-60 mV/decade SS and enhanced drive current with respect to the benchmarked 45-nm n and pMOSFETs. Moreover, an increase in the ε-Ge/In$_x$Ga$_{1-x}$As H-TFET strain state (up to 3%) corresponded to an order of magnitude improvement in I_{ON}, thereby allowing the 3% strained H-TFETs to significantly outperform their MOSFET counterparts at a supply voltage of 0.3 V. Fig. 4 shows the $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristics for the p-type and n-type ε-Ge/InGaAs H-TFET at 1.5% strain (2%–3% $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ not shown here). One can find from Fig. 4 that both H-TFETs demonstrated unidirectional operation at reverse bias, which can be attributed to the asymmetric TFET device structure utilized in this paper. As a result, it is expected that 6T SRAM cell operation, which implicitly utilizes the bidirectionality of standard MOSFET access transistors, would be adversely affected by transitioning to a TFET-based design. Additionally, the n-type ε-Ge/In$_x$Ga$_{1-x}$As H-TFET displayed an increased reverse saturation current as compared with the p-type device. Whereas homojunction TFETs exhibit an approximately uniform E_{beff} at the source–channel and drain–channel junctions, H-TFETs, by nature, exhibit asymmetric source and drain tunneling barriers. As shown in Fig. 4 (inset), the asymmetries in E_{beff} and source/drain material bandgaps in H-TFETs can give rise to reverse bias conditions that result in enhanced reverse bias leakage current [11]. In this paper, at V_{DS} of -0.3 V and V_{GS} of 0.6 V, the simulated n-type ε-Ge/In$_x$Ga$_{1-x}$As H-TFET energy band diagram revealed an electron quasi-Fermi level that was above the hole quasi-Fermi level within the In$_x$Ga$_{1-x}$As channel. This, in conjunction with the availability of states in the source, directly resulted in the

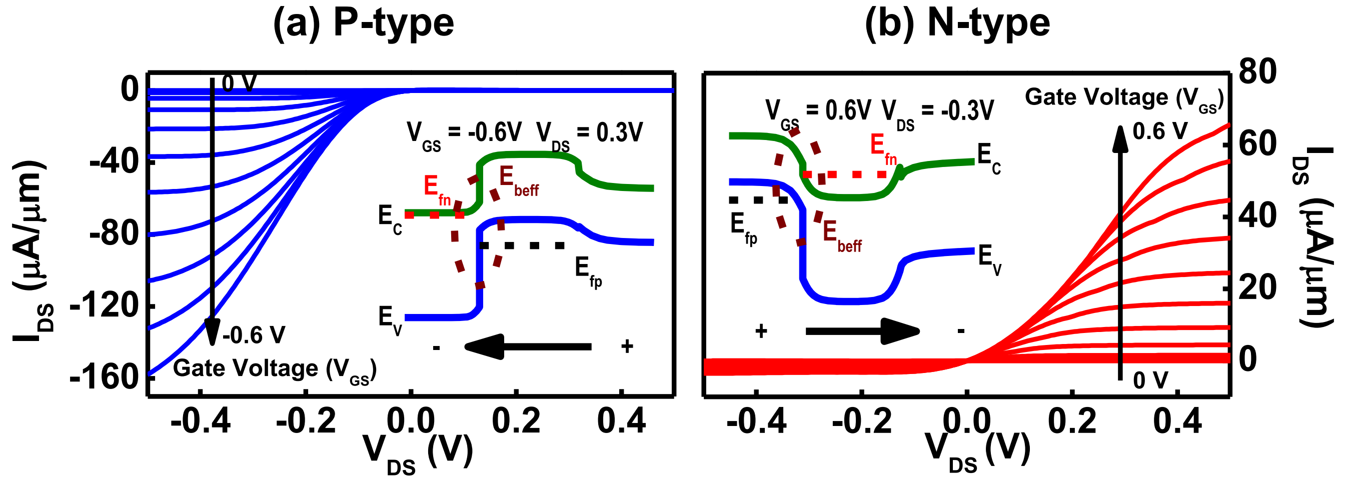

Fig. 4. $I_{DS} - V_{DS}$ characteristics for (a) p-type and (b) n-type ε-Ge/In$_x$Ga$_{1-x}$As H-TFETs at 1.5% strain. Both insets show corresponding band diagrams under positive gate bias and a reverse bias from drain to source ($|V_{DS}| = 0.3$ V and $|V_{GS}| = 0.6$ V).

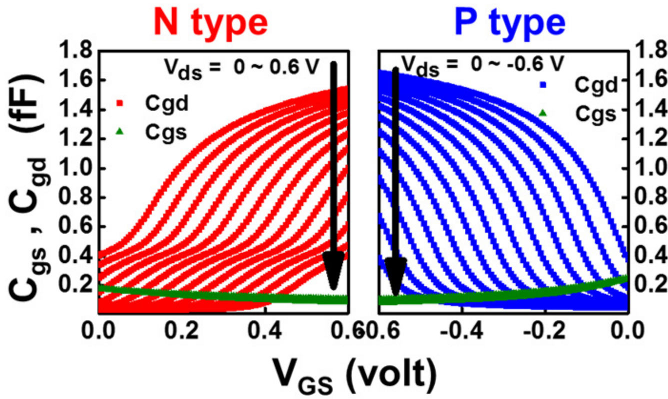

Fig. 5. Gate capacitances C_{gs} and C_{gd} as observed in the n and pTFETs at 1.5% strain as a function of gate voltage. C_{gd} was found to exhibit a strong dependence on gate voltage.

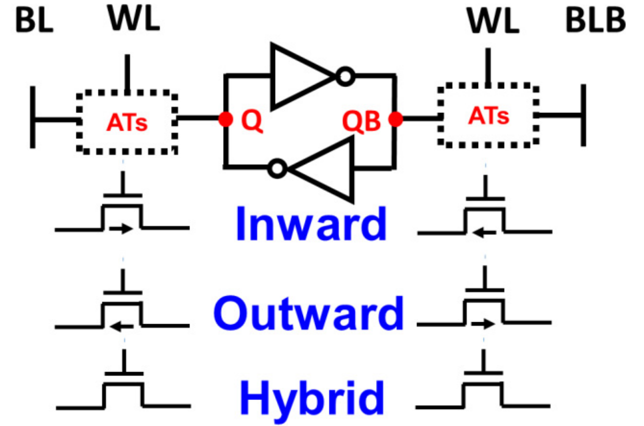

Fig. 6. Circuit schematic for the 6T SRAM cell and investigated access transistor configurations.

generation of a tunneling current between the drain and source, mirroring the negative differential resistance process in a tunnel diode structure. Moreover, the reduced source–channel E_{beff} (due to the nature of the H-TFET structure) resulted in an enhancement of the reverse tunneling probability, thereby increasing reverse bias leakage current as compared to a homojunction TFET device. Conversely, although the p-type ε-Ge/In$_x$Ga$_{1-x}$As H-TFET exhibited considerable hole accumulation in the channel, a lack of available states within the source prevented the generation of a reverse tunneling current, leading to stronger unidirectionality as compared to the n-type ε-Ge/In$_x$Ga$_{1-x}$As H-TFET.

The dependence of the ε-Ge/In$_x$Ga$_{1-x}$As H-TFET gate capacitance on gate bias was also investigated, as shown in Fig. 5. One can find from Fig. 5 that a large gate–drain (C_{gd}) capacitance was observed, which would lead to a substantial Miller capacitance during the complimentary operation of p- and n-type ε-Ge/In$_x$Ga$_{1-x}$As H-TFETs. The enhanced C_{gd} can be attributed to inversion layer formation occurring in close proximity to the drain, whereas a strong depletion region is formed at the source–channel interface, thereby resulting in lowered gate–source capacitance (C_{gs}).

C. SRAM Cell Design

In a standard 6T SRAM cell, two end-to-end inverters create the bistable latch circuit used to store a single bit. The read and write operations, as signaled by a complementary pair of bit lines (BL and BLB), are completed *via* two access transistors (ATs) controlled by a word line (WL). As a result, data retention can be significantly affected by the operational characteristics of the ATs, thereby impacting overall SRAM performance. Fig. 6 shows the possible 6T SRAM configurations utilizing MOSFETs and TFETs.

Due to the unidirectional nature of TFETs, the standard 6T SRAM cell becomes limited to two AT configurations, as denoted by the direction of current flow: 1) inward and 2) outward. In both configurations, the TFET unidirectionality enhances one operation (either read or write) while detrimentally affecting the other. Thus, by blocking either charging or discharging of the cell, the TFET unidirectionality results in a single-ended operation, which could hence lead to the inoperability of the SRAM cell. As an example, writing a "1" onto node Q ("0") of Fig. 6 while using the inward configuration is trivial as current can freely flow from BL to Q. On the other hand, performing the same operation

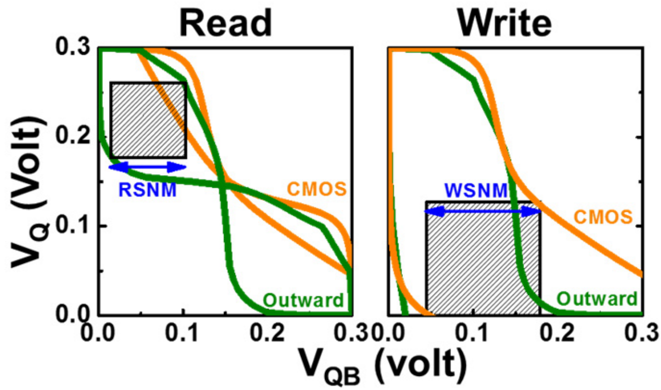

Fig. 7. Butterfly curves for MOSFET and outward TFET AT configurations under read and write operations. Black square: graphical definition of RSNM and WSNM.

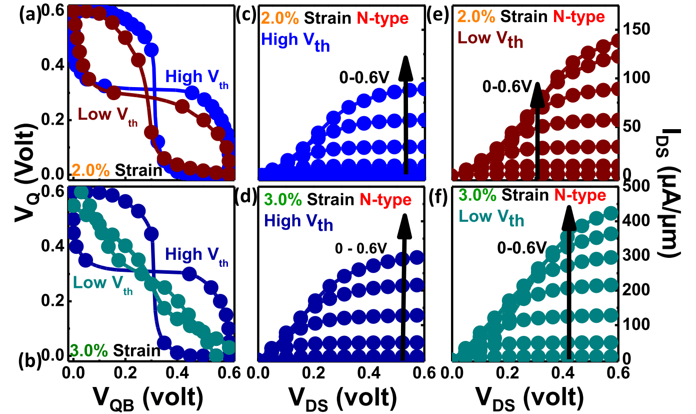

Fig. 8. Butterfly charts for different V_{TH} ε-Ge/InGaAs TFET-based SRAM cells during a read operation with (a) 2% and (b) 3% strain at $V_{DD} = 0.6$ V. $I_{DS} - V_{DS}$ plots for high V_{TH} and low V_{TH} n-type TFETs with (c) and (e) 2% strain, and (d) and (f) 3% strain.

utilizing outward ATs greatly restricts the charging of Q, thereby potentially resulting in a read-fail. Similar difficulties can be observed for access to node QB, leading to the conclusion that both inward and outward TFET accessing schemes exhibit single-ended access characteristics. To overcome this issue, several researchers have developed a "hybrid" design in which TFETs are used for bit storage whereas conventional MOSFETs are used for accessing the latch [3], [8]. Nevertheless, under ultralow supply voltage operation, the current mismatch between the two devices could inhibit SRAM performance, as will be discussed shortly.

D. Static Noise Margins—Read and Write Operations

An SRAM cell's static noise margin (SNM) during read or write operations serves as an important quantifiable metric in order to gauge the cell's robustness. The SNM is typically taken to be the maximum dc noise value for which the SRAM's stored data remains intact [14]. In order to visualize and evaluate both read SNM (RSNM) and write SNM (WSNM), respectively, butterfly curves were generated, as shown in Fig. 7. During a read operation, BL and BLB (Fig. 6) are charged to V_{DD}, thereby charging Q ("1") and discharging QB ("0"). To mimic this behavior, half-circuit voltage transfer characteristics for two inverters are generated. Analysis of the transfer characteristics results in a square of maximal area inscribed between each curve. The RSNM is then defined as the length of one side of the fit square. Similarly, during a write operation, BL is charged to V_{DD} while BLB remains grounded, thereby discharging Q ("0") and charging QB ("1"). Analysis of the half-circuit voltage transfer characteristics yields the WSNM.

E. Impact of Late Saturation on Noise Margins

Fig. 8 shows the butterfly chart for a read operation as a function of strain from 1.5% (not shown) to 3% and effective threshold voltage. From Fig. 8, one can observe that lower V_{TH} devices exhibit reduced RSNM, especially at higher strain levels. This is due to an increase in the drain current saturation delay for increasing strain [7]. Although higher strain and a lower V_{TH} can provide considerable drive current, the current in this case saturates at higher voltage, which further increases the transition region between the OFF- and ON-states and deteriorates the stability of read operations. This can be explained as follows. The voltage across a device is divided into two parts, i.e., the channel and junction resistances. Additionally, the high strain and low V_{TH} devices are flooded with carriers that have less channel resistance, thus a higher voltage drop is placed across the junction and enhanced tunneling current is observed. On the other hand, a larger voltage drop across the channel results in less voltage across the junction and a reduction in tunneling carrier generation. These results indicate that V_{TH} control remains a key issue affecting TFET device performance. In this paper, we have intentionally tuned the effective V_{TH} for all ε-Ge/In$_x$Ga$_{1-x}$As H-TFETs such that I_{OFF} is fixed at 100 pA/μm, thereby minimizing variability in our results due to saturation delay.

III. Result and Discussion

A. Static Read and Write Operations Using H-TFETs

Fig. 9 shows the RSNM and WSNM for different SRAM cell architectures operating at 0.3 and 0.6 V supply voltages. We note that 1.5% strained Ge/In$_x$Ga$_{1-x}$As H-TFETs were used in the TFET-based SRAM architectures. One can find from Fig. 9 that as the ratio between the cell access and inverter pull-down transistor widths increased (i.e., W_{AT}/W_{PD}), the RSNM was observed to decrease. This result was due to the sensitivity of the node voltage at Q (or QB) to the magnitude of the charging current provided by the ATs as well as the ability of the inverter pull down transistors to sink current. Consequently, a larger W_{AT}/W_{PD} ratio indicates an increased AT charging current wherein the inverter pull-down transistor cannot sink the excess current. As a result, charge accumulated at node Q (QB), resulting in a "flip" of the stored data. It can, therefore, be posited that the ability of the AT to source current has a significant impact on the stability of the SRAM cell. For the case of inward TFET ATs, the charging current magnitude is large in comparison to the other accessing schemes, resulting in a disturbance of the stored data. Similarly, for outward ATs, the unidirectionality of the TFETs under reverse bias served to further isolate the SRAM cell by inhibiting current flow

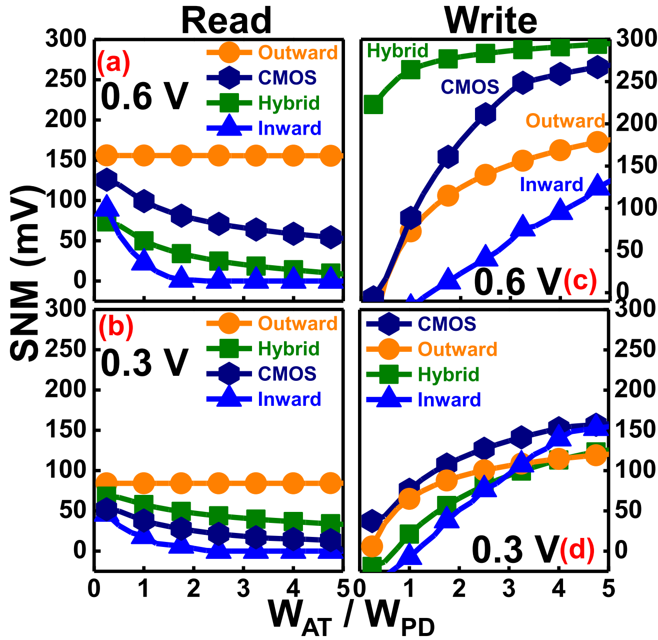

Fig. 9. (a) and (b) RSNM and (c) and (d) WSNM for different SRAM cell architectures operating at 0.6 and 0.6 V supply voltage, respectively, as a function of the access transistor (AT) and pull-down transistor (PD) width ratio.

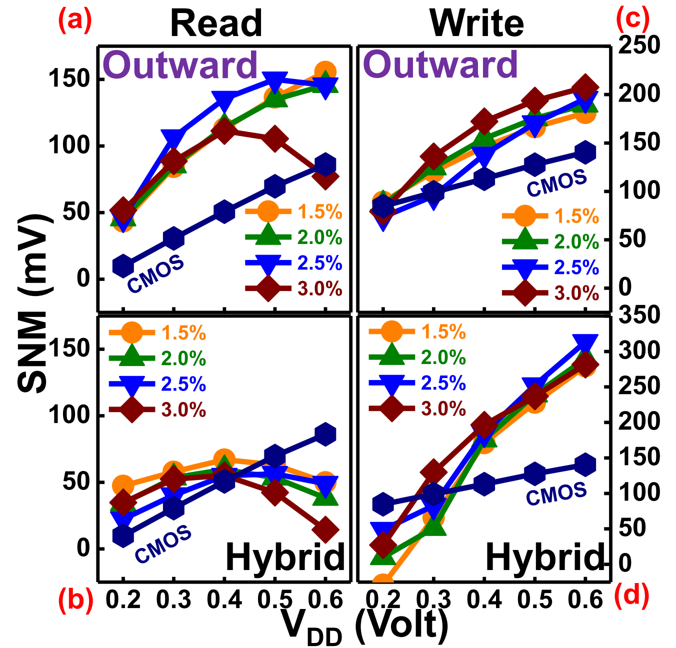

Fig. 10. RSNM and WSNM as a function of supply voltage under different ε-Ge strain states. Outward AT configurations exhibit superior RSNM and WSNM as compared with the MOSFET benchmark regardless of strain amount or supplied voltage. (a) and (b) RSNM and (c) and (d) WSNM with outward and hybrid AT as a function of supply voltage under different ε-Ge strain states.

to Q (QB). To circumvent these issues, the hybrid approach utilized bidirectional MOSFETs as ATs. As shown in Fig. 9, the hybrid SRAM cell design provided similar RSNM and WSNM performance to the standard High Performance CMOS SRAM cell. However, due to the ability of the inverter pull-down transistor (in this case a TFET) to sink additional current at 0.3 V as compared with a standard MOSFET, the hybrid SRAM cell design exhibited a larger RSNM under ultralow supply voltage operation.

Additionally, Fig. 9(c) and (d) shows the WSNM for the investigated SRAM cell architectures, again using supply voltages of 0.3 and 0.6 V and a ε-Ge strain state of 1.5%. Under these conditions, a trend opposite that observed for the RSNM was found. In this case, "flipping" the stored data necessitates that the BL (BLB) charging current magnitude be greater than the ability of the inverter pull-down transistors to sink current. Hence, an increase in the W_{AT}/W_{PD} ratio resulted in an increase in the observed WSNM. Moreover, as predicted, the inward and outward TFET AT schemes yielded single-ended write operability. This is in comparison to the hybrid and standard CMOS accessing schemes, which resulted in symmetric write operability. This can be explained as follows. For inward TFET ATs, only the AT at the grounded node (either Q or QB) is under forward bias. Likewise, for outward TFET ATs, only the AT at the high node (again, either Q or QB) is under forward bias. Correspondingly, unlike the standard CMOS or hybrid accessing schemes wherein operating on stored data occurs simultaneously through bidirectional MOSFET operation, the write process for TFET accessing schemes occurs *via* one AT and propagates through the remainder of the cell. As a result of this behavior, the WSNM is reduced for unidirectional TFET accessing schemes. Moreover, it was observed that nTFETs exhibited an enhanced ability to sink current as outward ATs, thereby corresponding to an increased WSNM over outward accessing schemes [3]. At V_{DD} of 0.6 V, the hybrid SRAM cell design was observed to leverage the enhanced drive current of the bidirectional MOSFETs and the strong latch behavior of the H-TFETs so as to deliver an enhanced WSNM. On the other hand, under a 0.3 V operating voltage, the hybrid accessing scheme suffered from degraded charging/discharging currents due to the subthreshold operation of the MOSFET ATs, resulting in a dramatically reduced WSNM. We, therefore, conclude that for 6T SRAM cell architectures, a tradeoff exists between the ability to read and write as a function of W_{AT}/W_{PD} as well as accessing scheme. Correspondingly, we have selected the outward and hybrid accessing schemes for further investigation due to the poor SNM observed under the inward AT scheme.

B. Effect of Strain on Static Noise Margins

In order to understand the impact of ε-Ge/In$_x$Ga$_{1-x}$As strain state on the observed SNMs, RSNM and WSNM as a function of supply voltage are plotted in Fig. 10 for each strain level and accessing scheme. Due to the poor performance of inward TFET ATs, as previously discussed, we hereon focus on the hybrid, outward, and standard MOSFET accessing schemes. As can be seen in Fig. 10(a) and (b), increasing the ε-Ge strain level has little effect until the strain state reaches 3%. This difference is even further suppressed under the hybrid SRAM cell design, as can be observed in Fig. 10(b). Regarding the hybrid accessing scheme, for operating voltages above 0.4 V, the MOSFET ATs provided higher drive currents than the constituent latch H-TFETs, thereby resulting in a limitation to the extracted RSNM due

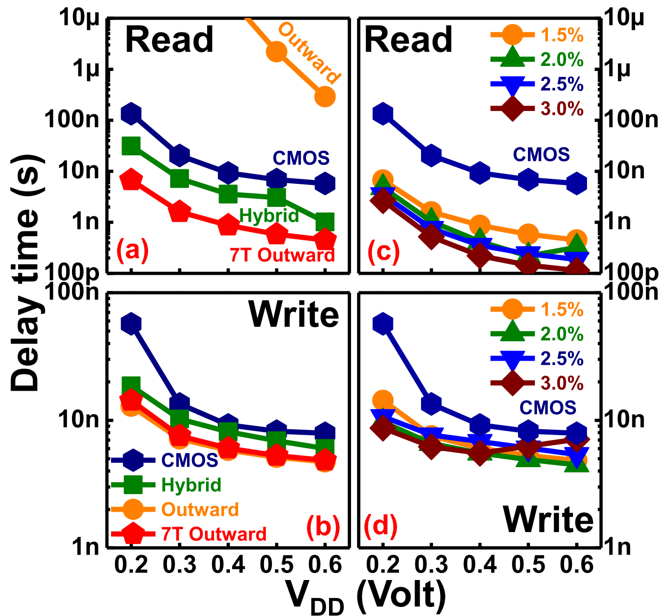

Fig. 11. (a) and (b) Delay times for different SRAM architectures as a function of applied voltage. (c) and (d) Delay times for the investigated strain levels of 7T H-TFET SRAM as a function of applied voltage.

to the H-TFET drive current. Conversely, for supply voltages below 0.4 V, the hybrid accessing scheme exhibited superior performance as compared with the standard CMOS SRAM cell. This result stems from the subthreshold operation of the MOSFETs, thereby leading to reduced MOSFET drive current in comparison to the H-TFETs. For the outward AT scheme, all strain levels demonstrated improved SNMs as compared with the 45-nm CMOS benchmark. However, the high strain (3%)-based SRAM cells exhibited a significant drop in RSNM as a result of intrinsic Negative Differential Resistance behavior, as discussed in Section II-B.

Fig. 10(c) and (d) shows the WSNM as a function of supply voltage for the investigated strain states and accessing schemes. Due to the large charging/discharging current observed under the outward TFET accessing scheme, the WSNM for the outward TFET AT SRAM cell was markedly larger than that of the CMOS benchmark. For supply voltages above 0.3 V, the hybrid accessing scheme also demonstrated improved WSNM performance as compared with the CMOS benchmark. However, for lower operational voltages, the subthreshold operation of the MOSFET ATs limited the overall WSNM of the hybrid accessing scheme. Correspondingly, the outward TFET accessing scheme provides the widest SNMs under both read and write conditions, outperforming the 45-nm CMOS benchmark up to 0.6 V supply voltage.

C. Dynamic Performance of 6T and 7T SRAM Cells

In this section, we investigate the dynamic performance of the previously discussed SRAM cell architectures. We note that the convention used hereon for the write and read delays is the times required for the storage node to charge to 90% V_{DD} or for ($V_{BLB} - V_{BL}$) to reach 10% V_{DD}, respectively. Moreover, a 20-fF capacitance was used to represent the line capacitance of metal interconnects.

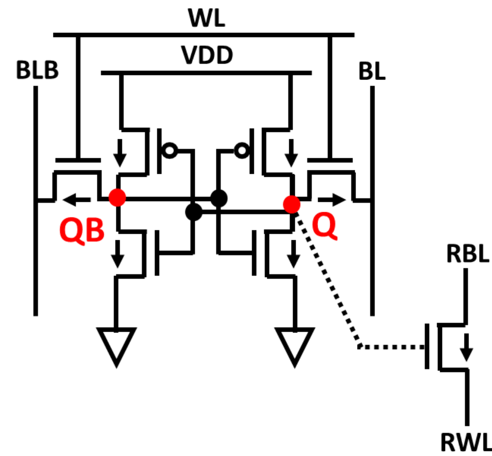

Fig. 12. Proposed 7T SRAM read-assisted architecture.

Fig. 11(a) shows the read delay times for the studied accessing schemes. The delay time for the outward TFET AT configuration was observed to be largest due to the unidirectional nature of the TFET and the resultant limitation to the cell discharging current. To resolve this issue, a 7T SRAM cell architecture, as reported by Lee *et al.* [8], is proposed. As can be seen in Fig. 12, this modified SRAM cell design incorporates an additional transistor with its gate connected to Q, its drain connected to the read bitline (RBL), and its source connected to the read word line (RWL). During a read operation, RWL becomes grounded and RBL is charged to V_{DD}. If data is stored at Q, RBL will be discharged to ground. By leveraging the unidirectional nature of TFETs, undesirable reverse leakage current can be suppressed. Moreover, the SRAM cell is allowed to stay in data retention mode during the read operation, thereby allowed for robust readability. Consequently, the proposed 7T H-TFET SRAM cell design exhibits a superior read delay as compared with the alternative cell architectures, as shown in Fig. 11(a) and (b).

Under write operation, the write delay time of the outward and 7T outward AT SRAM cell configurations were observed to significantly outperform the CMOS-based designs for supply voltages below 0.3 V. This was due to the subthreshold operation of the MOSFETs within this operating regime. Similarly, the proposed 7T SRAM cell design was found to display lower read and write delay times, with respect to the 45-nm CMOS benchmark, across all investigated strain states and operating voltages.

D. SRAM Energy Dissipation

Fig. 13 compares the SRAM cell standby power as a function of supply voltage for the 45-nm CMOS benchmark and the ε-Ge/In$_x$Ga$_{1-x}$As H-TFET cell designs. The standby power was found to reduce for decreasing operational voltages, as expected. Moreover, at V_{DD} of 0.6 V, the standby power of the 7T H-TFET SRAM cell was observed to be 52.7×, 47.6 ×, 20.7×, and 4.91× lower than the CMOS benchmark for the 1.5%, 2%, 2.5%, and 3% strain states, respectively. At a 0.2 V supply voltage, the difference in standby power

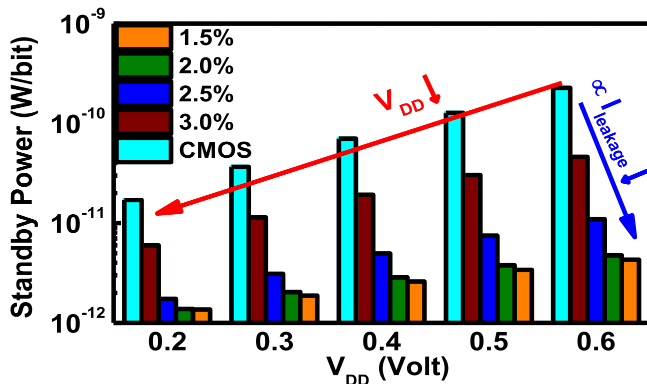

Fig. 13. SRAM cell standby power as a function of supply voltage for the 45-nm CMOS benchmark and the ε-Ge/In$_x$Ga$_{1-x}$As H-TFET cell designs. All configurations take advantage of supply voltage scaling to save power. 7T H-TFETs SRAM cells exhibit reduced standby power in comparison to the 45-nm MOSFET benchmark due to low H-TFET I_{OFF}.

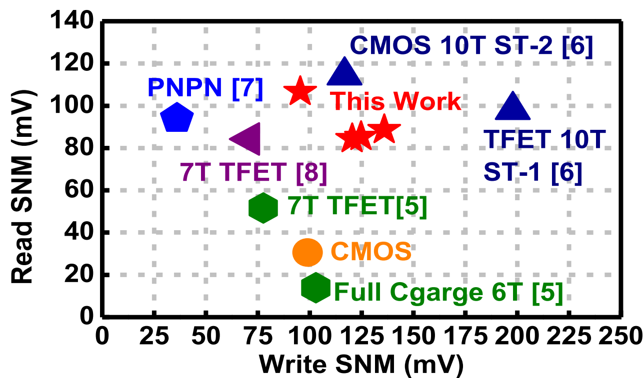

Fig. 14. RSNM and WSNM for the 7T H-TFET SRAM cell in comparison with previously published results at 0.3 V supplied voltage. Top-right corner is desirable region for high-performance SRAM cells.

was observed to decrease to 12.5×, 12.4×, 9.8 ×, and 2.86× for the 1.5%, 2.0%, 2.5%, and 3.0% strain states, respectively. Although higher strain H-TFETs provide some performance improvement, the 3% strained H-TFETs exhibit significant standby power consumption, thereby limiting their usage in the future ultralow-voltage applications. Moreover, 1.5%–2.0% strained H-TFETs are more easily realizable due to their larger critical layer thickness during growth, thus preserving a defect-free tunneling interface [12].

Additionally, Fig. 14 highlights the extracted RSNM and WSNM for the 7T H-TFET SRAM cell in comparison with previously published results. The proposed 7T H-TFET SRAM cell design was found to outperform the competing SRAM architectures utilizing seven or less transistors while approaching the performance of comparable 10T SRAM design. As can be seen in Fig. 14, the balance between cell area, RSNM, and WSNM achieved by our proposed 7T design suggests the feasibility of utilizing ε-Ge/In$_x$Ga$_{1-x}$As H-TFET-based SRAM cell architectures in order to improve performance and reduce power consumption for ultralow-power applications.

IV. Conclusion

A novel, tensile-strained Ge/InGaAs TFET-based SRAM architecture has been proposed, simulated, and evaluated for its static and dynamic performance. Different accessing schemes were investigated, revealing that outward access transistors provide successful read and write capability, but suffer from increased read delay times. Adoption of a 7T SRAM cell architecture resulted in a reduction in read delay time. The ε-Ge/InGaAs TFET-based 7T SRAM cell standby energy was observed to strongly depend on both operational voltage and the Ge strain level. Strain modulation between 1.5% and 3% revealed considerable reduction in cell standby energy when compared with similar, CMOS-based SRAM designs under ultralow voltage operation.

References

[1] M.-H. Tu *et al.*, "A single-ended disturb-free 9T subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1469–1482, Jun. 2012.

[2] Y. B. Kim, Y.-B. Kim, F. Lombardi, and Y. J. Lee, "A low power 8T SRAM cell design technique for CNFET," in *Proc. IEEE Int. SoC Design Conf. (ISOCC)*, Busan, South Korea, Nov. 2008, pp. 176–179.

[3] S. Strangio *et al.*, "Impact of TFET unidirectionality and ambipolarity on the performance of 6T SRAM cells," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 223–232, May 2015.

[4] X. Yang and K. Mohanram, "Robust 6T Si tunneling transistor SRAM design," in *Proc. Des. Autom. Test Eur.*, Mar. 2011, pp. 1–6.

[5] J. Singh, K. Ramakrishnan, S. Mookerjea, S. Datta, N. Vijaykrishnan, and D. Pradhan, "A novel Si-tunnel FET based SRAM design for ultra low-power 0.3 V VDD applications," in *Proc. ASP-DAC*, Jan. 2010, pp. 181–186.

[6] V. Saripalli, S. Datta, V. Narayanan, and J. P. Kulkarni, "Variation-tolerant ultra low-power heterojunction tunnel FET SRAM design," in *Proc. Symp. Nanosc. Archit.*, Jun. 2011, pp. 45–52.

[7] Y.-N. Chen, M.-L. Fan, V. P.-H. Hu, P. Su, and C.-T. Chuang, "Design and analysis of robust tunneling FET SRAM," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 1092–1098, Mar. 2013.

[8] Y. Lee *et al.*, "Low-power circuit analysis and design based on heterojunction tunneling transistors (HETTs)," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 9, pp. 1632–1643, Sep. 2013.

[9] U. E. Avci, R. Rios, K. Kuhn, and I. A. Young, "Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic," in *VLSI Symp. Tech. Dig.*, Jun. 2011, pp. 124–125.

[10] I. A. Young, U. E. Avci, and D. H. Morris, "Tunneling field effect transistors: Device and circuit considerations for energy efficient logic opportunities," in *IEDM Tech. Dig.*, Dec. 2015, pp. 22.1.1–22.1.4.

[11] J.-S. Liu, M. B. Clavel, and M. K. Hudait, "Performance evaluation of novel strain-engineered Ge-InGaAs heterojunction tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp. 3223–3228, Oct. 2015.

[12] M. Clavel, P. Goley, N. Jain, Y. Zhu, and M. K. Hudait, "Strain-engineered biaxial tensile epitaxial germanium for high-performance Ge/InGaAs tunnel field-effect transistors," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 184–193, May 2015.

[13] *Nanoscale Integration and Modeling (NIMO) Group: Predictive Technology Model (PTM)*, accessed on Apr. 25, 2016, [Online]. Available: http://ptm.asu.edu

[14] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 5, pp. 748–754, Oct. 1987.

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