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Growth, structural, and electrical properties of germanium-*on*-silicon heterostructure by molecular beam epitaxy

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The growth, morphological, and electrical properties of thin-film Ge grown by molecular beam epitaxy on Si using a two-step growth process were investigated. High-resolution x-ray diffraction analysis demonstrated ~0.10% tensile-strained Ge epilayer, owing to the thermal expansion coefficient mismatch between Ge and Si, and negligible epilayer lattice tilt. Micro-Raman spectroscopic analysis corroborated the strain-state of the Ge thin-film. Cross-sectional transmission electron microscopy revealed the formation of 90° Lomer dislocation network at Ge/Si heterointerface, suggesting the rapid and complete relaxation of Ge epilayer during growth. Atomic force micrographs exhibited smooth surface morphology with surface roughness < 2 nm. Temperature dependent Hall mobility measurements and the modelling thereof indicated that ionized impurity scattering limited carrier mobility in Ge layer. Capacitance- and conductance-voltage measurements were performed to determine the effect of epilayer dislocation density on interfacial defect states (D_{it}) and their energy distribution. Finally, extracted D_{it} values were benchmarked against published D_{it} data for Ge MOS devices, as a function of threading dislocation density within the Ge layer. The results obtained were comparable with Ge MOS devices integrated on Si *via* alternative buffer schemes. This comprehensive study of directly-grown epitaxial Ge-*on*-Si provides a pathway for the development of Ge-based electronic devices on Si.
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I. INTRODUCTION

Silicon (Si) integrated circuits have reached the juncture whereby their performance growth is unlikely to depend solely on geometrical scaling. Moving forward, it is widely accepted that new innovations such as novel device structures and materials integrated onto Si, are needed in order to boost transistor performance. Concurrently, germanium (Ge) has emerged as a strong candidate to maintain device performance at low operating voltages,[1] primarily owing to its superior carrier mobility and ease of integration into mainstream Si process flow. More recently, researchers have focused on the development of Ge-based electronic and optoelectronic devices, including: (i) Ge lasers on Si for on-chip integrated photonics;[2,3] (ii) high-speed and high-sensitivity Ge photoreceivers on Si[4,5] for optical data communication; (iii) Ge-based metal-oxide-semiconductor field-effect transistors (MOSFETs) for low-power logic;[6,7] (iv) Ge-based complementary-metal-oxide-semiconductor

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(CMOS) integrated circuits;[8] and (v) Ge-based quantum well fin field-effect transistors (FinFETs)[9–11] for next-generation high-speed, low-power logic applications. Thin epitaxial Ge layers have also been introduced as a buffer layer for developing GaAs solar cells on Si[12,13] and in hybrid IV/III-V multi-junction solar cell configurations.[14] Nevertheless, the potential of *Ge-on-Si* platform in augmenting the performance of future electronics has faced several challenges, most notably due to the need for lattice mismatched epitaxy as well as differences in thermal expansion coefficient between Ge and Si. Low temperature (LT) and high temperature (HT) two-step growth of Ge on Si substrates is a practical direct epitaxy technique frequently reported in recent years to realize smooth, high quality Ge films. Ge epilayers with dislocation densities down to the range of $\sim 10^7$ cm^{-2} have been reported using the LT/HT deposition approach with intermediate annealing steps such as thermal cyclic annealing,[15,16] H_2 annealing[17] etc. This work aims at studying a very thin (<150 nm) Ge film grown directly on Si using two-step growth process to evaluate and correlate the impact of its defect microstructure on electrical properties of the Ge layer.

In order to address the challenges of developing Ge devices on Si substrates, this paper investigates the viability of direct Ge-*on*-Si heteroepitaxy *via* solid source molecular beam epitaxy (MBE). By studying the carrier transport properties, oxide-semiconductor heterointerface characteristics, and structural defects inherent to the as-grown Ge thin-films, we aim to elucidate the impact of Ge epilayer defect morphology and structural properties on metal-oxide-semiconductor (MOS) device performance. As such, the strain relaxation properties of the Ge-*on*-Si heterostructure were investigated by triple axis x-ray diffraction and micro-Raman spectroscopy. Surface roughness, which affects carrier mobility by increasing surface scattering, was evaluated *via* atomic force microscopy (AFM). Cross-sectional and plan-view transmission electron microscopy (TEM) analysis was used to evaluate the structural and defect properties of the epitaxial Ge-*on*-Si heterostructures. To assess electrical quality of the Ge epilayer, Hall mobility measurements were performed as a function of temperature. The experimental mobility data were further corroborated *via* theoretical consideration of the scattering processes in Ge in order to isolate the dominant scattering processes limiting carrier mobility. Moreover, low- and room-temperature multi-frequency capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were performed in order to analyze the interfacial quality of the atomic layer deposited (ALD) Al_2O_3/Ge MOS interfaces. The extracted interface trap density (D_{it}) values were benchmarked against previously published Ge MOS D_{it} data as a function of film dislocation density. Obtained results highlight the viability of the Ge-*on*-Si direct integration path for next-generation energy efficient Ge transistors.

II. EXPERIMENTAL

Unintentionally doped 135 nm Ge thin-film was epitaxially grown on a (100) Si substrate (offcut 4° towards the <110> direction), using solid-source MBE utilizing separate Ge and III-V growth chambers connected *via* an ultra-high vacuum transfer chamber. The (100) Si substrate was loaded into the load lock of the Veeco Gen II MBE reactor after RCA cleaning. Silicon oxide desorption was performed inside the III-V growth chamber in the absence of arsenic overpressure at a substrate thermocouple temperature of ~ 960°C. The substrate was cooled to 150°C before it was transferred to the Ge growth chamber for subsequent Ge epitaxy. A two-step, low temperature/high temperature growth process incorporating several annealing stages was employed, which has been previously reported to achieve device-quality Ge films with low surface roughness, good crystalline quality and minimal intermixing between the Ge and Si layers.[12] The substrate thermocouple temperature during Ge growth was in the range of 250°C to 400°C. The low temperature growth initiation facilitates the preservation of a highly ordered, two-dimensional growth surface, whereas subsequent high temperature annealing phases provide additional thermal budget for the growing film to relax *via* dislocation annihilation and glide. Following Ge growth, the sample was gradually cooled down to prevent any thermal cracking prior to unloading for material characterization. The surface morphology of the as-grown Ge on Si thin-film was studied using a Bruker atomic force microscope in Scanasyst mode. In order to determine the structural quality and relaxation state of the Ge epilayer, reciprocal space maps (RSMs) were recorded using a PANalytical X'Pert Pro x-ray diffractometer

equipped with a Cu Kα-1 x-ray source. High resolution RSMs in both symmetric (004) and asymmetric (115) crystallographic orientations were recorded to measure the out-of-plane and in-plane lattice constants, respectively. Cross-sectional transmission electron microscopy (TEM) was used to characterize the Ge/Si heterointerface, whereas plan view TEM was used to estimate the threading dislocation density in the Ge film. The X-TEM and plan view TEM (PV-TEM) investigations were performed using a JEOL 2100 transmission electron microscope. For this purpose, electron transparent foils of thin-film cross-sections and wide-area sample surfaces were prepared *via* standard polishing techniques, i.e., mechanical grinding, dimpling and low-temperature Ar^+ ion beam milling.

Au/Ti (700 Å/500 Å) Ohmic contacts required for Hall mobility measurements were deposited on the Ge/Si heterostructure in a Kurt J. Lesker PVD 250 physical vapor deposition system. The four corner contacts were defined using positive photoresist and prebaked at ~85°C prior to the deposition of Au and Ti metals. The deposited contacts were annealed at 350°C for 5 minutes under forming gas (95% N_2:5% H_2 volume ratio). The carrier density and Hall mobility were measured as a function of temperature from 90 K to 315 K with a fixed magnetic field of 0.55 T using an Ecopia HMS5000 Hall measurement system. P-type MOS capacitors were also fabricated on the epitaxial Ge-*on*-Si heterostructure in order to investigate the Ge epilayer's interfacial and bulk trap densities. Fabrication of the devices began with a 60s degrease using acetone, isopropanol, and deionized (DI) water, followed by a 60s native oxide removal in dilute (1:10) hydrofluoric acid. A high-quality, native GeO_x interfacial passivating layer was then formed by thermal oxidation at 450°C for 10 minutes in an O_2 ambient. Immediately afterwards, a 4 nm Al_2O_3 gate oxide was deposited at 250°C using a Cambridge NanoTech ALD system with trimethylaluminum and DI water as precursors for Al and oxygen, respectively. The 250 nm Al gate electrodes and 250 nm Al Ohmic contacts were subsequently deposited using a Kurt J. Lesker PVD250 electron beam deposition chamber. Low-temperature and room temperature multi-frequency C-V and G-V measurements of the Ge MOS capacitors were performed using an HP4284A precision LCR meter with frequencies ranging from 100 Hz to 1 MHz. Accurate measurements were obtained with the removal of series resistance.

III. RESULTS AND DISCUSSION

A. Material characterization

Surface morphology is understood to play a key role in electronic, optoelectronic, and photovoltaic device applications due to the direct correlation between surface roughness and device properties (*e.g.*, surface scattering-induced mobility degradation, minority carrier surface recombination velocity, *etc.*). Correspondingly, the ability to accurately quantify material surface morphology *via* AFM provides a useful metric for the evaluation of growth and fabrication processes. In this work, the surface morphology and root-mean-square *(rms)* roughness of an MBE grown Ge-*on*-Si thin film was measured *via* AFM, as shown by the representative micrograph in Figure 1 (10 μm x 10 μm scan area). The *rms* roughness of the as-grown Ge epilayer was found to be less than 2 nm despite the 4% lattice mismatch between Ge and Si, suggesting that the low temperature Ge nucleation aids in maintaining a smooth, two-dimensional (2-D) surface reconstruction throughout the growth, with no visible island formation.

Micro-Raman spectroscopy was employed in order to determine the residual strain (if any) in the epitaxial Ge thin-film grown on Si. It is worth noting that the penetration depth of the optical excitation source is expected to be less than 20 nm[18] in Ge, thus the collected Raman spectra are representative of the Ge epilayer (~135 nm) and suitable for the subsequent strain-state analysis. Figure 2 compares representative Raman spectra acquired from the Ge thin-film grown on Si (in green) and an *n*-type (100)Ge substrate (in yellow), highlighting the fundamental unstrained Ge Raman line at 300.83 cm^{-1}. Additionally, the inset shows the fitted Raman spectrum for the Ge-*on*-Si epilayer, clearly identifying the experimentally observed Ge-*on*-Si peak position ($\omega_{Ge\text{-}on\text{-}Si}$ = 300.40 cm^{-1}) and its corresponding wavenumber shift with respect to the bulk Ge phonon mode. The in-plane biaxial strain in the Ge epilayer was estimated from the shift in phonon vibration mode ($\Delta\omega$) relative to bulk Ge, using the relation $\Delta\omega = -b\varepsilon_{//}$, where b is a material parameter

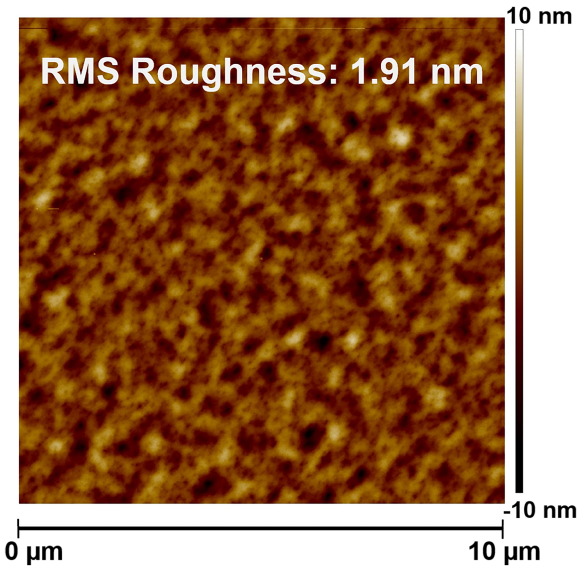

FIG. 1. AFM micrograph of the epitaxial Ge-*on*-Si heterostructure for 10 µm x 10 µm scan exhibiting rms surface roughness < 2 nm.

dependent on the material's phononic and elastic constants. Using the reported literature value of $b = 415$ cm^{-1} for Ge,[19] a tensile strain of $\varepsilon_{//} = 0.10\%$ was deduced in the Ge-*on*-Si epilayer for the observed Raman shift. Moreover, for single-crystal Ge, only one active phonon mode contributes to Raman scattering in the (001) back scattering measurement orientation. One can find from Figure 2 that a singular active phonon mode was indeed observed, whereas the low full width at half maxima (FWHM ~ 3.24 cm^{-1}) of the measured Ge-*on*-Si phonon mode suggests a highly ordered film.[20] In order to confirm the Raman-derived strain-state of the epitaxial Ge-*on*-Si film, high-resolution x-ray diffraction measurements were used to independently analyze the structural properties of the Ge epilayer.

The relaxation state of the Ge epilayer and its crystalline quality were investigated using symmetric (004) and asymmetric (115) RSM analysis, as shown in Figures 3a and 3b, respectively. As can be readily seen in the symmetric (004) RSM shown in Figure 3a, the Ge reciprocal lattice point (RLP) was found to be aligned (in Q_x) with the RLP of the Si substrate, indicating minimal lattice tilt within the Ge epilayer. Additionally, the in-plane and out-of-plane lattice constants for each material were calculated using the asymmetric (115) and symmetric (004) RSMs respectively, and methods outlined in literature.[21] Utilizing the experimentally derived lattice constants, the relaxation state of the Ge epilayer was determined with respect to the Si substrate, indicating that the

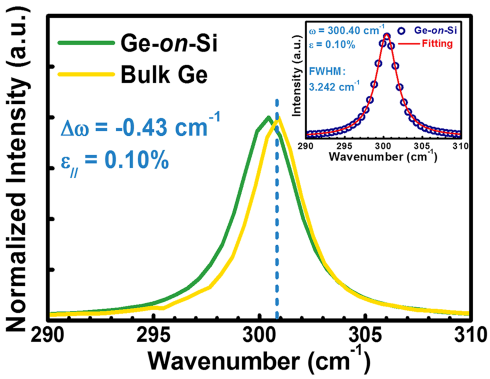

FIG. 2. Raman spectra of the 135 nm Ge-*on*-Si thin-film and a bulk Ge substrate. The shift in the FWHM centroid indicates a slightly tensile-strained Ge epilayer.

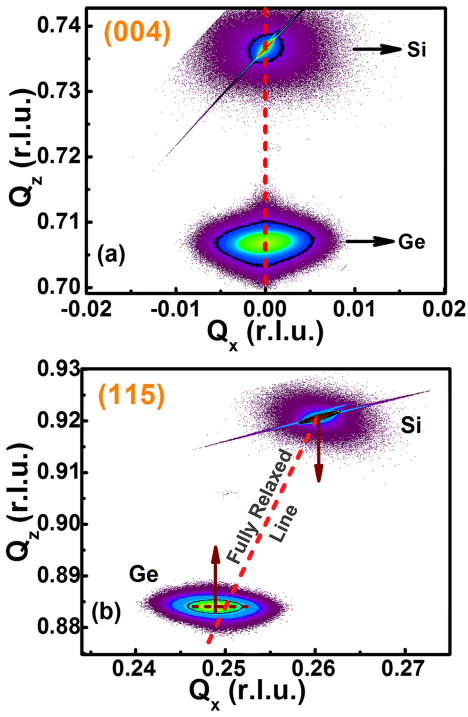

FIG. 3. (a) Symmetric (004) and (b) asymmetric (115) RSMs of Ge-*on*-Si. . No lattice tilt was observed, as shown by the alignment in Qx of the Ge and Si RLPs in the (004) RSM. The asymmetric (115) RSM indicates the presence of residual stress in the Ge epilayer.

as-grown Ge-*on*-Si thin-film was ~99% relaxed. Upon further inspection of the asymmetric (115) RSM (Figure 3b), the (115) Ge RLP was found to be distinctly shifted towards lower Q_x, deviating from the vector (pointing towards (000) in reciprocal space) indicative of full epilayer relaxation. These results suggest the presence of low levels of residual stress in the Ge epilayer, corroborating the Raman analysis discussed earlier. The observed tensile strain in the Ge epilayer can be linked to the thermal expansion coefficient mismatch between Ge and Si, resulting in residual epilayer strain following high temperature Ge-*on*-Si growth.[22] Finally, minimal Ge RLP mosaicity in both (004) and (115) RSMs further confirmed the crystalline quality of the Ge/Si heterostructure. Additional insight into the relaxation mechanisms at the Ge/Si heterointerface and the defect distribution within the Ge epilayer was provided by cross-sectional and plan-view TEM analysis.

Figure 4a shows a representative low-magnification TEM micrograph of the as-grown Ge/Si heterostructure, consisting of approximately 135 nm of unintentionally doped Ge epitaxially grown

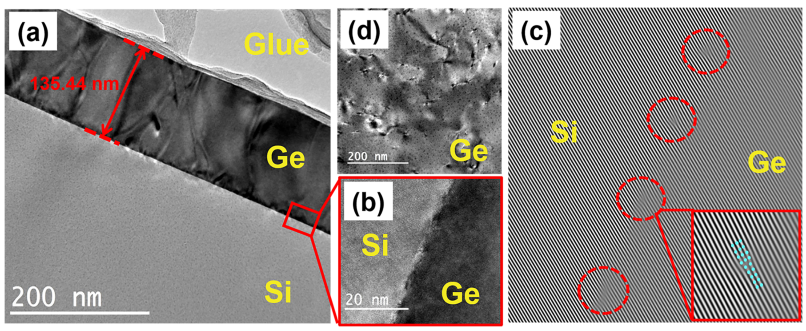

FIG. 4. (a) Cross sectional TEM micrograph of the Ge-*on*-Si heterostructure. (b) High-resolution TEM micrograph of the Ge/Si heterointerface revealing interfacial misfit dislocations, which upon further analysis were found to be 90° Lomer dislocations (c). (d) Plan view TEM micrograph highlighting threading dislocations present in the Ge epilayer.

on (100)/4° Si, whereas Figure 4b shows a high magnification TEM micrograph corresponding to the Ge/Si heterointerface. The abrupt and uniform nature of the Ge/Si interface suggests minimal atomic intermixing occurred during growth. Moreover, the low magnification TEM micrograph in Figure 4a shows limited propagation of defects from the heterointerface towards the Ge surface. Additionally, the recorded TEM micrographs revealed two distinct strain relaxation mechanisms: (i) a periodic array of 90° Lomer misfit dislocations (MDs) with separation varying from 5.8 nm to 12.1 nm, as clearly seen in Figure 4c; and (ii) a network of threading dislocations (TDs) visible from the plan-view TEM micrograph shown in Figure 4d. Atomistic modelling of Lomer dislocation arrays at the Ge/(001)Si heterointerface by Dornheim *et al*[23] showed that full relaxation of misfit strain in the [110] direction implies a separation of 9.6 nm between two Lomer dislocations. In such a compressively strained material system, wherein the Ge epilayer lattice constant (5.658 Å) is larger than the Si substrate lattice constant (5.431 Å), the MD is associated with an extra half-plane of atoms inserted within the substrate, as can be seen in the reconstructed HR-TEM image of the (111) planes shown in the bottom-right inset of Figure 4c. The MDs at the Ge/Si heterointerface allow for partial strain relaxation and are understood to aid in reducing threading dislocation propagation through the Ge layer. Moreover, the pure edge nature of 90° Lomer dislocations implies that they do not have a tilt component, as was corroborated by the (004) RSM shown in Figure 3a. Figure 4d shows a representative PV-TEM micrograph of the Ge/Si heterostructure, from which a threading dislocation density (TDD) of $\sim 10^{10}$ cm^{-2} was determined. It is important to note that PV-TEM captures a set of threading dislocations, each of which has a component of its line vector perpendicular to the image plane. These dislocations may bend out of the image plane prior to reaching out to the top surface, and therefore have little influence over carrier transport or inversion behavior close to the Ge surface, as discussed below. The effect of propagating defects on carrier transport is modelled, followed by an investigation into their electrical trapping characteristics, in subsequent sections.

B. Electrical transport properties and scattering processes

Carrier mobility, and its dependence on temperature, are key figures of merit for the direct integration of Ge-based electronics on Si. Correspondingly, in order to assess the electrical quality of the Ge-*on*-Si thin-film, temperature-dependent Hall mobility measurements were performed and analyzed to extract carrier mobility and carrier concentration. Subsequent theoretical treatment of the measured data was employed to model relevant scattering mechanisms and determine their influence on carrier transport. To this end, the carrier density (n) and mobility (μ_n) of an n-type semiconductor can be determined from the measured Hall coefficient ($R_H(B)$) and the resistivity ($\rho(B)$) using the relations:[24]

$$n = \frac{r_H}{qR_H(B)}, \tag{1}$$

$$\text{and} \quad \mu_n = \frac{1}{nq\rho(B)}, \tag{2}$$

where q is the electronic charge, B is the applied magnetic field, and r_H is the Hall factor. Figure 5 shows the measured μ_n and sheet carrier concentration (N_s) from 135 nm Ge layer as a function of temperature. The measured electron mobility was found to weakly depend on temperature, exhibiting decreases at both high and low temperatures. Such behavior has been previously observed in heavily doped semiconductors, due to the reduced contribution of lattice scattering component to carrier mobility.[25] Despite the absence of a dopant source during growth, a sheet carrier electron concentration of 5.46×10^{13} cm^{-2} (bulk concentration $\sim 4.0\times10^{18}$ cm^{-3}) was measured in the Ge epilayer. Moreover, the high free carrier density at low temperatures (<100 K) reveals the shallow nature of the donor-like impurities. The p-type Si substrate has a resistivity of 1 to 5 Ω-cm, and the *p-n* junction formed enables electrical isolation of the n-type Ge layer from the substrate in these measurements.

The experimental transport data was treated theoretically employing Boltzmann's transport equation to model epilayer carrier mobility as a function of scattering mechanism and measurement temperature. The relaxation time approximation allows linearization of the Boltzmann transport

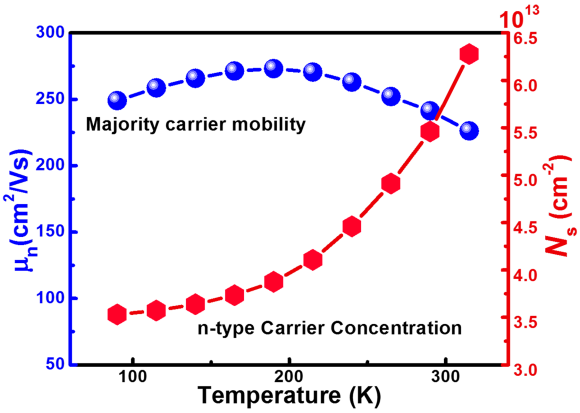

FIG. 5. Mobility and sheet carrier concentration of epitaxial thin 135 nm n-type Ge-*on*-Si.

equation:

$$\frac{df}{dt} = \left(-\dot{k}.\nabla_k f - \dot{r}.\nabla_r f\right) + \left.\frac{\partial f}{\partial t}\right|_c + \frac{\partial f}{\partial t}, \tag{3}$$

such that the collision term, $\left.\frac{\partial f}{\partial t}\right|_c$, can be expressed in terms of the ratio of the perturbed distribution function $(f - f_0)$ and the relaxation time $<\tau>$. This collision term represents the internal relaxation mechanisms, which correlate to the collision of charged carriers with different scattering sources in a semiconductor under the influence of external forces. Hence, the transport properties of a semiconductor depend strongly upon the types of scattering mechanisms involved in their carrier transport process.

In the following analysis, the dominant scattering mechanisms assumed to govern carrier transport in epitaxial Ge are: (i) acoustical phonon and optical phonon scatterings; (ii) ionized impurity scattering; (iii) neutral impurity scattering; and (iv) dislocation scattering. It should be noted that the calculated carrier mobility assumes the validity of Matthiessen's rule and that the total mobility can be obtained following the relaxation time approximation. The individual and total mobilities are thus given by:[26]

$$\mu_i = \frac{q < \tau_m >^i}{m^*} \tag{4}$$

$$\text{and} \quad \mu_{total}^{-1} = \sum\nolimits_i \mu_i^{-1}, \tag{5}$$

respectively, where $<\tau_m>^i$ is the average momentum relaxation time for the i-th scattering mechanism, given by

$$< \tau_m >^i = \frac{4}{3\sqrt{\pi}} \int_0^\infty \tau_m^i(z)\, z^{3/2} \exp(-z)\, dz, \tag{6}$$

where z is the electron energy in $k_B T$. The mobility expressions and material parameters associated with each scattering mechanism are reported in the supplementary material.

Figure 6 shows the calculated mobility as a function of temperature for various scattering processes following the procedures previously outlined. Scattering by ionized impurities is modelled upon the semi-classical solution for the long-range Coulomb field induced at an ionized impurity center in the lattice, developed by Conwell and Weisskopf.[27] The scattering potential due to a neutral shallow level impurity center is described by a square well potential which becomes a dominant scattering source for carriers at low temperatures.[28] Consequently, neutral impurity scattering mobility varies indirectly with temperature *via* the neutral impurity density, N_N. Lastly, the effect of dislocations on carrier mobility can be understood by the introduction of acceptor centers along a dislocation line, which capture electrons from the conduction band of the n-type Ge.[29,30] The resulting potential field around these charged dislocation lines scatter the conduction electrons and reduce electron mobility. The $T^{3/2}/\lambda$ dependence of the dislocation scattering mobility on temperature (T) and Debye screening length (λ) shows competition between a number of high thermal energy

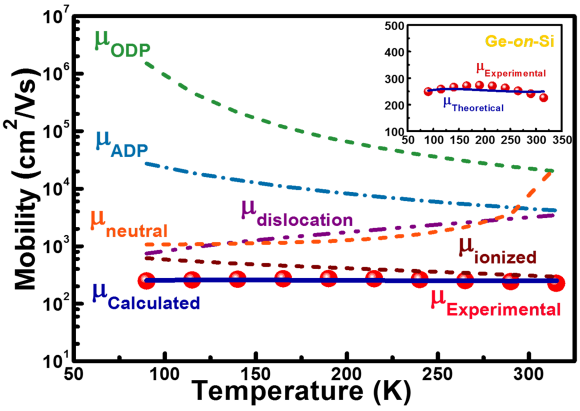

FIG. 6. Measured electron mobility of Ge-*on*-Si epilayer as a function of temperature along with the theoretical calculated mobility from individual scattering mechanisms. The calculated and measured mobilities show good agreement, as can be seen more clearly in the inset.

carriers and screening of the scatter source (charged dislocations). Fitting of the measured mobility data to this dislocation scattering model indicates a dislocation density of $7x10^9$ cm^{-2} influencing carrier mobility in the Ge-*on*-Si structure, slightly lower than the 10^{10} cm^{-2} TDD extracted from the PV-TEM micrograph shown in Figure 4d. The total calculated mobility compared to that measured *via* Hall shows comparable mobility values well within limits of error (<2.2% *rms* fit error); however, the model was found to overestimate electron mobility at higher temperatures (>300 K). One possible cause for the quantitative disagreement between the calculated and experimental curves in Figure 6 are additional scattering sources not accounted for by the proposed model, such as intervalley and electron-electron scattering. Additionally, the carrier mobility was found to be limited by ionized impurity scattering due to the high unintentional doping concentration ($\sim10^{18}$ cm^{-3}) in the Ge epilayer, particularly at higher temperatures. Neutral impurities and dislocations appear to limit electron mobility only at low temperature when there is less screening by ionized donors. Previous research revealed that ionized impurity scattering and acoustic deformation potential (ADP) scattering dominate Ge mobility;[31,32] however, due to the high density of impurities and the presence of dislocations in the Ge-*on*-Si structure, ADP no longer strongly influences the carrier mobility. Moreover, as compared to ionized impurity scattering, dislocations introduced into the Ge epilayer upon lattice-mismatched heteroepitaxy were found to have less of an impact on carrier mobility under the high substrate doping conditions.

C. MOS capacitor characteristics

It is generally understood that the oxide-semiconductor interface plays a critical role in determining the inversion characteristics of a metal-oxide-semiconductor (MOS) device. Consequently, MOS capacitors (MOSCAPs) have proven invaluable in providing insight into the quality of the oxide/semiconductor heterointerface as well as the bulk semiconductor material. By conducting C-V and G-V measurements on MOSCAP structures, standard metrics including flat-band voltage (V_{FB}), doping level (N_D or N_A), fixed oxide charge (N_{OT}), equivalent oxide thickness (EOT), effective work function (φ_{eff}), and interface trap density (D_{it}) can be extracted. Extraction of these parameters therefore allows for a quantitative assessment of the quality of the oxide/semiconductor interface.

To this end, p-MOSCAPs were fabricated on the epitaxial n-type Ge-*on*-Si structure utilizing an ALD Al_2O_3–based composite (Al_2O_3/GeO_x) high-κ gate stack. Specifically, the gate insulator is comprised of a thermally grown GeO_x interfacial passivating layer followed by an ALD Al_2O_3 high-κ layer. Figures 7 and 8 show a cross-sectional MOSCAP device schematic and the temperature-dependent C-V characteristics from a representative Ge *p*-MOSCAP, respectively. The C-V measurements demonstrate an increasing suppression of minority carrier- and/or D_{it}-induced inversion response for decreasing temperatures. A plausible reason for the persistence of low-frequency minority carrier inversion at 77 K are near-surface mid-gap traps in the depletion layer

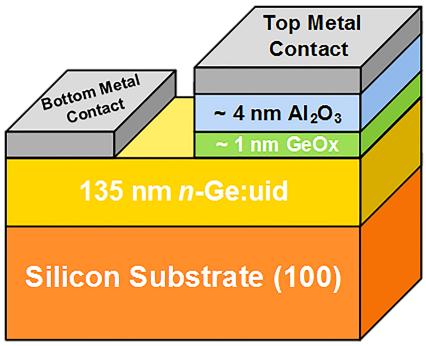

FIG. 7. Ge-*on*-Si MOS capacitor structure.

that create electron-hole (*e-h*) pairs and provide the necessary population of minority carriers (holes) to create an inversion layer at negative bias.[33] Alternatively, interface traps and fixed oxide charge could also mediate *e-h* pair generation or induce a permanent inversion layer, thereby providing a supply of minority carriers at low temperatures.[33,34] Equivalent oxide thickness (*EOT*) of ~ 3.47 nm was derived for the Al_2O_3/GeO_x gate stack at 292 K. A moderate V_{FB} shift (~ 0.28 V) was observed

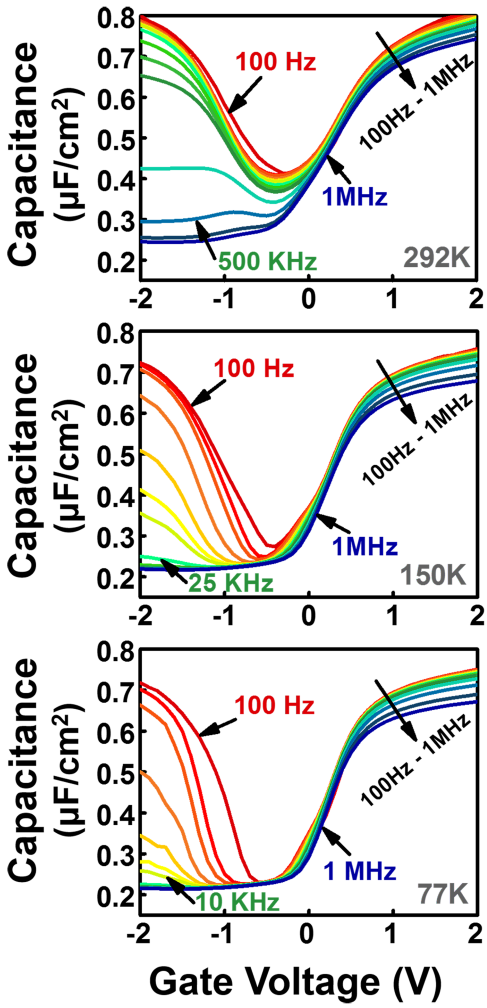

FIG. 8. Capacitance-voltage characteristics of a representative Ge-*on*-Si MOS capacitor measured from 292 K to 77 K as a function of frequency, indicating the frequency (in green) at which inversion response begins to appear in the device.

across all temperatures, which was attributed to the high unintentional doping in the Ge epilayer, as reported previously.[35] Limited interface states induce stretch out in the C-V curves, and a frequency dispersion of 2.8% per decade at 292 K was also observed. Additionally, high frequency C-V measurements taken at 292 K exhibited a signature of mid-gap interface trap response.

Trapped oxide charge density and hysteresis were also measured as a function of temperature, as shown in Figure 9. One can find from Figure 9 that the Ge MOSCAPs demonstrated a hysteresis of 323 meV at 292 K, which reduced to 250 meV at 250 K before increasing to 308 meV at 77 K (f = 100 kHz). The experimentally observed hysteresis was attributed to bulk oxide traps as opposed to insufficient dangling bond passivation at the oxide/Ge heterointerface.[36,37] From the measured C-V hysteresis, N_{ot} can be extracted using the Maserjian method, which takes into account carrier quantization in the accumulation regime:[38]

$$N_{ot} = \frac{\Delta V_{FB} C_{ox}}{q}. \tag{7}$$

Here, ΔV_{FB} is the shift in flat-band voltage and C_{ox} is the oxide capacitance per unit area.[38] The extracted N_{ot} values were found to parallel the C-V hysteresis behavior over the range of investigated temperatures, peaking at ~3×10^{12} cm^{-3}.

Figure 10 shows the conductance contours corresponding to G-V sweeps measured between 77 K and 292 K, qualitatively highlighting the Fermi level efficiency (FLE) of the fabricated Ge MOSCAPs. The Fermi level (FL) trace (dotted black line) at each measurement temperature follows the conductance peak under different frequency and bias conditions, and its slope demonstrates how efficiently the FL is biased throughout the bandgap. The magnitude of the conductance peak within the depletion region was found to reduce significantly at decreased temperatures, as indicated by the gradual constriction of the blue region in Figure 10. This indicates a reduction in D_{it}, which is directly proportional to the magnitude of conductance peaks, with decreasing temperature. FLE is quantitatively defined as the derivative of surface FL position E_f (V_G) or band bending at the semiconductor surface φ_s (V_G) with respect to gate bias V_G, and was calculated within the depletion region using the relation:[39]

$$FLE = \ln\frac{f_2}{f_1}\frac{kT/q}{V_1 - V_2}\,(\%), \tag{8}$$

where f_1 and f_2 are frequencies at which the G_p/ω conductance contours peak under gate bias V_1 and V_2, respectively, k is the Boltzmann constant, T is temperature, and q is the elementary charge. The frequency at which the conductance peak occurs can be associated with the trap energy within Ge bandgap, and consequently with FLE using the characteristic trapping time equation:[33]

$$\tau_n = \frac{1}{2\pi f} = \frac{\exp(\Delta E/kT)}{\sigma_n v_{th} N_c}, \tag{9}$$

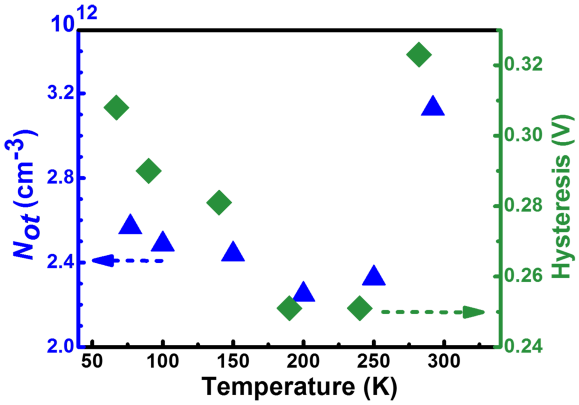

FIG. 9. Extracted trapped oxide charge density and corresponding hysteresis in a representative Ge-*on*-Si MOS capacitor as a function of measurement temperature.

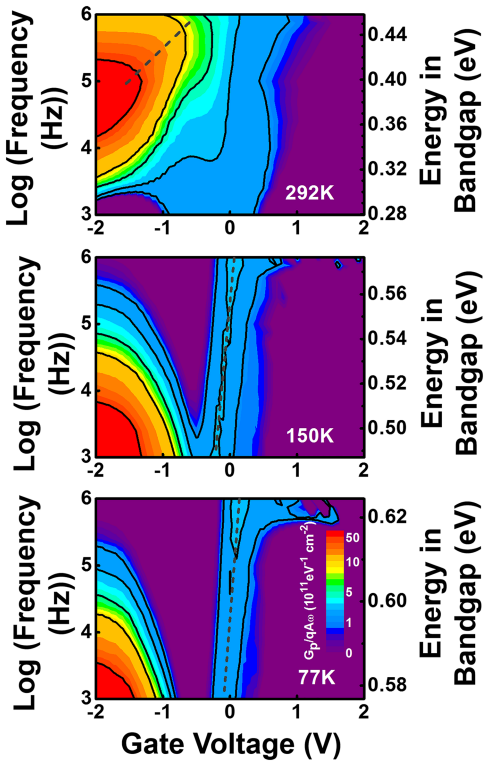

FIG. 10. Conductance contours of a representative Ge-*on*-Si MOS capacitor measured from 292 K to 77 K, indicating steeper fermi level trace at lower temperatures. All figures follow the scale shown in 77K plot.

where τ_n is the characteristic trapping time constant for electrons, f is the measurement frequency, σ_n is the trap state capture cross section, ΔE is the energy level of the trap state from the conduction band edge, v_{th} is the thermal velocity of electrons, N_c is the density of states in the conduction band of Ge, k is the Boltzmann's constant, and T is temperature. σ_n was assumed to be a constant value[40] of 10^{-16} cm^{-2} for Ge MOS capacitors.[41] By using the characteristic trapping time equation, FLE is plotted as a function of trap energy E_t away from midgap E_i, in Figure 11. A peak FLE of 32.7% was extracted about 0.17 eV away from the midgap (E_i) indicating good FL modulation with gate

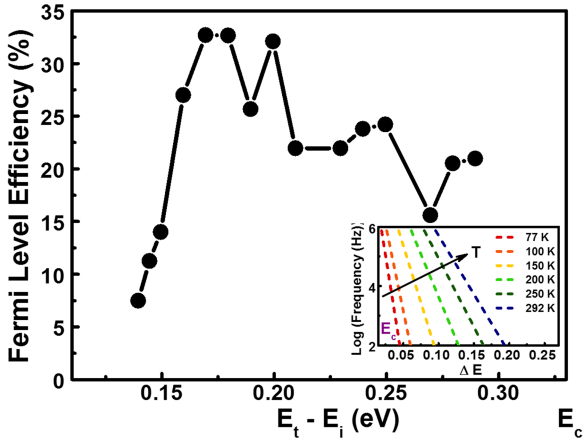

FIG. 11. *FLE* as a function of energy of the Ge-*on*-Si MOS capacitor showing a decline in FLE close to the midgap. Inset shows Ge bandgap energy ranges accessible at various measurement temperatures (77 K- 292 K) for frequencies from 100 Hz to 1 MHz.

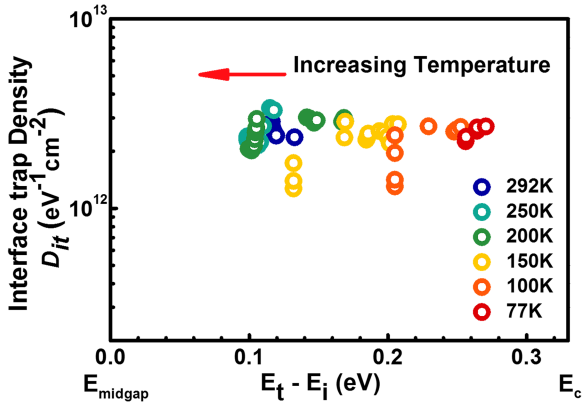

FIG. 12. Extracted D_{it} values at different temperatures plotted with trap energy level from midgap for Ge-*on*-Si MOS capacitor.

biasing (V_G), but declined sharply close to the midgap. This behavior indicates an increased density of interface states close to the mid bandgap region, which is corroborated later with the extracted D_{it} distribution. Conductance contours extracted from G-V measurements performed at temperatures ranging from 77 K to 292 K were utilized in the calculation of FLE, as each temperature allows the sampling of a limited region of the Ge bandgap, indicated in the inset of Figure 11. Figure 12 shows the extracted D_{it} as a function of energy within the bandgap for representative Ge MOSCAPs on Si. The variable temperature measurement scheme (292 K to 77 K) allows for a more accurate extraction of D_{it} due to the suppression of the weak inversion response observed in low bandgap materials. Additionally, the lower temperatures (and higher frequencies) allow for the extraction of D_{it} closer to the band edge. D_{it} was calculated using the conductance method (accounting for surface potential)[33,42] following:

$$D_{it} = \left(\frac{G_p}{\omega}\right)_{max} \left[f_D\left(\sigma_S\right) qA\right]^{-1}, \tag{10}$$

where $(G_p/\omega)_{max}$ is the maximum parallel conductance G_p normalized over angular frequency ω, q is the electric charge, $f_D(\sigma_s)$ is the universal function of standard deviation for band bending σ_s, and A is the capacitor area. For low bandgap materials, D_{it} values extracted from room temperature C-V measurements are overestimated due to the temperature-dependent supply of minority carriers to the inversion layer, which, in turn, contributes to higher conductance.[40,41] In this work, a peak D_{it} of 3.38x10^{12} cm^{-2} eV^{-1} was observed approximately 0.115 eV away from the midgap, E_i, whereas a minimum D_{it} of 1.3x10^{12} cm^{-2} eV^{-1} was observed approximately 0.13 eV away from E_i. We observe a denser distribution of interface states closer to the mid bandgap region, reflected by the lower FLE in this energy range discussed earlier. These obtained D_{it} values, an important parameter for transistor performance, are later benchmarked against previously published D_{it} values for various Ge MOS devices.

D. Benchmarking D_{it} as a function of dislocation density

Interface trap density, a key metric in MOS device performance, has been previously shown to have a direct correlation with *TDD*. Moreover, it has been reported that both D_{it} and *TDD* were directly reduced *via* high-temperature thermal cycle annealing.[16] Figure 13 shows a collection of room temperature D_{it} values measured for Ge MOS devices as a function of *TDD*, including the work reported herein. The previously published data use a variety of gate oxides and substrates, which could affect both the reported D_{it} and *TDD* values.[7,8,10,16,43–47] Hence, the device structure is indicated alongside each data point. An interesting pattern emerges for Ge devices on Si using different epitaxial integration schemes and an Al_2O_3/GeO_x gate stack: an almost linear increase in D_{it} with increasing *TDD*. Bulk Ge devices can be observed to benefit from the lowest D_{it} due to the absence of lattice mismatch-induced dislocations propagating through to the inversion surface. From Figure 13, a representative D_{it} value for Ge-*on*-Si MOSCAPs studied in this work can be found to

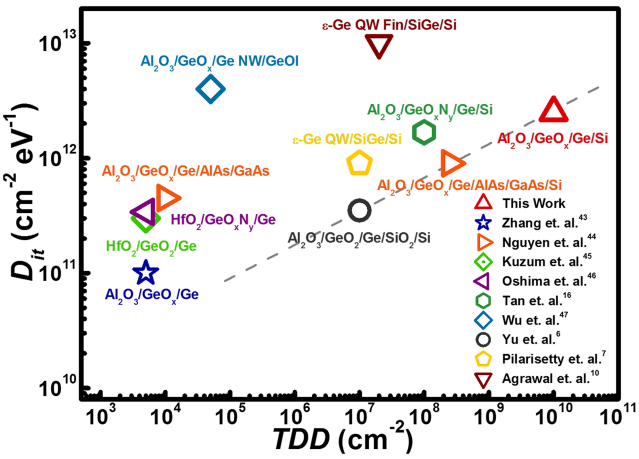

FIG. 13. Benchmarking of obtained D_{it} to that previously reported for various Ge MOS devices as a function of *TDD*.

be on par with that from other Ge devices integrated on Si *via* buffer techniques[7,10,44] or insulator layers.[47] Thus, the various electrical characteristics of Ge-*on*-Si MOS capacitors investigated here provides critical guidance in understanding the viability of high-mobility channel material directly integrated on Si, for low-voltage CMOS logic application.

IV. CONCLUSION

In summation, we have demonstrated high crystalline quality Ge thin-films directly grown on Si *via* MBE to realize cost-effective heterostructures for multifunctional (e.g., next-generation electronics, photonics, photovoltaics) device applications. The crystallinity, surface morphology, epitaxial Ge relaxation state, and optically excited photoemission were investigated in order to evaluate the material properties of the thin 135 nm Ge epilayer on Si. Atomic force microscopy revealed a smooth surface morphology and demonstrated a surface roughness of ~2 nm. Relaxation in the Ge epilayer was found to occur *via* defect formation as well as the formation of Lomer 90° misfit dislocations at the Ge/Si heterointerface. X-ray diffraction analysis confirmed the presence of residual tensile stress in the as-grown Ge epilayer, which was further corroborated by micro-Raman spectroscopy. The majority carrier mobility and density were measured as a function of temperature and modelled in accordance with different scattering mechanisms in Ge. Ionized impurity scattering was found to limit carrier mobility in the unintentionally doped *n*-type Ge layer. Further assessment of the epitaxial Ge-*on*-Si thin-film was made by analyzing the MOS behavior of fabricated *p*-MOS capacitors, yielding interface and oxide trap densities in the epitaxial Ge-*on*-Si MOS structure. A peak FLE of 32.7% was extracted between the midgap and conduction band edge in Ge, corresponding to the low D_{it} value of $1.3\text{x}10^{12}$ cm^{-2} eV^{-1}. Finally, the extracted D_{it} values were benchmarked against previously reported D_{it} data for Ge MOS devices as a function of threading dislocation density within the Ge layer. The D_{it} values obtained in this work were found to be comparable with other Ge MOS devices integrated on Si *via* alternative buffer schemes.

The results discussed in preceding sections highlight that the high density of dislocations (10^{10} cm^{-2}) in the Ge-*on*-Si heterostructure does not severely limit Ge epilayer properties such as surface roughness, carrier mobility, and FL modulation in fabricated Ge MOSCAPs. From the theoretical modelling of carrier mobility in Ge layer, we find that the density of electrically active dislocation lines scattering conduction electrons is smaller than the *TDD* value measured *via* PV TEM. This work further demonstrates that D_{it} in Ge MOS devices on Si is directly dependent on the defect microstructure of the Ge film, and increases linearly with increasing *TDD* value. Consequently, this comprehensive study of the structural and electrical properties of directly-grown epitaxial Ge-*on*-Si provides a pathway for the development of Ge-based electronic, optoelectronic, and photovoltaic devices on Si.

SUPPLEMENTARY MATERIAL

See supplementary material for the PL spectra obtained from Ge-*on*-Si heterostructure and a summary of mobility expressions and material parameters associated with the scattering mechanism modelling in *Section III B*, as taken from literature.

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