Investigating FinFET Sidewall Passivation Using Epitaxial (100)Ge and (110)Ge Metal–Oxide–Semiconductor Devices on AlAs/GaAs

Peter D. Nguyen, *Student Member, IEEE*, Michael B. Clavel, *Student Member, IEEE*, Jheng-Sin Liu, *Student Member, IEEE*, and Mantu K. Hudait, *Senior Member, IEEE*

***Abstract*— Device-quality crystallographically oriented epitaxial (100)Ge and (110)Ge were grown on GaAs substrates using a large bandgap AlAs buffer. Electrical characteristics of p-type metal–oxide–semiconductor (pMOS) capacitors, fabricated from the aforementioned material stacks, are presented for the first time. High-resolution cross-sectional transmission electron microscopy analysis demonstrated atomically abrupt heterointerfaces between Al_2O_3/Ge as well as Ge/AlAs for both (100) and (110) orientations. Various process conditions were implemented during MOS capacitor fabrication to study their impact on the Al_2O_3/Ge interface. The fabricated pMOS devices demonstrated excellent electrical characteristics with efficient modulation of the Fermi level from midgap to the conduction band edge, corresponding to a minimum D_{it} value of 1.2×10^{11} $cm^{-2}{\cdot}ev^{-1}$ on (100)Ge, indicative of a high-quality oxide/Ge heterointerface, and an effective electrical passivation of the Ge surface. Postdeposition annealing under O_2 was found to be less effective at reducing oxide trap density (N_{OT}) as compared to forming gas or O_2 postmetallization anneals (PMA), indicating that metal-induced bandgap states at the gate metal/dielectric interface have a notable impact on Ge pMOS N_{OT}. On the other hand, a tradeoff must be made between N_{OT} and the equivalent oxide thickness when performing PMA under O_2 or forming gas ambient.**

***Index Terms*— Epitaxy, germanium (Ge), III–V materials, metal–oxide–semiconductor (MOS) devices, orientation.**

I. Introduction

GERMANIUM (Ge) is an attractive candidate for low-power, high-speed electronics due to its 2× and 4× increase in electron and hole mobility, respectively, compared to those of silicon (Si) [1]. Numerous methods have been demonstrated to heterogeneously integrate Ge on to GaAs substrates [2]–[6], and thus aiding the eventual transfer of Ge on to Si substrates in order to streamline Ge into the standard Si CMOS process flow. However, carrier confinement remains an issue for Ge directly integrated on to GaAs due to the low valance band and conduction band offsets at the Ge/GaAs heterointerface. Recently, a novel method was demonstrated wherein epitaxial Ge was heterogeneously integrated on to AlAs/GaAs via molecular beam epitaxy (MBE) [7], [8]. High conduction and valance band offsets of ∼1 and ∼0.5 eV, due to the large bandgap (2.17 eV) AlAs buffer layer, aid in confining electrons and holes to the active Ge layer, thereby restricting carrier transport solely to Ge and preventing parallel conduction [9]. Moreover, in addition to improved carrier confinement, III–V buffers more closely match the thermal expansion coefficient of Ge, and are, therefore, less likely to suffer from defects generated by the relaxation of thermally induced mechanical stress, e.g., as compared to $Si_{1-x}Ge_x$ [10].

Simultaneously, the adoption of the FinFET architecture has resulted in enhanced gate control over channel electrostatics due to its multigate design [11]. Consequently, short-channel effects have been drastically mitigated, thereby allowing for continued transistor scaling. Thus, an attractive approach is to combine epitaxial Ge integrated on to AlAs/GaAs with FinFET technology, allowing for the exploitation of enhanced Ge hole mobility along <110> directions [1], [12], and hence the continued scaling of operating voltages below 0.5 V. In order to pursue Ge-based FinFET architectures, it is necessary to study the interfacial passivation of both (100) and (110) epitaxial Ge grown on AlAs/GaAs buffer layers, thereby mimicking the (110) sidewall and (100) top surfaces intrinsic to an FinFET device. Although investigations have been performed on the interfacial passivation of crystallographically oriented bulk Ge metal–oxide–semiconductor (MOS) capacitors [13], [14], no prior work exists on the study of interfacial passivation of crystallographically oriented epitaxial Ge MOS capacitors [15]–[19]. Moreover, it remains unclear as to whether postdeposition or postmetallization annealing is needed in order to obtain low interface-induced defects (D_{it}),

Manuscript received April 27, 2017; revised August 1, 2017; accepted September 18, 2017. Date of publication October 4, 2017; date of current version October 20, 2017. The work of P. D. Nguyen was supported by the NSF under Grant 478969. The work of M. B. Clavel, J.-S. Liu, and M. K. Hudait were supported by the National Science Foundation under Grant ECCS-1507950. The review of this paper was arranged by Editor J. C. S. Woo. *(Corresponding author: Mantu K. Hudait.)*

The authors are with the Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061 USA (e-mail: mantu@vt.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2017.2755460

low equivalent oxide thickness (EOT), and low oxide trap density (N_{OT}), all of which are essential for epitaxial Ge-based FinFET devices.

Therefore, this paper investigates the impact of crystallographic orientation on: 1) EOT scaling and 2) the passivation of interfacial defects and oxide charges at the oxide/Ge heterointerface for epitaxial (100)Ge and (110)Ge grown on GaAs substrates using a large bandgap AlAs buffer. Various annealing schemes were utilized to obtain a balance between EOT and the passivation of defects/charges, thereby yielding optimized (100) and (110) oxide/Ge heterointerfaces suitable for FinFET implementation. Temperature-dependent multifrequency capacitance–voltage (C–V) and conductance–voltage (G–V) measurements were used to analyze the electrical quality of the oxide/Ge heterointerface. Cross-sectional transmission electron microscopy (TEM) was used to investigate the structural quality of each oxide/Ge heterointerface. X-ray photoelectron spectroscopy (XPS) analysis was performed to determine the oxide composition of the thermally grown GeO_x for each orientation and relate the results with the measured electrical characteristics.

II. Experiment

Two lattice-matched heterostructures, consisting of (100)Ge and (110)Ge on AlAs buffers, were grown on GaAs substrates by solid-source MBE. A 250-nm GaAs buffer layer was first grown on the (100)GaAs (offcut 6° toward the [110] direction) and (110)GaAs substrates at a growth temperature of 650 °C, and a growth rate of 0.5 μm/hr. Following GaAs homoepitaxy, a 170-nm AlAs layer was grown at 670 °C. Upon completion of the composite buffer growth within the III–V chamber, the sample was cooled down and transferred to the Ge growth chamber via an ultra-high vacuum transfer chamber. The unintentionally doped (uid) 270-nm Ge layer growth was performed at 400 °C using a low growth rate of 0.067 Å/s. Full details of the growth process are reported elsewhere [7], [8].

High-resolution TEM (HR-TEM) was performed in order to characterize the oxide/Ge and Ge/AlAs/GaAs heterointerfaces. The composition of thermally grown GeO_x on (100)Ge and (110)Ge was investigated using XPS. Additionally, Hall measurements employing the van der Pauw geometry were performed on (100)Ge and (110)Ge samples, revealing a $\sim 2 \times 10^{18}$ cm^{-3} uid concentration exhibiting electron-like conduction.

pMOS capacitors were fabricated on the epitaxial (100)Ge and (110)Ge material stacks following identical fabrication processes. After a standard degrease and removal of native oxide using dilute (1:10) hydrofluoric acid, a high-quality native GeO_x passivating layer was formed by thermal oxidation at 450 °C for 40 min in an ultrahigh purity oxygen (O_2) ambient. Immediately afterward, a 4-nm Al_2O_3 gate oxide was deposited at 250 °C using atomic layer deposition from trimethylaluminum and DI H_2O. The 0.8-nm TiN/100-nm Al gate electrodes and 0.8-nm TiN/100-nm Al/10-nm Ti/30-nm Ni ohmic contacts were subsequently deposited using electron beam deposition. Temperature- and multifrequency-dependent C–V and G–V measurements of the fabricated Ge MOS capacitors were performed on an ARS cryogenic probe station using a HP4284A precision LCR meter with frequencies ranging from 1 kHz to 1 MHz. Following initial electrical characterization, the fabricated devices were subjected to postmetallization annealing under an O_2 or forming gas (N_2:H_2, 95%:5%) ambient. An alternative device lot underwent postdeposition annealing in an O_2 ambient prior to gate metal evaporation, as opposed to postmetallization annealing. Table I summarizes the annealing schemes investigated in this paper.

TABLE I
Process Conditions Used to Investigate the Impact of Annealing on Ge MOS Behavior

Annealing Scheme	Annealing Temperature (°C)	Annealing Time (min)	Annealing Ambient
PDA	405	30	O_2
PMA	405	30	O_2
FGA	300	2	N_2:H_2 (95%:5%)

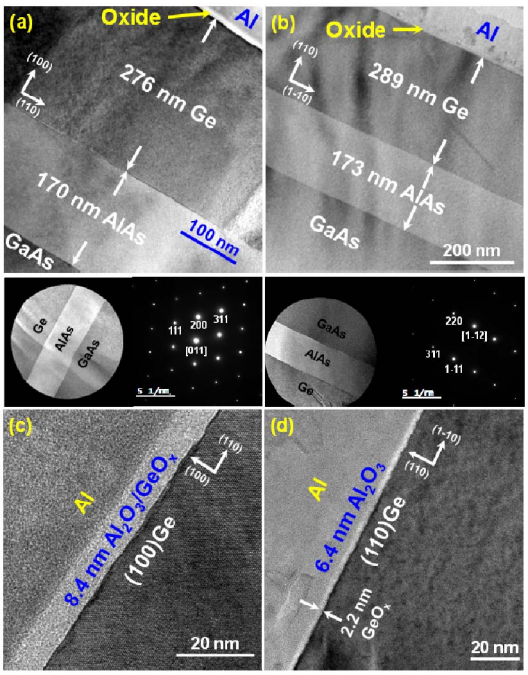

Fig. 1. Cross-sectional TEM micrographs of (a) Al/Al_2O_3/GeO_x/(100)Ge/AlAs/GaAs and (b) Al/ Al_2O_3/GeO_x/(110)Ge/AlAs/GaAs and their associated SAED patterns. HR-TEM micrographs of the heterointerfaces for (c) Al/Al_2O_3/GeO_x/(100)Ge and (d) Al/Al_2O_3/GeO_x/(110)Ge.

III. Results and Discussion

A. TEM Analysis of Al/Al_2O_3/GeO_x/(100)Ge and (110)Ge/AlAs/GaAs Material Stacks

Fig. 1(a) and (b) shows the cross-sectional TEM micrographs and selective-area electron diffraction (SAED) patterns of each heterostructure, respectively. Similarly, Fig. 1(c) and (d) shows the HR-TEM micrographs of the Al/Al_2O_3/GeO_x/(100)Ge and Al/Al_2O_3/GeO_x/(110)Ge MOS interfaces, respectively. Sharp heterointerfaces between Ge/AlAs and AlAs/GaAs were observed, which is essential for

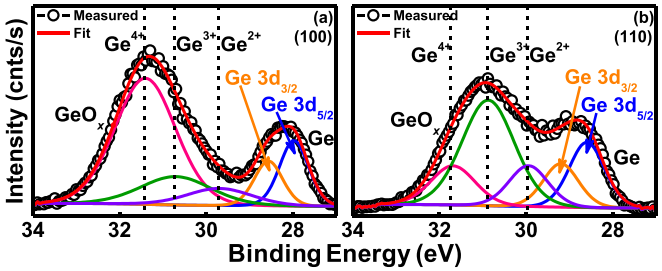

Fig. 2. XPS analysis of the oxygen composition of GeO_x thermally grown on (a) (100) epitaxial Ge and (b) (110) epitaxial Ge surfaces.

the minimization of interface scattering in thin Ge active layers, wherein charge transport occurs within close proximity of the Ge/AlAs heterointerface. Likewise, the SAED pattern from each heterostructure confirms the quasi-lattice-matched nature of the investigated heterostructures. The relative uniformity and abrupt nature of the Al_2O_3/GeO_x/(100)Ge and (110)Ge heterointerfaces is clearly visible in the HR-TEM micrographs shown in Fig. 1(c) and (d), respectively. The observed uniformity at the interface between the 6.4 nm/2 ~2.2 nm amorphous Al_2O_3/GeO_x composite gate oxide and each Ge layer is expected to aid in the reduction of surface scattering due to interfacial roughness or a nonuniform native oxide regrowth. Correspondingly, the qualitatively distinct GeO_x uniformity [Fig. 1(d)] suggests a coherent native oxide regrowth, which could indicate a high degree of dangling bond (DB) passivation and would be observed electrically as a reduction in interfacial D_{it}. Additional native oxide compositional analysis, e.g., via XPS, can provide further insight into the quality and consistency of the native oxide interfacial passivation scheme.

B. XPS Analysis of Interfacial GeO_x Composition

In order to study the as-grown GeO_x composition, XPS measurements were performed on epitaxial (100)Ge and (110)Ge surfaces oxidized at 450 °C prior to annealing. Fig. 2(a) and (b) shows the representative XPS spectra for the Ge 3d orbital from each (100)Ge and (110)Ge surface, respectively, where the curves corresponding to Ge^{4+}, Ge^{3+}, Ge^{2+}, Ge $3d_{3/2}$, and Ge $3d_{5/2}$ were determined by fitting (shown in red) against the measured envelope spectra (shown in black). As shown in Fig. 2(a), the Ge^{4+} peak was found to dominate the (100)Ge surface, whereas the GeO_x suboxide peaks exhibited substantially lower intensity. These results indicate that GeO_x thermally grown on epitaxial (100)Ge surfaces predominantly consists of stoichiometric GeO_2. Conversely, for the (110)Ge surface shown in Fig. 2(b), the Ge^{3+} peak dominated the measured spectra, resulting in an increased convolution of the O–Ge and Ge–Ge related spectral features. Consequently, the resultant (110)Ge native oxide composition was found to be predominately $Ge_2O_3^-$, which is in stark contrast to the as-grown GeO_x composition on epitaxial (100)Ge surfaces. These results differ from the bulk Ge case, where thermally grown GeO_x was found to be predominately composed of GeO_2 irrespective of surface orientation [13]. In the following section, we will investigate the impact of these thermally grown oxide layers on the fabricated MOS C–V characteristics and account for the discrepancies in oxide composition.

C. MOS Capacitor C–V and Conductance Characteristics of Al/Al_2O_3/GeO_x/(100)Ge Gate Stacks

Fig. 3 shows the C–V characteristics of the (100)Ge MOS-Cs, including as-deposited, O_2 postdeposition anneal (O_2 PDA), O_2 postmetallization anneal (O_2 PMA), and forming gas postmetallization anneal (FGA), measured at temperatures ranging from 78 to 300 K. The C–V curves shown in Fig. 3 were measured at 78 and 300 K (other experimental results not shown) in order to demonstrate the suppression of the minority carrier-related weak inversion response as a function of decreasing temperature [8], [20], [21]. C_{max} decreased for all annealing schemes investigated, as shown in Fig. 3(c)–(h), thereby indicating an increase in EOT with annealing due to the formation of additional interfacial GeO_x. Furthermore, we note that EOT significantly increased with O_2 PMA, as compared to the alternative annealing schemes, due to the additional oxidation of the Al gate metal at the gate metal/dielectric interface. For the as-deposited case, there was a small frequency dispersion kink in the depletion regime, which was apparent even at low temperatures (i.e., 78 and 150 K). The temperature independence of this feature suggests that it was not due to the weak inversion response from minority carriers [20], but rather N_{OT}- and/or D_{it}-related charge trapping. Moreover, this kink was not suppressed with O_2 PDA, as shown in Fig. 3(c). Conversely, the observed midgap trap response was found to be better suppressed using FGA, as shown in Fig. 3(e), although it remained marginally apparent at 78 K. Under O_2 PMA, the kink was completely suppressed, demonstrating effective passivation of the associated charge-trapping center. Due to the temperature independence of this feature and its suppression only following postmetallization forming gas or O_2 annealing, it can be attributed to the formation of metal-induced bandgap states (MIGS) introduced via metal wave function decay into the oxide bandgap or a disordered interfacial microstructure at the gate metal/oxide interface [22]–[24]. Lastly, unlike the cases for FGA and O_2 PMA, a low-frequency inversion-like response persisted at 78 K under the O_2 PDA scheme, suggesting that traps with quick response times remain uncompensated when using the O_2 PDA process.

Fig. 4 shows the G_p/ω contours of the (100)Ge MOS-Cs, wherein the contour intensity follows the scale indicated in Fig. 4(h). The G_p/ω contours shown were extracted from measurements taken at 78 and 300 K in order to separate the contribution of minority carrier conduction [8], [20], [21] from the Fermi-level tracing, thereby yielding a more accurate representation of the devices' Fermi-level efficiencies (FLEs). Significant broadening of the contours was observed at 78 and 300 K for the as-deposited and O_2 PDA cases. In fact, this broadening worsened for the O_2 PDA case at 78 K, wherein the low intensity conductance region (blue) increases in width across voltage bias. This broadening suggests increased charge trapping due to a large presence of D_{it} at the GeO_x/(100)Ge interface resulting from insufficient DB passivation and/or

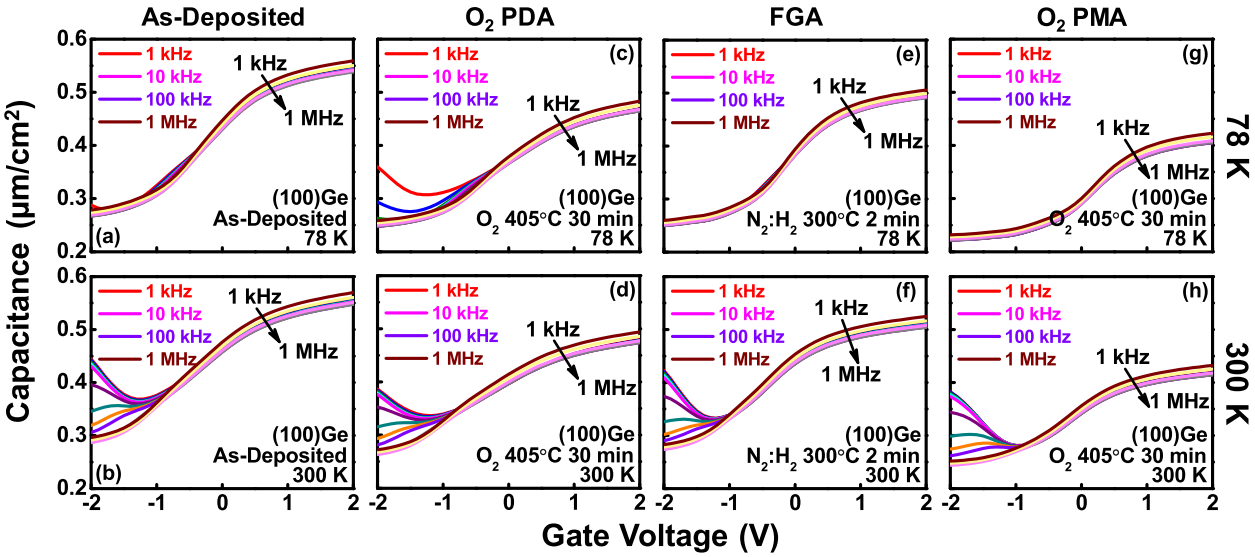

Fig. 3. *C–V* characteristics of the (100)Ge MOS-C on GaAs via an AlAs buffer architecture, where (a) and (b) *C–V* curves measured at 78 and 300 K for the as-deposited case, (c) and (d) *C–V* curves measured at 78 and 300 K for the O_2 PDA case, (e) and (f) *C–V* curves measured at 78 and 300 K for the FGA case, and (g) and (h) *C–V* curves measured at 78 and 300 K for the O_2 PMA case.

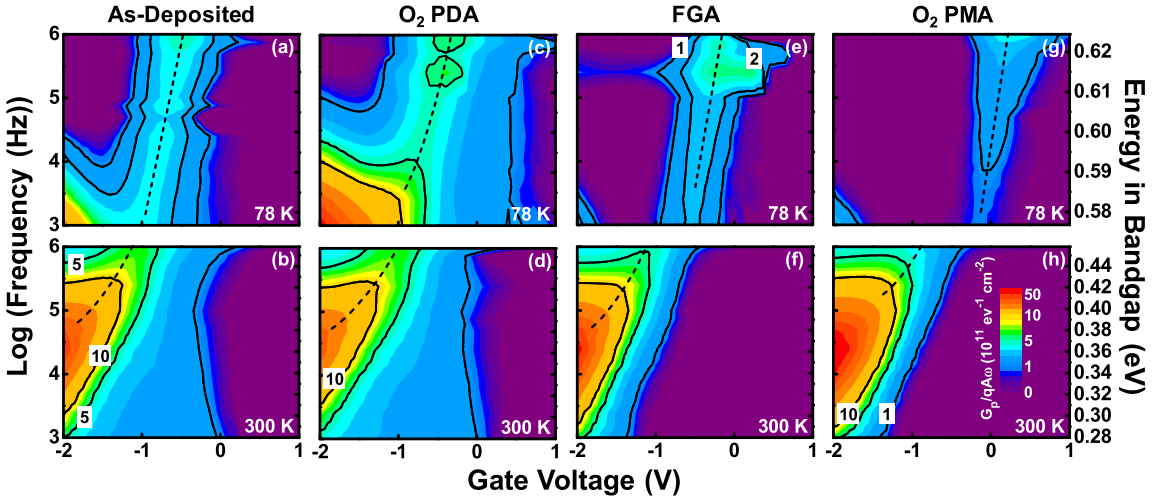

Fig. 4. G_p/ω contours of the (100)Ge MOS-C on GaAs via an AlAs buffer architecture measured at 78 K (top row) and 300 K (bottom row) for the (a-b) as-deposited, (c-d) O_2 PDA, (e-f) FGA, and (g-h) O_2 PMA annealing schemes.

oxide defects in close proximity ($\leq$1 nm) to the interface [21]. On the other hand, the G_p/ω contour widths tapered significantly for the FGA and O_2 PMA cases, as shown in Fig. 4(e)–(h), respectively. Furthermore, the Fermi-level traces appeared steeper for both FGA and O_2 PMA as compared to either as-deposited or O_2 PDA conditions. Such steep Fermi-level traces demonstrate good modulation of the Fermi level with respect to gate voltage (V_G), corresponding to efficacious D_{it} passivation [25]. The reduction of the measured G_p/ω contour intensity to below background levels [Fig. 4(g)] indicates excellent electrical passivation, expected to correlate with a strong decrease in D_{it} for the FGA and O_2 PMA schemes.

From the *C–V* hysteresis, the trapped oxide charge density (N_{OT}) was extracted for each annealing condition using [26]

$$N_{OT} = \frac{\Delta V_{FB} C_{ox}}{q} \tag{1}$$

where ΔV_{FB} is the flat-band voltage (V_{FB}) shift (also known as hysteresis) between the bidirectional 100-kHz *C–V* sweep, q is the elementary charge, and C_{ox} is the oxide capacitance per unit area. Additionally, the EOT value for each process condition was extracted. Table II summarizes the EOT and N_{OT} values extracted from the (100)Ge MOS *C–V* measurements for the various annealing schemes investigated. As expected, EOT is highest for the O_2 PMA scheme, which correlates well with the significant decrease in C_{max} shown in Fig. 3(g) and (h). N_{OT} also decreases with annealing, and was found to reduce the most under O_2 PMA, whereas FGA yielded the second lowest N_{OT} value. Furthermore, the as-deposited and O_2 PDA processes were found to exhibit similarly high N_{OT}, attributed to the formation of MIGS as previously discussed.

D_{it} values for each annealing scheme were also extracted using the conductance method corrected for surface potential fluctuation [27], [28],

$$D_{it} = \left(\frac{G_p}{\omega}\right)_{max} \{f_D(\sigma_s) q A\}^{-1} \tag{2}$$

TABLE II
EOT AND N_{OT} EXTRACTED FROM THE AS-DEPOSITED AND INVESTIGATED ANNEALING SCHEMES FOR THE (100)Ge MOS-C DEVICES

Annealing Scheme	*EOT* (nm)	N_{OT} (10^{11} cm^{-2})
As-Deposited	4.95	8.82
O_2 PDA	5.56	8.01
O_2 PMA	6.62	4.81
FGA	5.45	6.15

TABLE III
EOT AND N_{OT} EXTRACTED FROM THE AS-DEPOSITED AND INVESTIGATED ANNEALING SCHEMES FOR THE (110)Ge MOS-C DEVICES

Annealing Scheme	*EOT* (nm)	N_{OT} (10^{11} cm^{-2})
As-Deposited	5.06	9.68
O_2 PDA	4.75	11.4
O_2 PMA	6.51	5.17
FGA	5.51	7.74

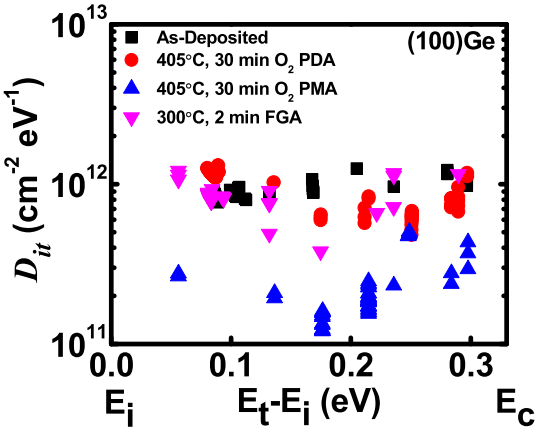

Fig. 5. D_{it} as a function of energy for the (100)Ge MOS-C on GaAs via an AlAs buffer architecture under various annealing schemes.

where $(G_p/\omega)_{\max}$ is the maximum parallel conductance G_p normalized by angular frequency ω, q is the electronic charge, $f_D(\sigma_s)$ is the universal function of the standard deviation of band bending σ_s, and A is the capacitor area. The conductance method was performed from 78 to 300 K to allow for sampling of the D_{it} distribution over multiple ranges within the bandgap, wherein (2) can be applied to show the distribution of D_{it} as a function of energy within the Ge bandgap [20], [21], [27]. Fig. 5 shows D_{it} extracted from the measured (100)Ge pMOS devices for all annealing schemes. The D_{it} is highest across the bandgap for the as-deposited devices (black squares) and is generally improved using annealing conditions. The lowest D_{it} distribution was observed for the O_2 PMA scheme ($D_{it}^{\min} = 1.2 \times 10^{11}$ cm^{-2}·eV^{-1}), drawing a correlation to the N_{OT} results previously discussed. Similarly, the second lowest D_{it} distribution was achieved using FGA, exhibiting a low D_{it} value of 3.79×10^{11} cm^{-2}·eV^{-1}. The increase in D_{it} closer to midgap observed across all devices was due chiefly to the temperature-dependent supply of minority carriers to the inversion layer, which contributes to higher conductance, and thus leads to an overestimation of D_{it} [8], [20], [21].

D. MOS Capacitor C–V and Conductance Characteristics of Al/Al_2O_3/GeO_x/(110)Ge Gate Stacks

Fig. 6 shows the C–V characteristics of the (110)Ge MOS-Cs measured from 78 to 300 K. Unlike the (100)Ge system, however, the low-frequency inversion response was not effectively suppressed at lower temperatures. Moreover, none of the investigated annealing schemes were found to strongly aid in the reduction of the low-frequency inversion response. These results suggest that despite passivation of D_{it} via GeO_x regrowth and subsequent annealing, there still exist shallow traps with quick response times distributed throughout the Ge bandgap. Moreover, the frequency-dependent threshold voltage shift indicates a high density of electrically active traps in close proximity to the valance band [20]. Similar to the case for the (100)Ge devices, $C_{\max}$ was observed to decrease for the FGA and O_2 PMA processes, demonstrating a general increase in EOT as well as a significant increase in EOT for the O_2 PMA process, specifically. However, unlike the (100)Ge devices processed under the O_2 PDA scheme, EOT was found to decrease for (110)Ge devices subjected to O_2 PDA. Additionally, a small frequency dispersion kink in the depletion regime was apparent for the as-deposited and O_2 PDA devices, as shown in Fig. 6(a) and (c). The dispersion kink is fully suppressed with FGA and O_2 PMA, as shown in Fig. 6(e) and (g), mirroring the results for (100)Ge pMOS.

Fig. 7 shows the as-deposited, O_2 PDA, O_2 PMA, and FGA G_p/ω contours for the (110)Ge MOS-Cs. The G_p/ω contours shown are from measurements taken at 78 and 300 K in order to suppress the minority carrier weak inversion response, and therefore yield a more accurate representation of the devices' FLEs. However, as discussed earlier, a significant inversion-like response remains for the measured (110)Ge G_p/ω conductance contours, as evidenced in the C–V measurements. Despite this, the Fermi level can be traced at 78 K, as shown in Fig. 7. As with the (100)Ge devices, a significant broadening of the conductance contours was observed at 78 and 300 K for the as-deposited and O_2 PDA schemes, as shown in Fig. 7. This suggests that for the as-deposited and O_2 PDA processes, a large presence of D_{it} (and/or N_{OT} in the vicinity of the interface) remains following the anneal step, thereby resulting in increased carrier trapping as opposed to O_2 PMA and FGA. Moreover, the Fermi-level traces for the as-deposited and O_2 PDA schemes exhibited arcing at lower temperature, indicative of poor FLE [8]. Conversely, the FGA and O_2 PMA process conditions resulted in devices exhibiting narrow conductance contours and steep Fermi-level traces, and hence demonstrating good modulation of the Fermi level with respect to gate voltage due to improved D_{it} passivation [25]. Additionally, the G_p/ω contour intensity for the FGA and O_2 PMA devices was found to decrease with respect to the as-deposited control, corresponding to a decrease in conductance

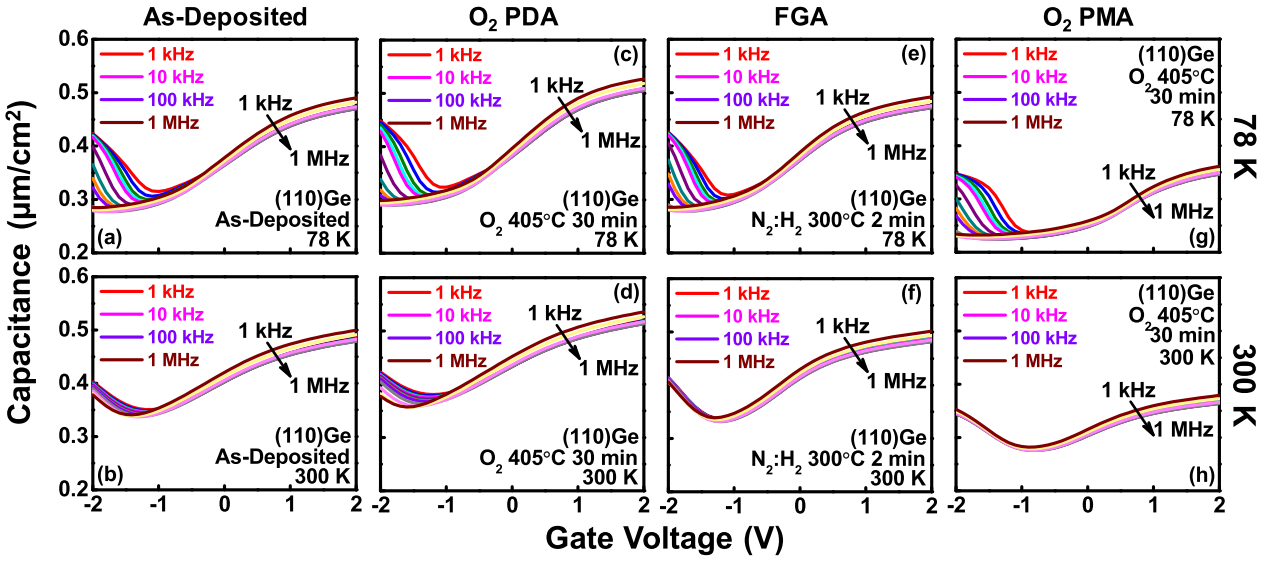

Fig. 6. *C–V* characteristics of the (110)Ge MOS-C on GaAs via an AlAs buffer architecture, where (a) and (b) *C–V* curves measured at 78 and 300 K for the as-deposited case, (c) and (d) *C–V* curves measured at 78 and 300 K for the O_2 PDA case, (e) and (f) *C–V* curves measured at 78 and 300 K for the FGA case, and (g) and (h) are *C–V* curves measured at 78 and 300 K for the O_2 PMA case.

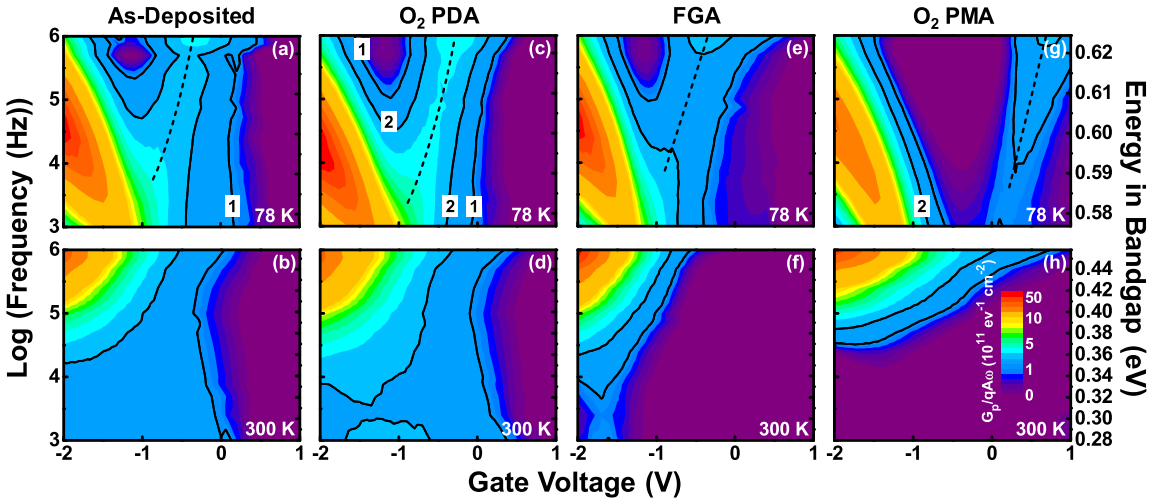

Fig. 7. G_p/ω contours of the (110)Ge MOS-C on GaAs via an AlAs buffer architecture measured at 78 K (top row) and 300 K (bottom row) for the (a-b) as-deposited, (c-d) O_2 PDA, (e-f) FGA, and (g-h) O_2 PMA annealing schemes.

magnitude and a reduction in D_{it}. Table III summarizes the EOT and N_{OT} values extracted from the (110)Ge MOS *C–V* measurements. As with the (100)Ge devices, EOT was highest under O_2 PMA conditions, correlating with the substantial decrease observed in C_{max} [Fig. 6(g) and (h)] previously attributed to the formation of Al_2O_3 at the Al/oxide interface. Moreover, N_{OT} was found to reduce with annealing, excluding O_2 PDA, and saw the largest improvement via O_2 PMA.

Fig. 8 shows D_{it} extracted from the measured (110)Ge devices as processed under each annealing scheme. D_{it} was found to be highest throughout the bandgap for the as-deposited control (black squares), and was improved under the different annealing schemes, with the exception of O_2 PDA. Moreover, a low D_{it} value of 3.84×10^{11} $cm^{-2}{\cdot}eV^{-1}$ was achieved using the FGA scheme, whereas a D_{it} minimum of 2.56×10^{11} $cm^{-2}{\cdot}eV^{-1}$ was achieved using the O_2 PMA scheme. Mirroring the results from the (100)Ge devices, an increase in D_{it} in proximity to midgap was observed across all devices, due in part to the temperature-dependent supply of minority carriers as well as the shallow traps observed to be specific to epitaxial (110)Ge.

E. Comparison of Epitaxial (100)Ge and (110)Ge pMOS

As hitherto demonstrated, a difference in the efficacy of the interfacial passivation and annealing processes was observed between (100)Ge and (110)Ge pMOS. A comparison of ΔV_{FB} between (100)Ge and (110)Ge more clearly highlights this result, as shown in Fig. 9. From Fig. 9, one can find that (110)Ge pMOS exhibited a larger ΔV_{FB} at 300 K, independent of annealing scheme, as compared to (100)Ge. This can be attributed to the difference in GeO_x stoichiometry between the two orientations. Specifically, the lower coordination of the $Ge_2O_3^-$ observed on (110)Ge would introduce

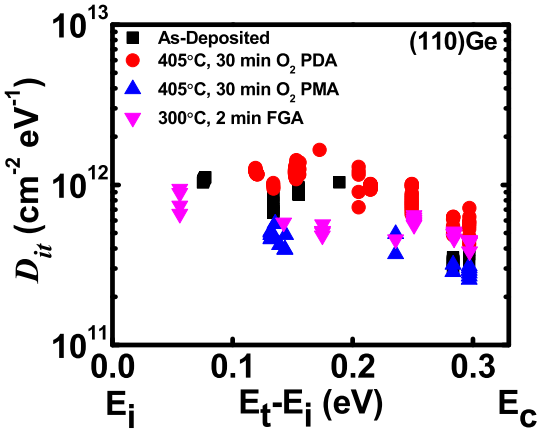

Fig. 8. D_{it} as a function of energy for the (110)Ge MOS-C on GaAs via an AlAs buffer architecture under various annealing schemes.

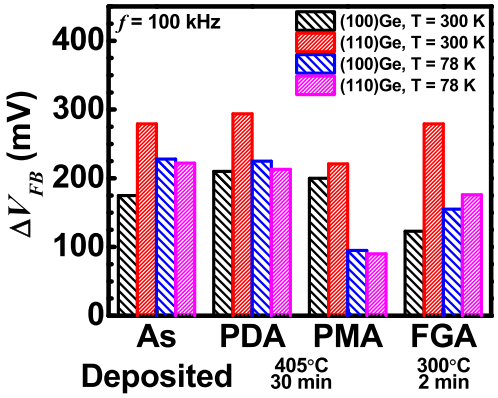

Fig. 9. Comparison of ΔV_{FB} extracted from 78 and 300 K *C–V* measurements ($f = 100$ kHz) as a function of orientation and annealing.

a greater number of oxide (vacancy) defect states, characterized by the $O_3 \equiv Ge\bullet$ microstructure, thereby leading to increased charge trapping within the interfacial passivation layer. Moreover, oxide defects in close proximity ($\leq$1 nm) to the GeO_x/Ge interface would be electrically indistinguishable from interface disorder-induced D_{it}, thereby leading to an increase in D_{it} on the (110)Ge surfaces studied in this paper. Furthermore, the presence of nonstoichiometric GeO_x would suggest incomplete DB passivation due to insufficient oxygen incorporation at the Ge surface during oxidation. These expected results are in agreement with the increased (110)Ge N_{OT} and D_{it} values presented earlier; however, they do not fully explain the discrepancy observed between bulk and epitaxial Ge [13], the qualitative difference in D_{it} trends for (100)Ge and (110)Ge orientations, and the origin of the difference in (100)Ge and (110)Ge GeO_x composition.

To account for these differences, it becomes necessary to understand the impact of crystallographic orientation on surface reconstruction and DB formation. In general, it is understood that surface reconstruction processes occur in order to reduce surface energy and compensate for the unequal interatomic forces experienced by the surface terminating atoms of a crystal [29]. In doing so, additional bonds between surface atoms are formed (e.g., dimers), thereby reducing the DB density at the surface and the surface energy. Correspondingly, the DB density for differing surface orientations is expected to differ, not only due to the intrinsic differences in surface atom density, but as well the corresponding differences in surface reconstruction.

Several decades of work with Si have experimentally confirmed the effect of orientation on DB microstructure and density [30]. Extending this paper and comparing with electrical (e.g., *C–V*) results, a near one-to-one correspondence between DB and D_{it} density was observed in many cases [31], [32]. Similarly, recent work with Ge has identified corresponding P_{b0} and P_{b1}-like defect centers on (111)Ge and (100)Ge, respectively [33], [34]. Moreover, Baldovino *et al.* [35] have demonstrated the effect of different oxidation conditions and oxidizing species on DB and oxide defect densities, as well as the corresponding density and distribution of D_{it} throughout the upper half of the Ge bandgap. More concretely, Molle *et al.* [36] have shown a direct correlation between surface reconstruction and the chemical reactivity and MOS properties, e.g., D_{it}, for $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS interfaces on nominally (100)$In_{0.53}Ga_{0.47}As$ surfaces. Last, Hudait *et al.* [4] have revealed a distinct difference in the surface reconstructions of (100)Ge and (110)Ge grown on GaAs substrates [4].

Based on these interpretations, it can be posited that the observed differences in passivation efficacy in this paper stem from the fundamentally different surface reconstructions, and therefore defect microstructure and reactivity, between epitaxial (100)Ge and (110)Ge surfaces. Correspondingly, the difference in surface reactivity leads to oxygen incorporation that mimics atomic oxygen (O_1) oxidation, generating oxide defects (vacancies) within the "bulk" GeO_x as well as at the GeO_x/(110)Ge interface for (110)Ge surfaces [35]. Conversely, for the oxidation temperature (450 °C) employed in this paper, epitaxial (100)Ge surfaces oxidize via the rate-limited O_2 migration process, i.e., molecular oxygen diffusion through the growing interfacial oxide layer [37], [38]. Thus, it can be said that at temperatures insufficient to promote the formation of GeO_2, oxide/epitaxial (110)Ge interfaces form the nonstoichiometric $Ge_2O_3^-$, leading to degraded MOS device performance. This is further evidenced by the (110)Ge D_{it} trend (i.e., a gradual increase toward midgap) observed in this paper, which mirrors that found by Baldovino *et al.* [35] for Ge surfaces oxidized via atomic oxygen.

IV. Conclusion

In summary, high-quality crystallographically oriented epitaxial (100)Ge and (110)Ge were grown on GaAs substrates using AlAs buffers via solid-source MBE. Various process conditions were implemented for the fabrication of pMOS capacitors on epitaxial (100)Ge and (110)Ge for the first time. HR-TEM micrographs demonstrated the successful growth of device-quality epitaxial Ge layers and sharp heterointerfaces between Al_2O_3/Ge as well as Ge/AlAs for each orientation. The fabricated pMOS devices demonstrated excellent electrical characteristics with efficient modulation of the Fermi level from midgap to the conduction band edge, corresponding to

a minimum D_{it} value of 1.2×10^{11} cm^{-2}·eV^{-1} on (100)Ge, indicative of a high-quality oxide/Ge heterointerface and an effective electrical passivation of the Ge surface. PDA under O_2 ambient was found to be less effective at reducing N_{OT} as compared to forming gas or O_2 PMA, indicating that metal-induced bandgap states at the gate metal/dielectric interface have a notable impact on Ge pMOS N_{OT}. On the other hand, a tradeoff must be made between the oxide trap density and EOT when using PMA under O_2 or forming gas ambient.

Additionally, the differences in epitaxial (100)Ge and (110)Ge MOS interfaces have been elucidated for the first time. The effect of surface reconstruction and reactivity was correlated with MOS electrical characterization, suggesting that increased oxidation temperatures are necessary to form stoichiometric GeO_2 on epitaxial (110)Ge surfaces, and thereby improve passivation efficacy. Consequently, the high-quality growth of crystallographically oriented epitaxial (100)Ge and (110)Ge on AlAs/GaAs substrates and the superior electrical characteristics of fabricated (100)Ge and (110)Ge pMOS devices provide a pathway for the realization of future high-mobility Ge-based FinFETs for low-voltage, high-performance CMOS logic applications.

Acknowledgment

The authors would like to thank the National Science Foundation.

References

[1] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012, doi: 10.1109/TED.2012.2193129.

[2] M. Zhu, H.-C. Chin, G. S. Samudra, and Y.-C. Yeo, "Fabrication of p-MOSFETs on germanium epitaxially grown on gallium arsenide substrate by chemical vapor deposition," *J. Electrochem. Soc.*, vol. 155, no. 2, pp. H76–H79, Apr. 2008, doi: 10.1149/1.2811859.

[3] M. Bosi and G. Attolini, "Germanium: Epitaxy and its applications," *Prog. Cryst. Growth Charact. Mater.*, vol. 56, nos. 3–4, pp. 146–174, Dec. 2010. [Online]. Available: https://doi.org/10.1016/j.pcrysgrow.2010.09.002

[4] M. K. Hudait, Y. Zhu, N. Jain, and J. L. Hunter, Jr., "Structural, morphological, and band alignment properties of GaAs/Ge/GaAs heterostructures on (100), (110), and (111)A GaAs substrates," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 31, no. 1, pp. 011206-1–011206-14, Jan/Feb. 2013. [Online]. Available: https://dx.doi.org/10.1116/1.4770070

[5] S. H. Tang *et al.*, "High quality Ge thin film growth by ultrathin vacuum chemical vapor deposition on GaAs substrate," *Appl. Phys. Lett.*, vol. 98, no. 16, pp. 161905-1–161905-3, Apr. 2011. [Online]. Available: https://dx.doi.org/10.1063/1.3580605

[6] M. Clavel, P. Goley, N. Jain, Y. Zhu, and M. K. Hudait, "Strain-engineered biaxial tensile epitaxial germanium for high-performance Ge/InGaAs tunnel field-effect transistors," *IEEE J. Electron Devices Soc.*, vol. 3, no. 3, pp. 184–193, May 2015, doi: 10.1109/JEDS.2015.2394743.

[7] M. K. Hudait, M. Clavel, P. Goley, N. Jain, and Y. Zhu, "Heterogeneous integration of epitaxial Ge on Si using AlAs/GaAs buffer architecture: Suitability for low-power fin field-effect transistors," *Sci. Rep.*, vol. 4, pp. 6964–6970, Nov. 2014, doi: 10.1038/srep06964.

[8] P. D. Nguyen *et al.*, "Heteroepitaxial Ge MOS devices on Si using composite AlAs/GaAs buffer," *IEEE J. Electron Dev. Soc.*, vol. 3, no. 4, pp. 341–348, Apr. 2015, doi: 10.1109/JEDS.2015.2425959.

[9] M. K. Hudait, M. Clavel, P. S. Goley, Y. Xie, and J. J. Heremans, "Magnetotransport properties of epitaxial Ge/AlAs heterostructures integrated on GaAs and silicon," *ACS Appl. Mater. Inter.*, vol. 7, no. 40, pp. 22315–22321, Oct. 2015, doi: 10.1021/acsami.5b05814.

[10] C. L. Andre, "III-V semiconductors on SiGe substrates for multijunction photovoltaics," Ph.D. dissertation, Ohio State, Columbus, OH, USA, 2004.

[11] J. T. Kavalieros *et al.*, "Tri-gate transistor architecture with *high-k* gate dielectric, metal gates and strain engineering," in *Proc. VLSI Symp. Tech.*, Oct. 2006, pp. 50–51, doi: 10.1109/VLSIT.2006.1705211.

[12] C. Young *et al.*, "(110) and (100) sidewall-oriented FinFETs: A performance and reliability investigation," *Solid-state Electron.*, vol. 78, pp. 2–10, Dec. 2012, doi: 10.1016/j.sse.2012.05.045.

[13] T. Sasada, Y. Nakakita, M. Takenaka, and S. Takagi, "Surface orientation dependence of interface properties of GeO_2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation," *J. Appl. Phys.*, vol. 106, no. 7, pp. 073716-1–073716-7, Apr. 2009. [Online]. Available: https://dx.doi.org/10.1063/1.3234395

[14] R. Zhang, N. Taoka, P.-C. Huang, M. Takenaka, and S. Takagi, "1-nm-thick EOT high mobility Ge n- and p-MOSFETs with ultra-thin GeOx/Ge MOS interfaces fabricated by plasma post oxidation," in *IEDM Tech. Dig.*, Dec. 2011, pp. 28.3.1–28.3.4, doi: 10.1109/IEDM.2011.6131630.

[15] C. H. Lee, T. Nishimura, C. Lu, S. Kabuyanagi, and A. Toriumi, "Dramatic effects of hydrogen-induced out-diffusion of oxygen from Ge surface on junction leakage as well as electron mobility in n-channel Ge MOSFETs," in *IEDM Tech. Dig.*, Dec. 2014, pp. 32.5.1–32.5.4, doi: 10.1109/IEDM.2014.7047156.

[16] X. Gong *et al.*, "InAlP-capped (100) Ge nFETs with 1.06 nm EOT: Achieving record high peak mobility and first integration on 300 mm Si substrate," in *IEDM Tech. Dig.*, Dec. 2014, pp. 9.4.1–9.4.4, doi: 10.1109/IEDM.2014.7047017.

[17] H. Arimura *et al.*, "Ge nFET with high electron mobility and superior PBTI reliability enabled by monolayer-Si surface passivation and La-induced interface dipole formation," in *IEDM Tech. Dig.*, Dec. 2015, pp. 21.6.1–21.6.4, doi: 10.1109/IEDM.2015.7409752.

[18] B. Liu *et al.*, "High performance Ge CMOS with novel InAlP-passivated channels for future sub-10 nm technology node applications," in *IEDM Tech. Dig.*, Dec. 2013, pp. 26.7.1–26.7.4, doi: 10.1109/IEDM.2013.6724700.

[19] C.-M. Lin *et al.*, "Interfacial layer-free ZrO_2 on Ge with 0.39-nm EOT, K~43,~2×10^{-3} A/cm^2 gate leakage, SS =85 mV/dec, Ion/Ioff =6×10^5, and high strain response," *IEDM Tech. Dig.*, Dec. 2012, pp. 23.2.1–23.2.4, doi: 10.1109/IEDM.2012.6479086.

[20] K. Martens *et al.*, "On the correct extraction of interface trap density of MOS devices with high-mobility semiconductor substrates," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 547–556, Feb. 2008, doi: 10.1109/TED.2007.912365.

[21] D. Kuzum, "Interface-engineered Ge MOSFETs for future high performance CMOS applications," Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, USA, Dec. 2009.

[22] V. Heine, "Theory of surface states," *Phys. Rev.*, vol. 138, no. 6A, pp. A1689–A1696, Jun. 1965. [Online]. Available: https://doi.org/10.1103/PhysRev.138.A1689

[23] S. G. Louie and M. Cohen, "Electronic structure of a metal-semiconductor interface," *Phys. Rev. B, Condens. Matter*, vol. 13, no. 6, pp. 2461–2469, Mar. 1976. [Online]. Available: https://doi.org/10.1103/PhysRevB.13.2461

[24] Y. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *J. Appl. Phys.*, vol. 92, no. 12, pp. 7266–7271, Dec. 2012. [Online]. Available: https://dx.doi.org/10.1063/1.1521517

[25] H. C. Lin *et al.*, "The Fermi-level efficiency method and its applications on high interface trap density oxide-semiconductor interfaces," *Appl. Phys. Lett.*, vol. 94, no. 15, p. 153508, 2009. [Online]. Available: https://dx.doi.org/10.1063/1.3113523

[26] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. Hoboken, NJ, USA: Wiley, 2006, doi: 10.1002/0471749095.

[27] J. R. Brews, "Rapid interface parametrization using a single MOS conductance curve," *Solid-State Electron.*, vol. 26, no. 8, pp. 711–716, Aug. 1983. [Online]. Available: https://doi.org/10.1016/0038-1101(83)90030-8

[28] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Hoboken, NJ, USA: Wiley, 2003.

[29] H. J. W. Zandvliet, "The Ge(001) surface," *Phys. Rep.*, vol. 388, no. 1, pp. 1–40, Sep. 2003. [Online]. Available: https://doi.org/10.1016/j.physrep.2003.09.001

[30] E. H. Poindexter, "MOS interface states: Overview and physicochemical perspective," *Semicond. Sci. Technol.*, vol. 4, no. 12, pp. 961–969, Aug. 1989, doi: 10.1088/0268-1242/4/12/001.

[31] P. J. Caplan, E. H. Poindexter, B. E. Deal, and R. R. Razouk, "ESR centers, interface states, and oxide fixed charge in thermally oxidized silicon wafers," *J. Appl. Phys.*, vol. 50, no. 9, pp. 5847–5854, May 1979. [Online]. Available: https://dx.doi.org/10.1063/1.326732

[32] E. H. Poindexter, P. J. Caplan, B. E. Deal, and R. R. Razouk, "Interface states and electron spin resonance centers in thermally oxidized (111) and (100) silicon wafers," *J. Appl. Phys.*, vol. 52, no. 2, pp. 879–884, Oct. 1980. [Online]. Available: https://dx.doi.org/10.1063/1.328771

[33] S. Paleari, S. Baldovino, A. Molle, and M. Fanciulli, "Evidence of trigonal dangling bonds at the Ge(111)/oxide interface by electrically detected magnetic resonance," *Phys. Rev. Lett.*, vol. 110, no. 20, pp. 206101-1–206101-5, May 2013. [Online]. Available: https://doi.org/10.1103/PhysRevLett.110.206101

[34] S. Baldovino, A. Molle, and M. Fanciulli, "Evidence of dangling bond electrical activity at the Ge/oxide interface," *Appl. Phys. Lett.*, vol. 93, no. 24, pp. 242105-1–242105-3, Dec. 2008. [Online]. Available: https://dx.doi.org/10.1063/1.3050451

[35] S. Baldovino, A. Molle, and M. Fanciulli, "Influence of the oxidizing species on the Ge dangling bonds at the (100)Ge/GeO_2 interface," *Appl. Phys. Lett.*, vol. 96, no. 22, pp. 222110-1–222110-3, Jun. 2010. [Online]. Available: https://dx.doi.org/10.1063/1.3446839

[36] A. Molle *et al.*, "Reconstruction dependent reactivity of As-decapped $In_{0.53}Ga_{0.47}As(001)$ surfaces and its influence on the electrical quality of the interface with Al_2O_3 grown by atomic layer deposition," *Appl. Phys. Lett.*, vol. 99, no. 19, pp. 193505-1–193505-3, Oct. 2011. [Online]. Available: https://dx.doi.org/10.1063/1.3659688

[37] M. Houssa *et al.*, "Ge dangling bonds at the (100)Ge/GeO_2 interface and the viscoelastic properties of GeO_2," *Appl. Phys. Lett.*, vol. 93, no. 16, pp. 161909-1–161909-3, Oct. 2008. [Online]. Available: https://dx.doi.org/10.1063/1.3006320

[38] L. Tsetseris and S. T. Pantelides, "Morphology and defect properties of the Ge-GeO_2 interface," *Appl. Phys. Lett.*, vol. 95, no. 26, pp. 262107-1–262107-3, Dec. 2009. [Online]. Available: https://dx.doi.org/10.1063/1.3280385

Peter D. Nguyen (S'13) received the B.S. and M.S. degrees in electrical engineering from Virginia Tech, Blacksburg, VA, USA, in 2014 and 2016, respectively, where he is currently pursuing the Ph.D. degree with the Bradley Department of Electrical and Computer Engineering.

Michael B. Clavel (S'09) received the B.S. and M.S. degrees in electrical engineering from Virginia Tech, Blacksburg, VA, USA, in 2013 and 2016, respectively, where he is currently pursuing the Ph.D. degree with the Bradley Department of Electrical and Computer Engineering.

Jheng-Sin Liu (S'15) received the B.S. degree in electrical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2011, and the M.S. degree electrical engineering from the Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, Taiwan, in 2013. He is currently pursuing the Ph.D. degree with the Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA, USA.

Mantu K. Hudait (M'08–SM'08) received the M.S. degree in materials science and engineering from IIT Kharagpur, Kharagpur, India, in 1992 and the Ph.D. degree in materials science and engineering from Indian Institute of Science, Bangalore, India, in 1999.

He is currently with Virginia Tech, Blacksburg, VA, USA, where he is involved in the heterogeneous integration of compound semiconductors and Ge on Si for tunnel transistors, quantum-well transistors, and photovoltaics.