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Performance Analysis of $TaSiO_x$ Inspired Sub-10 nm Energy Efficient $In_{0.53}Ga_{0.47}As$ Quantum Well Tri-Gate Technology

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ABSTRACT In this paper, for the first time, the performance analysis of short channel $In_{0.53}Ga_{0.47}As$ quantum well (QW) 3-D tri-gate technology with advanced high-κ gate dielectric, $TaSiO_x$ is presented. We benchmark the projected performance of sub-10 nm $In_{0.53}Ga_{0.47}As$ transistor technology as a function of fin width, fin aspect ratio, and gate length scaling based on present-day lithographic advancement aiding InGaAs QW tri-gate technology as a replacement to Si for sub-10 nm transistor technology. The highly scaled oxide (EOT $\sim$ 12Å) while retaining superior interfacial properties ($D_{it} \sim 4 \times 10^{11}$ $cm^{-2}eV^{-1}$) provides higher ON current for given idle performance. Furthermore, the simulated $In_{0.53}Ga_{0.47}As$ tri-gate transistor exhibits superior gate electrostatic control with low OFF-state current (I_{OFF}) $\sim$ 24.5 nA/μm, peak transconductance (g_m) $\sim$ 2 mS/ μm and high I_{ON}/I_{OFF} ratio $\sim 2.3 \times 10^3$, aiding the case of alternate channel transistors for high-speed and low-power CMOS logic.

INDEX TERMS InGaAs, InGaAs/InAlAs heterojunctions, Fin field-effect transistors, tri-gate, simulation.

I. INTRODUCTION

The aggressive scaling of silicon (Si)-based CMOS logic has led to an unprecedented performance enhancement, while facing several technical challenges to work around the severity of an increased power density and idle leakage. A key solution utilized so far involved carrier mobility enhancement through the application of strain to the Si channel [1]. However, mobility enhancement through strained Si is bound to hit its limit due to strain relaxation once it reaches its critical layer thickness and hence, an alternate channel with higher carrier mobility will play a crucial role in effectively reducing the power density. III-V compound semiconductors have been the frontrunner to replace Si based n-channel metal-oxide-semiconductor field effect transistors (n-MOSFETs) due to its extremely high electron mobility compared to that of strained Si [2]. Furthermore, with scaling of transistor nodes, the semiconductor industry was pushed to employ Si based 3-D architecture at the 22 nm node to improve gate electrostatics [3]. In retrospect to this, III-V quantum well (QW) tri-gate device architecture has been investigated extensively as a replacement to current Si technology [2], [4]. As the aggressive scaling of device dimensions makes current transistor technology more susceptible to short channel effects such as, drain induced barrier lowering (DIBL) and subthreshold slope (SS) degradation, novel solutions need to be employed to mitigate such technological hindrances. Improvement in gate electrostatics is an effective way to reduce short channel induced performance degradation. $TaSiO_x$ as a gate dielectric on alternate channel InGaAs material can exhibit superior interfacial quality with lower interface induced defects (D_{it}) $\sim$ $4x10^{11}$ $cm^{-2}eV^{-1}$ [4], which is on par with Al_2O_3 [2]. Furthermore, $TaSiO_x$ is highly scalable demonstrating low gate leakage with an equivalent oxide thickness (EOT) $\sim$ 12 Å [5].

In addition, the 3-D tri-gate architecture can induce high gate leakage due to the clustering of electric field lines at the corners of the fin [6]. In this paper, the tri-gate device with $TaSiO_x$ as gate dielectric employing lattice matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ system has been calibrated to be further scaled down and hence predict short channel

device performance using TCAD's self-consistent solver coupled with the modified local density approximation (MLDA) quantization model [7], [8]. The model is calibrated with reported $TaSiO_x$/InGaAs results [2], [4], [5] to further conduct a performance benchmarking analysis of sub-10 nm $In_{0.53}Ga_{0.47}As$ QW 3-D tri-gate technology based on current day lithographic limitations.

II. DEVICE STRUCTURES AND PHYSICAL MODELS

A. $In_{0.53}Ga_{0.47}As$ FIN STRUCTURE AND BAND ALIGNMENT

An ultra-scaled gate-drain and gate-source separation (L_{SIDE} = 5 nm) InGaAs QW transistor was demonstrated, increasing effective gate area over the channel [4] and hence improving electrostatic control. Subsequently, a simplified source/drain (S/D) scheme was employed with an epitaxially grown un-doped $In_{0.7}Ga_{0.3}As$ QW fin on an $In_{0.52}Al_{0.48}As$ bottom barrier (lattice mismatched system). However, this limited the critical thickness of the active layer due to strain induced dislocations due to film relaxation resulting in a shorter fin height.

To overcome this and optimize quantum confinement within the fin, the lattice-matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ system was employed to demonstrate taller fin height H_{FIN} = 50 nm and width W_{FIN} = 30 nm using inductively coupled plasma (ICP) dry etch [4], [5]. Following this, device quality ultra-high fin aspect ratio (H_{FIN}/W_{FIN}) long channel devices were demonstrated using a novel ICP etch process followed by a digital etch which avoided dry etch damage improving device performance [9], [10]. Fin dimensionality plays a very influential role in improving device performance against short channel effects as will be discussed later in this paper. Fig. 1 (a) and (b) shows the InGaAs QW fin structure with simplified S/D scheme [3]. Fig. 2 shows the band alignment of the lattice matched undoped $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ QW system along with InP substrate and $TaSiO_x$ as gate dielectric.

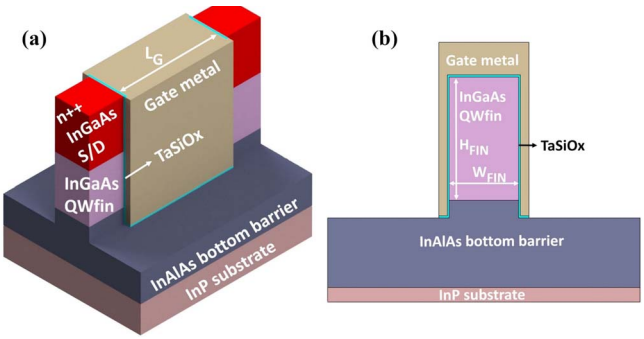

FIGURE 1. (a) Tri-gate InGaAs QW FinFET structure with simplified raised S/D scheme with scaled L_{SIDE} = 5nm [4], [5]. (b) Channel cross section with $TaSiO_x$ as gate dielectric on lattice matched (InGaAs/InAlAs) quantum well system.

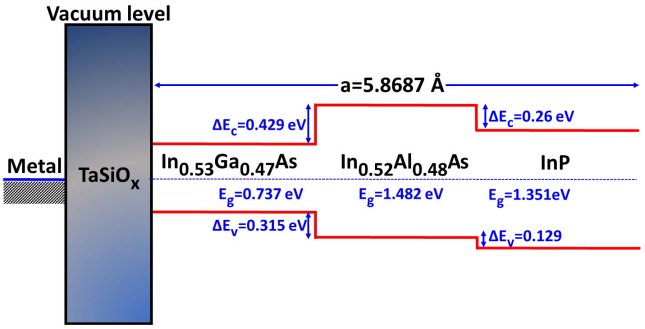

FIGURE 2. Band alignment of the epitaxially grown lattice matched Quantum well system. The lattice-matched QW system enables taller fins due to privation of critical thickness as in the case of $In_{0.7}Ga_{0.3}As$, however at the cost of mobility.

B. QUANTUM MECHANICAL MODEL

The MLDA model [7], [8] describes a multiple-electron system in a constant potential as a function of a spatially varying perturbation while accounting for quantum mechanical reflection (of the wave function) from an attractive potential, a phenomenon due to which the local density of states at the insulator/semiconductor interface shows oscillations and reduces to a null value [8]. This holds significant importance for the modelling of tri-gate transistors, given the narrow fin structure, in order to accurately describe the superior gate electrostatic control observed in tri-gate field effect transistors.

Therefore, we employ the MLDA model to all simulations in this work [8]. Furthermore, the quantum correction for carrier confinement in a QW shifts the carrier density centroid away from the interface by an additional spacing (t_{cen}) owing to the lack of carrier states. This can be observed in Fig. 3 resulting in the capacitance model shown in the inset of the figure. Consequently, the effective gate coupling will reduce in the form while accounting for spacing [11], [12]:

$$\frac{1}{C_{ox'}} = \frac{1}{C_{ox}} + \frac{1}{C_{cent}} = \frac{t_{ox}}{\varepsilon_o \varepsilon_{ox}} + \frac{t_{cen}}{\varepsilon_o \varepsilon_{ch}}$$

where, ε_{ch} is the dielectric constant of the alternate channel and C_{cent} is the centroid capacitance and is a function of the potential of the QW ($\Psi_{S,QW}$). The reduced oxide capacitance will hence affect device DIBL and SS characteristics:

$$SS = \frac{k_B T}{q}\left(1 + \frac{C_D}{C_{ox'}}\right).$$

A degraded SS is evident in the quantum mechanical model affecting the threshold voltage (V_T) roll-off hence worsening DIBL.

C. BENCHMARKING METHODOLOGY

The voltage of operation (V_{CC}) for the device is equal to the drain-to-source bias (V_{DS}) = 0.5V [13]. The threshold voltage (V_T) is selected at specified current $I_{DS} = 1\mu A/\mu m$ [14]. Approximately 1/3 of the gate voltage swing ($V_{GS} = V_{CC}$) below V_T is used to obtain the OFF-state current, I_{OFF} and

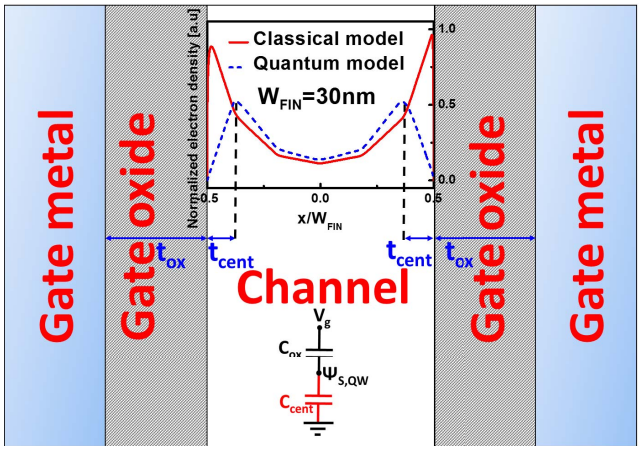

FIGURE 3. Schematic showing the shift of the normalized carrier density centroid away from the oxide/semiconductor interface. The carrier density for both models are normalized to the maximum carrier density of the classical model.

TABLE 1. Model parameters.

Parameter	Value
$E_{g,\Gamma}$	0.74eV
$E_{g,X}$	1.33eV
$E_{g,L}$	1.2eV
N_{ch}	$5*10^{17}$ (cm^{-3})
N_{SD}	$1*10^{20}$ (cm^{-3})
$m_{e,\Gamma}$*	$0.042m_0$
$m_{e,X}$*	$0.74m_0$
$m_{e,L}$*	$0.02m_0$
m_{hh}	$0.46m_0$
R_{SD}	150 Ω-μm
$\alpha_{\Gamma,InGaAs}$	$1.24eV^{-1}$
κ ($TaSiO_x$)	13

2/3 gate voltage (V_{GS}) swing over V_T provides the ON-state current, I_{ON} [13]. Short channel effects such as DIBL was evaluated as the shift in V_T at 1μA/μm with change in V_{DS} bias between 0.05V and 0.5V. Sub-threshold slope (SS) is calculated over the region of operation (V_{CC}). The calibration of the simulation model accounts for quantization effects which makes short channel effects more sensitive to device scaling. Furthermore, it has been shown that the sensitivity of ΔV_T increases below 15nm due to the amplification of quantization effects with deviation from the classical model [10].

D. DEVICE CALIBRATION

Fig. 4 shows the simulated capacitance-voltage (C-V) characteristics of an InGaAs QW tri-gate structure with highly scaled $TaSiO_x$ (EOT = 12 Å) as gate dielectric showing improved electrostatics over Al_2O_3 as gate oxide with same oxide thickness. The simulated results are in good agreement with the expected behavior presented for a planar device [2]. The response of the tri-gate FET at low fin aspect ratio is

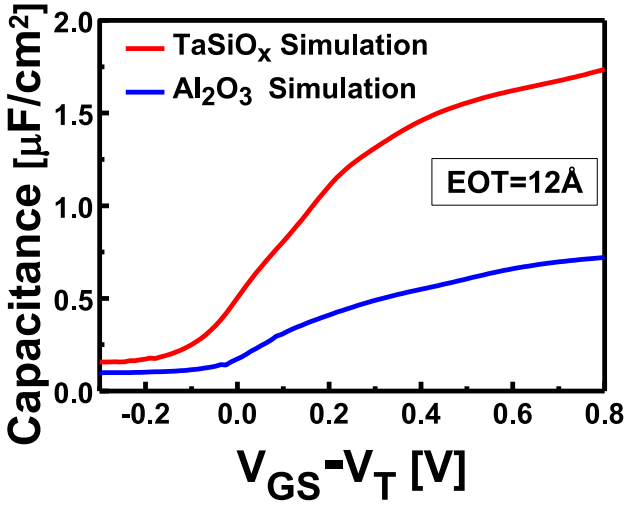

FIGURE 4. Simulated comparison showing improved electrostatics with $TaSiO_x$ (EOT = 12Å) over Al_2O_3 as gate dielectric. Both models have the same oxide thickness. The nature of the simulation agrees with data presented for the planar structure comparing Al_2O_3 and $TaSiO_x$ as gate dielectrics [2].

crucial to precisely determine the model's ability to estimate short channel effects and hence for L_G =60 nm, we base our model around $H_{FIN} = W_{FIN} = 40$ nm [5] employing the simulation parameters tabulated in Table 1. The influence of the interfacial properties on device characteristics is crucial to calibrate the device response. Depending on the magnitude, nature and position of traps, the C-V response of a device can be modelled [15]. Since we are modelling the device to follow the variation of DIBL and SS with L_G and W_{FIN} scaling based on previously presented data [5], the D_{it} distribution was developed which could agree with all variable parameters to calibrate the model to both DIBL and SS. Fig. 5 is the developed D_{it} distribution used to calibrate the model to C-V characteristics, transfer characteristics and short channel effects reported in [5]. The accuracy of the variation of short channel effects with the gate length and fin width variation aids to the validity of the developed distribution as depicted in Fig. 8 and 10. The D_{it} distribution implemented consisted of 3 Gaussian curves to fit the C-V and short channel effects. However, in the case of fitting DIBL, SS and C-V with a uniform distribution for several devices (i.e., multiple W_{FIN}), a small error towards the depletion region of the C-V response with doping $N_D = 5x10^{17}cm^{-3}$. This is also due to the fact that the reported C-V characteristics in [5] is for an n-doped MOSCAP, while an n-MOSFET requires a p-type channel doping indicating two samples of different dopant types and levels. However, to calibrate DIBL response, channel doping of $N_A = 5x10^{17}cm^{-3}$ provided accurate results while a doping of $N_D = 1x10^{17}cm^{-3}$ provided a matched C-V response as depicted in Fig. 6. Fig. 6 shows the calibrated C-V response of the InGaAs QW tri-gate structure with W_{FIN}= 45 nm and highly scaled $TaSiO_x$ gate oxide with EOT = 12Å ensuring favorable carrier response to gate bias [5].

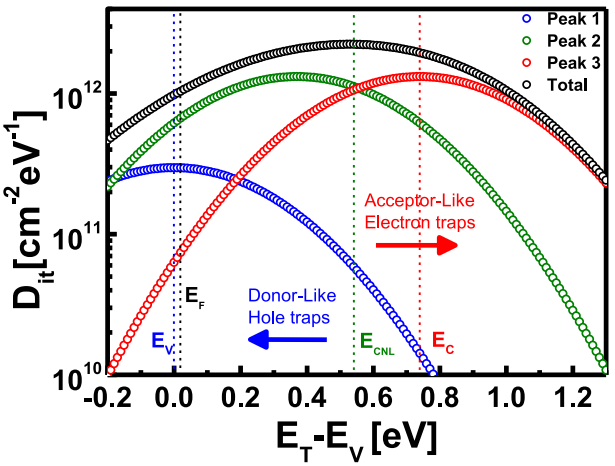

FIGURE 5. Developed D_{it} distribution for $TaSiO_x/In_{0.53}Ga_{0.47}As$ interface implemented to calibrate model to C-V characteristics, transfer characteristics and short channel effects presented in [5].

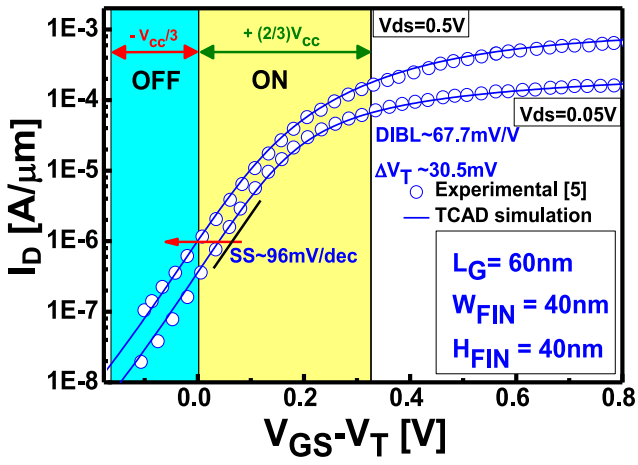

FIGURE 7. Transfer characteristics using TCAD simulation fitted to match reported experimental data [5]. Device operation range shows a high I_{ON}/I_{OFF} ratio~10^4. For performance analysis, I_D at V_T was selected as 1μA/μm as described InGaAs surface channel FET [14].

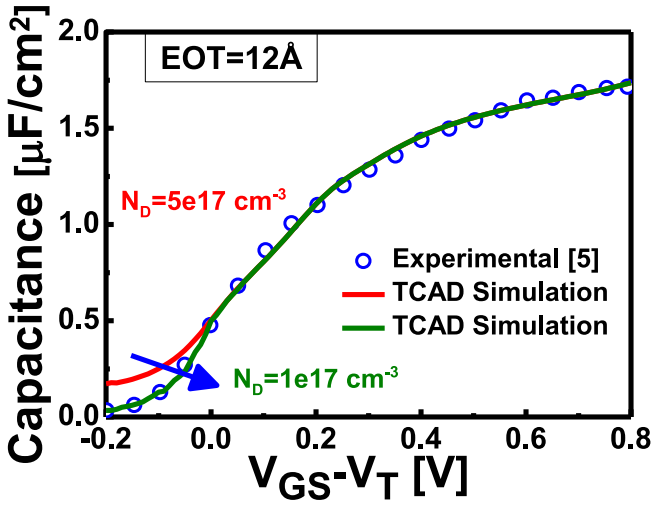

FIGURE 6. Simulated C-V characteristics using TCAD simulation fitted to presented experimental data [5]. The tri-gate QW fin width W_{FIN} = 45 nm and highly scaled (EOT = 12Å) $TaSiO_x$ as gate dielectric is in good agreement with presented experimental data [5].

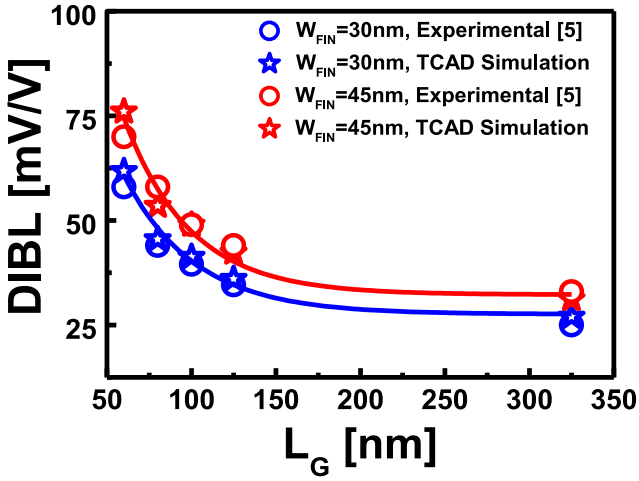

FIGURE 8. Simulated DIBL response with L_G scaling of the tri-gate QW fin has scaled to EOT = 12 Å using TCAD simulation along with best-fit curves fitted to simulation data points. Obtained data is in good agreement with the presented experimental data [5].

Fig. 7 shows the simulated transfer characteristics fitted to the experimental InGaAs QW tri-gate FET with L_G = 60nm and W_{FIN} = H_{FIN} = 40nm (low fin aspect ratio). The effective channel width of the fin structure is given by Z = 2*H_{FIN} + W_{FIN} = 120nm [5]. The simulation yields favorable results in good agreement with experimental data [5].

Fig. 8 and Fig. 9 show the calibrated DIBL and SS response as a function of gate length (L_G) scaling for W_{FIN} = 45nm and 30nm [5]. The figures depict the exponential increase in DIBL and SS with L_G being scaled below 150nm. This due to the amplification of short channel effects. Adding to this, we observe that 30nm devices show considerable improvement of both DIBL and SS over 45nm devices. This is a result of the deeper penetration of electric field into the channel through the side walls providing improved gate coupling over the channel from fin width reduction. The calibrated response of short channel effects with scaling of fin width are also in good agreement with reported data depicting the models accuracy. We continue to investigate the effect of fin dimension scaling on the short channel effects of the InGaAs QW tri-gate device with $TaSiO_x$ as gate dielectric to further understand the design criteria of sub-10nm post Si transistor technology.

III. RESULTS AND DISCUSSION

A. FIN SCALING INFLUENCE ON DEVICE PERFORMANCE

Fig. 10 shows the simulated DIBL response as a function of L_G/W_{FIN} with L_G = 60nm yielding favorable results with reported data [5]. Fin width (L_G/W_{FIN}) scaling is the primary factor that can be optimized to improve device performance against short channel effects. Beyond this, higher fin aspect ratios (H_{FIN}/W_{FIN}) can improve the performance

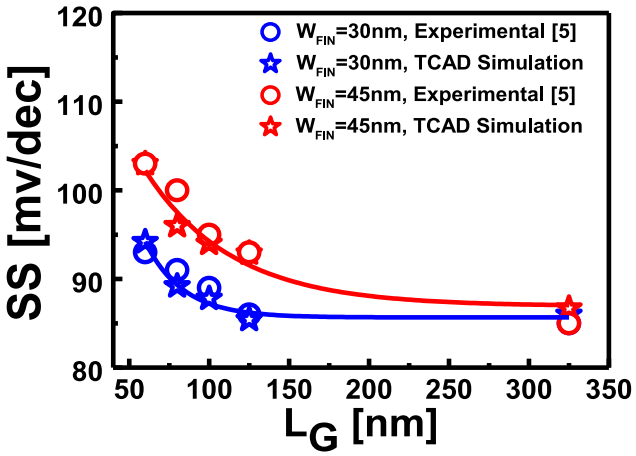

FIGURE 9. Simulated SS response with L_G scaling of the tri-gate QW fin has scaled EOT = 12 Å using TCAD simulation along with best-fit curves fitted to simulation data points. Obtained data is in good agreement with presented experimental data [5].

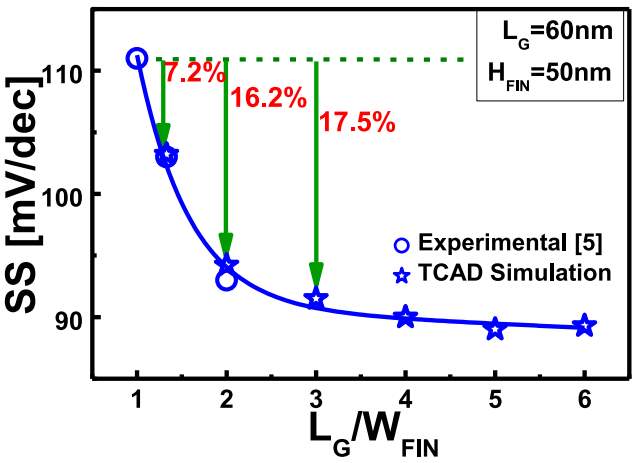

FIGURE 11. Simulated SS response as a function of L_G/W_{FIN} with L_G = 60nm along with best-fit curves fitted to simulation data points. Obtained data is in good agreement with presented experimental data [5].

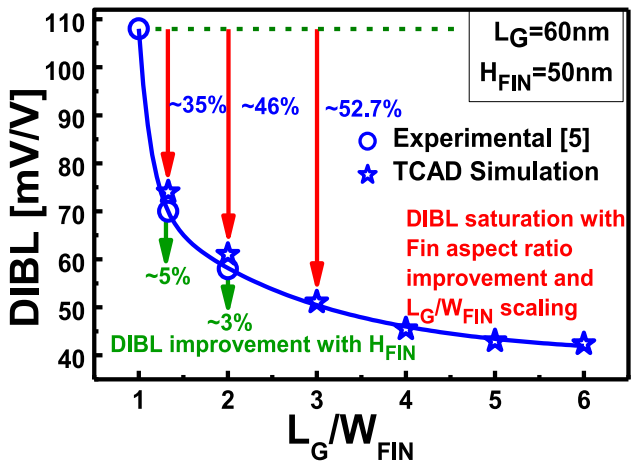

FIGURE 10. Simulated DIBL response as a function of L_G/W_{FIN} with L_G = 60nm along with best-fit curves fitted to simulation data points. Obtained data is in good agreement with presented experimental data [5].

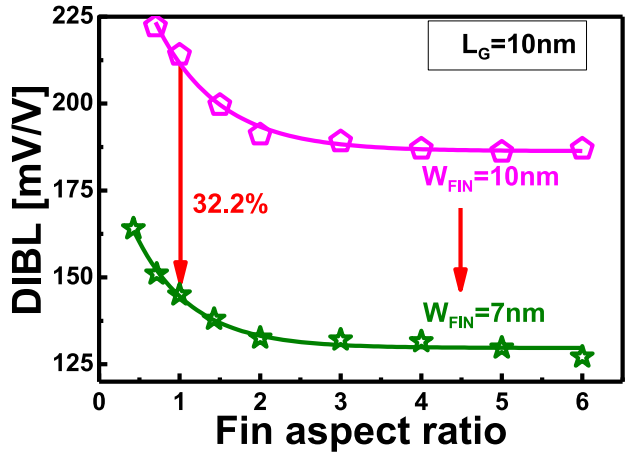

FIGURE 12. Simulated short channel (L_G = 10nm) DIBL response as a function of H_{FIN}/W_{FIN} with 10nm and 7nm W_{FIN} along with best-fit curves fitted to simulation data points. A 32% reduction in DIBL can be obtained by scaling fin width down to 7 nm.

against DIBL though its influence is lower compared to W_{FIN} scaling. The DIBL values decrease with increasing L_G/W_{FIN} (which means a smaller W_{FIN} is inevitable). This is attributed to the stronger electrostatic couple from a smaller W_{FIN}. We observe $\sim$ 52% drop in DIBL while scaling L_G/W_{FIN} between 1 and 3 as compared to Si fins which show a $\sim$ 65% drop in DIBL with scaling of L_G/W_{FIN} from 1 to 1.5 [16].

Fig. 11 shows modeled SS response as a function of L_G/W_{FIN}. Once again, the primary factor of SS improvement followed by optimization using fin aspect ratio. The influence of L_G/W_{FIN} on SS is as expected in favor of DIBL improvement in gate coupling with fin width reduction.

Fig. 12 and Fig. 13 show DIBL and SS improvement with fin aspect ratio. The reduction in both DIBL and SS saturates with doubling of the fin aspect ratio. This is due to the fact that the electric field created at the two side walls dominate the channel compared to influence from the top side. On the other hand, both DIBL and SS are improved with smaller W_{FIN} resulting in stronger electrostatic coupling from the two side walls which is regarded as the primary factor to improve gate electrostatics. Furthermore, H_{FIN} can be increased for improved carrier confinement taking into account the maximum fin height given a specific fin width to avoid yield issues. Ultra-high fin aspect ratios have been demonstrated on long channels as a promising step for the development of III-V QW tri-gate technology [9]. With continued scaling of L_G, the improvement in lithography and etch technology will play a crucial role in improving the performance of tri-gate QWFETs against short channel effects like SS and DIBL.

B. SHORT CHANNEL PERFORMANCE AND BENCHMARKING

Assuming transferable interfacial quality, the active layer is scaled to L_G = 10nm. Fig. 12 shows DIBL vs. fin aspect ratio for the scaled active layer. A 32% reduction in DIBL can be

achieved by scaling W_{FIN} from 10 nm to 7nm. The reduced improvement in performance against DIBL with variation against L_G/W_{FIN} is noticeable between L_G = 60nm and 10 nm. Fig. 13 shows reduction in SS for the short channel model with L_G = 10nm. The improvement with W_{FIN} reduction to 7nm along with SS saturation with high fin aspect ratios yields an SS ~ 120 mV/decade. High fin aspect ratio short channel devices for sub-10nm W_{FIN} are yet to be demonstrated for rectangular fins due to yield issues which can be improved using trapezoidal fins. However, rectangular fins exhibit superior electrostatics over their trapezoidal counterparts [17] while the latter can improve yield at the cost of device performance.

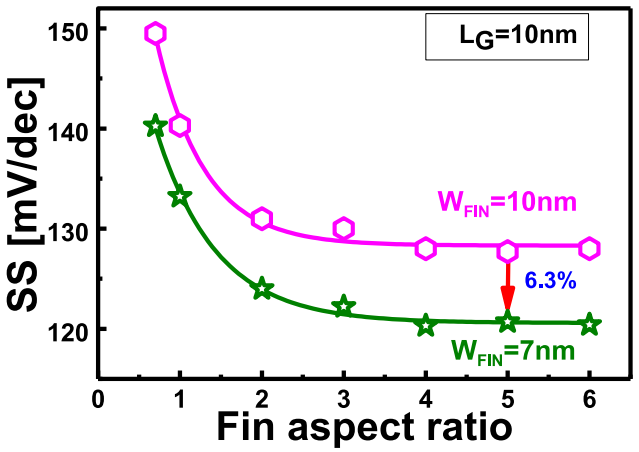

FIGURE 13. Simulated short channel (L_G = 10nm) SS response as a function of H_{FIN}/W_{FIN} with 10nm and 7nm W_{FIN} along with best-fit curves fitted to simulation data points. A 6% reduction in SS can be obtained by scaling fin width down to 7nm. However, this reduction has a drastic effect on the reduction of DIBL as can be seen in Fig. 12.

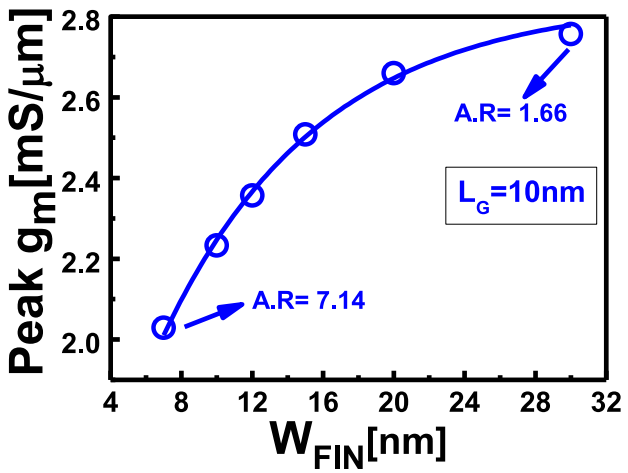

FIGURE 14. Simulated transconductance (g_m) response with W_{FIN} scaling with H_{FIN} = 50nm for L_G = 10 nm along with best-fit curves fitted to simulation data points.

Fig. 14 show the variation of transconductance (g_m) with W_{FIN} scaling for L_G = 10nm. The scaling of W_{FIN} which reduces ON current I_{ON} [10] negatively impacts the

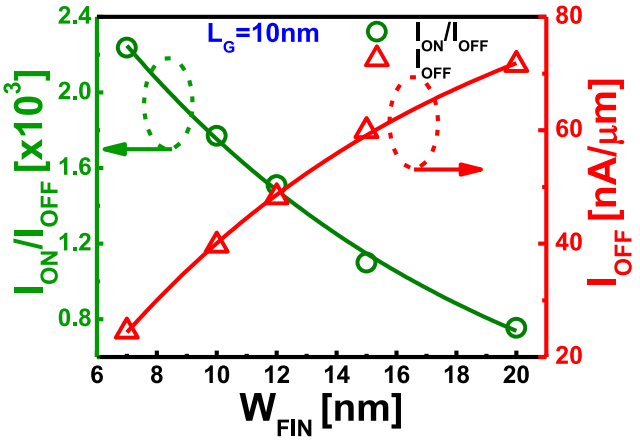

FIGURE 15. Observed short channel (L_G = 10nm) I_{ON}/I_{OFF} ratio along with best-fit curves fitted to simulation data points shows increase with W_{FIN} scaling for given I_{ON} with simultaneous reduction in I_{OFF} shows improved gate control.

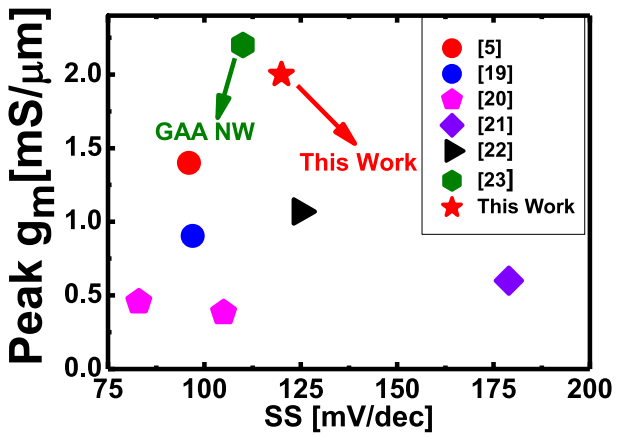

FIGURE 16. Performance benchmarking short channel (L_G = 10nm) InGaAs QW tri-gate structure with highly scaled $TaSiO_x$ (EOT = 12Å) as gate dielectric.

transconductance (g_m) as shown in Fig. 14. However, the severity of transconductance degradation reduces with scaling of the channel length which boosts ON current (I_{ON}) and hence improves the transconductance for given W_{FIN} [18]. The superior electrostatic properties of tri-gate architecture are enhanced with W_{FIN} reduction showing an improvement of the saturated peak g_m (from gate length scaling) [18]. Fig. 15 shows the variation of I_{ON}/I_{OFF} and I_{OFF} ratio with W_{FIN} depicting the tri-gate architectures superior electrostatic properties. We observe a near 45 nA/μm drop in OFF-state current along with a near 3-fold increase I_{ON}/I_{OFF} ratio showing improved gate control with W_{FIN} reduction. Fig. 16 is a benchmarking of transconductance (g_m) vs subthreshold slope (SS) aiding the case of $TaSiO_x$ as a gate dielectric with other relevant data having the same Indium composition in the channel aiding the case of tri-gate architecture. Table 2 shows the performance benchmarking of the short channel effects and device charactersitcs of simulated device structure with $TaSiO_x$ as gate dielectric.

TABLE 2. Performance benchmarking.

Reference	(Arch./Channel)	Oxide	L_G (nm)	Vds,Vgs (V)	EOT (Å)	DIBL (mV/V)	SS (mV/dec)	$\frac{I_{ON}}{I_{OFF}}$	g_m (mS/μm)
[5]	3D-$In_{0.53}Ga_{0.47}As$	$TaSiO_x$	60	0.5,0.5	12	68	96	$1.17x10^4$	~1.4
[9]	NW-$In_{0.53}Ga_{0.47}As$	Al_2O_3	240	0.5,1.0	22	180	155	$1x10^3$	0.255
[19]	UTB-$In_{0.53}Ga_{0.47}As$	HfO_2	40	0.5,0.5	-	110	83	$4x10^3$	1.2
[23]	NW-$In_{0.53}Ga_{0.47}As$	IL/ HfO_2	50	0.5,0.5	-	103*	96-400	$1.5\ x10^{3}$*	1.5-2.2*
[24]	NW-$In_{0.53}Ga_{0.47}As$	Al_2O_3	80	0.5,1.0	22	360	305	$~10^2$	0.73
[25]	3D-$In_{0.53}Ga_{0.47}As$-OI	-	50	0.5,0.5	CET=15	57**	92	$1.56x10^3$	0.615
[26]	NW-$In_{0.53}Ga_{0.47}As$	HfO_2	36	0.5,0.5	CET=16	-	90-210	$2.1x10^{3}$*	1.15-1.65
[27]	3D-$In_{0.53}Ga_{0.47}As$	-	30	0.5,0.5	-	90	100	$4x10^3$	0.9
This work	3D-$In_{0.53}Ga_{0.47}As$	$TaSiO_x$	60	0.5,0.5	12	~67.7	96	$1.17x10^4$	~1.4
This work	3D-$In_{0.53}Ga_{0.47}As$	$TaSiO_x$	10	0.5,0.5	12	130	120	$2.3\ x10^3$	2.04

*At SS_{min} **At I_D=0.5μA/μm

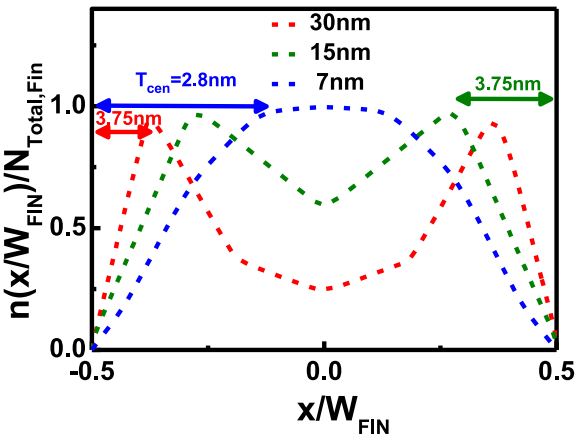

FIGURE 17. Normalized carrier density profile for W_{FIN} = 30nm, 15nm and 7nm. The fin structure exhibiting carrier volume inversion due to the amplification of quantization effects observes an apparent 'spread' in the charge centroid, i.e., a larger volume of the fin is completely inverted thereby reducing t_{cen} and hence EOT.

C. QUANTIZATION EFFECTS AND EOT SCALING

The sensitivity of ΔV_T increases below 15nm due to amplification of quantization effects with deviation from the classical model starting at W_{FIN} = 15nm [10]. Fin scaling leads to larger lateral electric field across its cross-section causing the carrier centroid to shift towards the interface thereby reducing the actual EOT with the reduction of T_{cen}. Adding to this, the amplification of quantization effects causes carrier volume inversion [28], thereby enhancing the gates inverting ability of the channel with a larger volume of the channel contributing to conduction leading to the enhancement of device performance.

Fig. 17 shows a comparison of the normalized electron density profile for W_{FIN} = 30nm, 15nm and 7nm. The fin structure exhibiting carrier volume inversion due to the amplification of quantization effects observes an apparent 'spread' in the charge centroid, i.e., a larger volume of the fin is completely inverted thereby reducing t_{cen} and hence the EOT as EOT = ε_{SiO2}*($t_{ox}/\varepsilon_{ox}+t_{cen}/\varepsilon_{ch}$).

IV. CONCLUSION

In summary, we have successfully modeled and conducted a performance benchmarking analysis of the 3-D III-V InGaAs QW tri-gate transistor architecture with high-κ $TaSiO_x$ gate dielectric and scaled down to analyze the performance at a sub-10nm scale. The simulated $In_{0.53}Ga_{0.47}As$ tri-gate transistor exhibits superior gate electrostatic control with low OFF-state current (I_{OFF}) ~ 24.5 nA/μm, peak transconductance (g_m) ~ 2mS/ μm and high I_{ON}/I_{OFF} ratio ~ $2.3x10^3$. The novel oxide $TaSiO_x$ coupled with tri-gate architecture has the potential to exhibit superior electrostatics and is a potentially feasible option for future sub-10 nm alternate channel transistor technology.

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