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Research paper

Metal work function engineering on epitaxial (100)Ge and (110)Ge metal-oxide-semiconductor devices

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ABSTRACT

Capacitance-voltage characterization of epitaxial *n*-type (100)Ge and (110)Ge metal-oxide-semiconductor capacitors (MOS−Cs) was performed using two work function Al and Pt gate metals to evaluate the orientation effect on flat-band voltage (V_{FB}) shift, Fermi level pinning factor (S), and interface induced defects (D_{it}). These epitaxial (100)Ge/AlAs/GaAs and (110)Ge/AlAs/GaAs heterostructures were grown *in-situ* using two separate molecular beam epitaxy (MBE) chambers. A V_{FB} shift of > 700 mV, S > 0.5, and D_{it} value of ~ $6 \times 10^{11}\,cm^{-2}\,eV^{-1}$ in the energy range of 0.05 eV to 0.3 eV below the conduction band, have been demonstrated from epitaxial *n*-type (100)Ge and (110)Ge surfaces, which are comparable to the reported bulk Ge MOS-C values, suggesting a robust MOS-C developed process as well as device quality epitaxial (100)Ge and (110)Ge layers on GaAs substrates using an AlAs intermediate buffer. Thus, the metal work function engineering on device-quality MBE grown crystallographically oriented Ge materials, can offer a promising path for extending the performance and application of Ge-based field-effect transistors for low-power devices.

1. Introduction

The replacement of polysilicon gates with metal gates in silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFETs) at the 45 nm transistor node has engendered a lot of interest in the metal work function engineering of MOSFETs [1] for continued transistor miniaturization. For *n*-channel and *p*-channel MOSFETs, two distinct gate metals are generally used to accommodate for the difference between the metal work function, φ_m, and the semiconductor work function, φ_s (which differs for *n*- and *p*-type channels), φ_{ms}. φ_{ms} has a direct impact on the flat-band voltage (V_{FB}), which in turn affects the transistor threshold voltage (V_{TH}). However, the ability to tune V_{FB} using two different work function metals in a metal-oxide-semiconductor capacitor (MOS−C) configuration, and consequently V_{TH}, is limited by Fermi-level pinning (FLP) at the semiconductor's surface. This FLP stems from the formation of a dipole layer, shown in Fig. 1, originating from intrinsic surface states that have been filled due to the presence of charged interfacial defects [2] at the oxide/semiconductor heterointerface. The formation of an additional dipole layer at the metal/oxide heterointerface is also possible, corresponding to the well-described metal-induced gap states, *i.e.*, the filled intrinsic oxide surface states resulting from the evanescent coupling of the metal electron wave function and available oxide surface states. [3, 4] The influence of these dipole layers depends on the cumulative difference between φ_m and the charge neutrality level φ_{CNL} at the semiconductor surface, as shown in Fig. 1, where $E_{F,m}$ is the Fermi-level energy of the metal and E_{CNL} is the charge neutrality level (CNL) energy level, *i.e.*, the *effective* Fermi-level energy at the semiconductor surface. The interface dipole(s) that forms alters the interfacial band alignment, generating significant band bending at the semiconductor surface in order to equilibrate E_{CNL} and $E_{F,m}$, thereby altering φ_m and producing $\varphi_{m,eff}$, the effective metal work function. $\varphi_{m,eff}$ can be expressed by the following: [5]

$$\varphi_{m,eff} = \varphi_{CNL} + S(\varphi_m - \varphi_{CNL}) \quad (1)$$

where S is known as the Schottky pinning parameter, which ranges from 0 (full pinning) to 1 (no pinning). If MOS-C's implementing different gate metals [5–7] are fabricated from the same oxide/semiconductor structure, the difference in flat-band voltage, ΔV_{FB}, is now equivalent to the difference in $\varphi_{m,eff}$, *i.e.*, $\Delta\varphi_{m,eff}$. Correspondingly, Eq. (1) can be re-written in terms of ΔV_{FB}, S, and the difference in effective metal work functions:

$$\Delta V_{FB} = \Delta\varphi_{m,eff} = S\Delta\varphi_m \quad (2)$$

In this work, the integration of two different gate metals, platinum (Pt) and aluminum (Al), to form MOS-Cs on (100) and (110) crystallographically oriented epitaxial Ge heterostructures grown by solid

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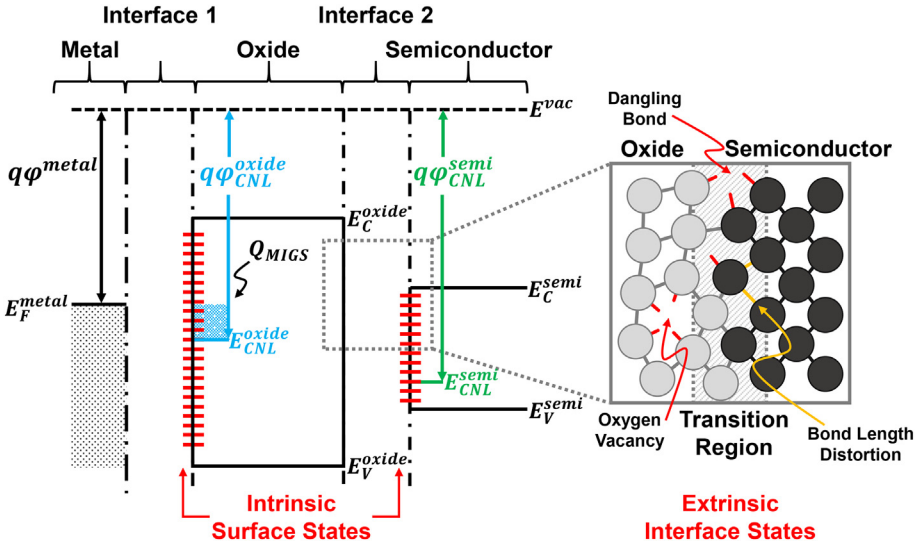

Fig. 1. Schematic energy band diagram of a metal-oxide heterointerface and the intrinsic interface states that form due to differing charge neutrality levels (CNLs) between the dissimilar materials (adapted from Ref. [5]). It also illustrates the intrinsic and extrinsic surface states at each heterointerface.

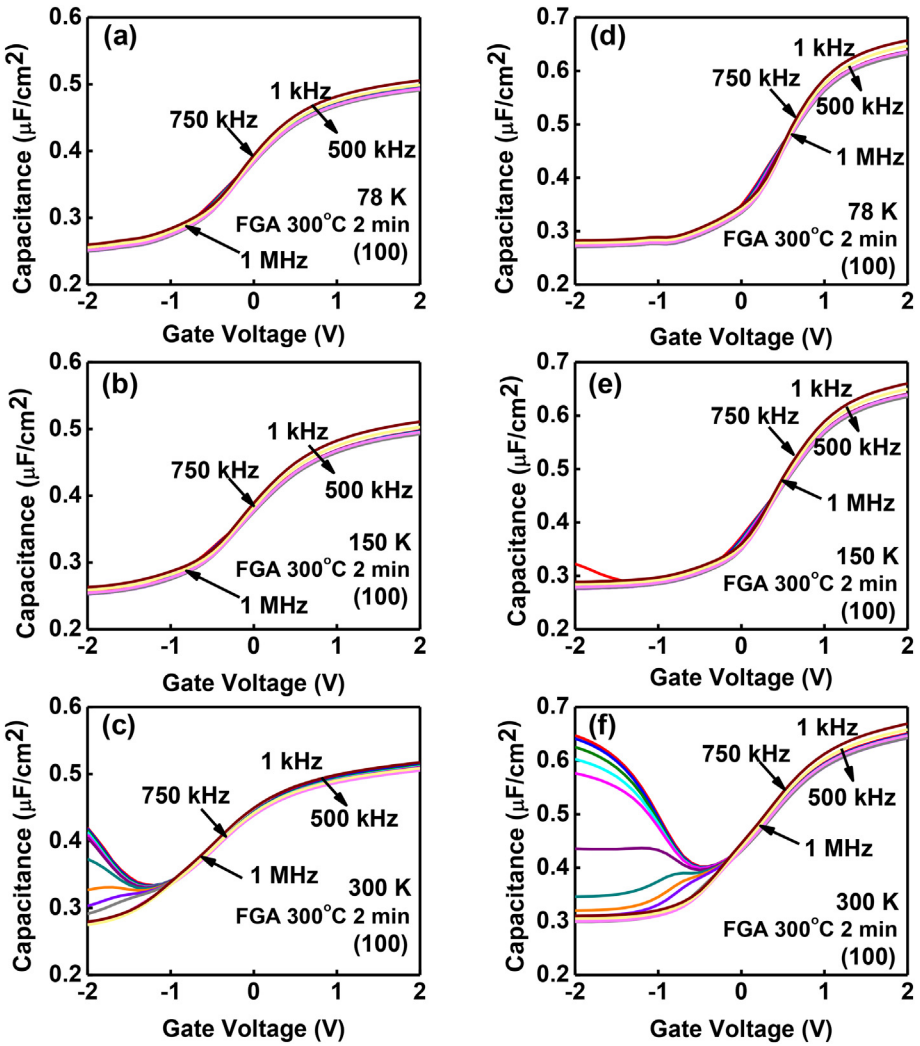

Fig. 2. C–V characteristics of the (100) Ge MOS-C on GaAs *via* an AlAs buffer architecture using two different gate metals. Devices with 100 nm Al/0.4 nm TiN measured at (a) 78 K (Ref. [10]), (b) 150 K and (c) 300 K. Devices with 60 nm Au/40 nm Pt/0.4 nm TiN measured at (d) 78 K, (e) 150 K and (f) 300 K.

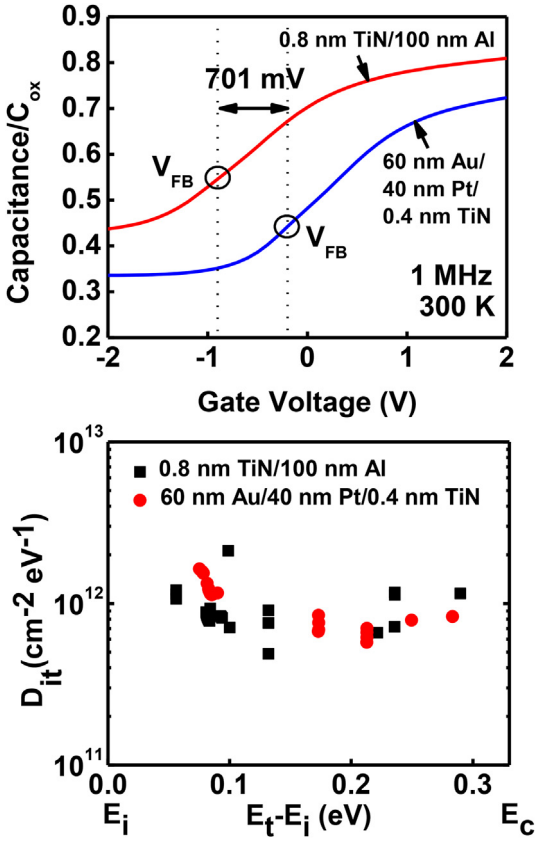

Fig. 3. (a) Comparison of the 1 MHz C–V curves measured at 300 K of the (100)Ge MOS-C on GaAs *via* an AlAs buffer architecture. Both curves are normalized to their respective oxide capacitance, C_{ox}. (b) D_{it} as a function of energy for Al and Pt gate metals of (100)Ge MOS-Cs on GaAs *via* an AlAs buffer architecture (D_{it} result for Al gate metal at 78 K and 150 K are taken from Ref. [10]).

source molecular beam epitaxy is investigated. Al and Pt metals were selected due to the large separation in their work functions (> 1.3 eV), thereby permitting an unambiguous extraction of ΔV_{FB}. Moreover, Al ($\varphi_m \sim 4.06$ eV) [8] and Pt (5.12 eV < φ_m < 5.93 eV) [8] can be considered as candidate *n*-MOS and *p*-MOS metals for future Ge FET applications, respectively.

2. Methods of preparation

The undoped (uid) *n*-type 270 nm (100)Ge and 270 nm (110)Ge epitaxial layers were grown by an *in-situ* growth process on epi-ready semi-insulating (100)GaAs (offcut 2° towards the [110] direction) and (110)GaAs substrates, respectively, with 170 nm AlAs buffers, using separate solid source molecular beam epitaxy chambers [9] for Ge and III-V materials connected *via* an ultra-high vacuum transfer chamber. [10–13] The epitaxial AlAs intermediate buffer layer at the Ge/GaAs heterointerface has been demonstrated to block the cross diffusion of Ge, Ga and As atoms [11–14] as well as reduce phosphorus-vacancy-related deep levels in GaInP/Ge systems, [15] and suppress the inter-diffusion of P atoms into the Ge substrate. [16] Substrate oxide desorption was carried out at ~680 °C under an arsenic overpressure of ~1 × 10^{-5} Torr in the III-V MBE chamber. During the substrate oxide desorption, GaAs layer growth, and subsequent Ge layer growth, reflection high-energy electron diffraction patterns were recorded for each step of the growth process. An initial 250 nm uid GaAs buffer layer followed by 170 nm uid AlAs was then deposited at 650 °C/630 °C under a stabilized As_2 flux in order to generate a smooth surface for (100)Ge/(110)Ge growth. The GaAs wafers were then transferred to the Ge MBE chamber (base pressure of 6×10^{-11} Torr) for Ge epilayer growth. During the Ge epilayer growth, the chamber pressure was ~2.9×10^{-8} Torr. The growth rate and the growth temperature of the Ge layer studied here were ~0.06 Å/s and 400 °C, respectively, with the growth rate being determined by cross-sectional transmission electron microscopy. The growth temperature referred herein is the thermocouple temperature. After each Ge epilayer growth, the substrate temperature was carefully reduced to ~50 °C at a ramp rate of ~4 °C/min prior to unload the sample from the chamber.

The crystallographically oriented epitaxial Ge/AlAs/GaAs heterostructures were characterized using x-ray diffraction to determine their structural properties, [12] atomic force microscopy to examine their surface morphology, [12] transmission electron microscopy to investigate their interfacial properties, [10] and finally their electrical behavior was characterized following MOS-Cs fabrication. The *p*-MOS-Cs were fabricated on both epitaxial (100) and (110) crystallographically oriented *n*-Ge/AlAs/GaAs heterostructures. Each sample was cleaned with a standard degrease process (*i.e.*, acetone, isopropanol and deionized H_2O) followed by removal of native oxides using diluted hydrofluoric acid (1:10 HF:H_2O). A native GeO_x interfacial passivating layer was grown *via* thermal oxidation at 450 °C for 40 min, followed by deposition of a 4 nm Al_2O_3 gate oxide at 250 °C by atomic layer deposition. Two different gate metals were selected: (i) 100 nm Al/0.4 nm TiN and (ii) 60 nm Au/40 nm Pt/0.4 nm TiN. The ultra-thin 0.4 nm TiN deposition was used as an adhesion layer and diffusion barrier between each gate metal and the Al_2O_3 gate dielectric. In addition, 0.8 nm TiN/100 nm Al/10 nm Ti/30 nm Ni was used as an Ohmic contact for all devices. All metals were deposited using a Kurt J. Lesker PVD250 electron beam deposition chamber [17]. Following metallization, all devices were annealed at 300 °C for 2 min in a forming gas ambient (95%N_2:5%H_2 volume ratio). To evaluate the electrical characteristics of the fabricated MOS–Cs, temperature dependent multi-frequency capacitance-voltage (C–V) and conductance-voltage measurements (biased from accumulation-to-inversion) were performed using an HP4284A precision LCR meter with frequencies ranging from 1 kHz to 1 MHz. Analysis of the collected electrical data allowed for investigation of the carrier recombination dynamics at the metal/oxide/semiconductor heterointerface and the flat-band voltage shift due to depinning of the Fermi level. Accurate measurements were obtained with the removal of series resistance, as discussed in Ref. [18]. The interface induced defects (D_{it}) distribution, density and ΔV_{FB} were then quantified following the extraction procedures reported elsewhere. [10, 19].

3. Results and discussion

Figs. 2(a), 2(b) and 2(c) show the C–V characteristics measured at 78 K [10], 150 K and 300 K, respectively, for the (100)Ge MOS-Cs with the 100 nm Al/0.4 nm TiN gate metal. Likewise, Figs. 2(d)–(f) show the C–V characteristics measured at 78 K, 150 K and 300 K, respectively, for the (100)Ge MOS-Cs using the 60 nm Au/40 nm Pt/0.4 nm TiN gate metal. Apart from the large shift in V_{FB} observed at all temperatures studied here, there is also a difference in maximum capacitance, C_{max}. This C_{max} difference is not due to oxide thickness variation since both samples underwent the same fabrication process, but rather, due to the oxidation of the Al metal during post deposition metal annealing. Fig. 3(a) shows the comparison of 1 MHz C–V curves at 300 K from the two different gate metals, where the red line denotes the sample with 100 nm Al/0.4 nm TiN and the blue line denotes the sample with 60 nm Au/40 nm Pt/0.4 nm TiN. These curves were normalized to their respective C_{ox} values. The difference in V_{FB} was measured to be ~701 mV. Using the measured ΔV_{FB} along with the work functions of Al (4.28 eV [20]) and Pt (5.65 eV[20]), Eq. (2) was used to estimate an *S* value of 0.512, which is the highest value reported to date for *n*-type Ge. [21–23] It has been reported that the work function of Pt gate metals is often less than that of elemental Pt with respect to the vacuum level (5.65 eV). [5, 24, 25] A wide range of tunable Pt work functions (from

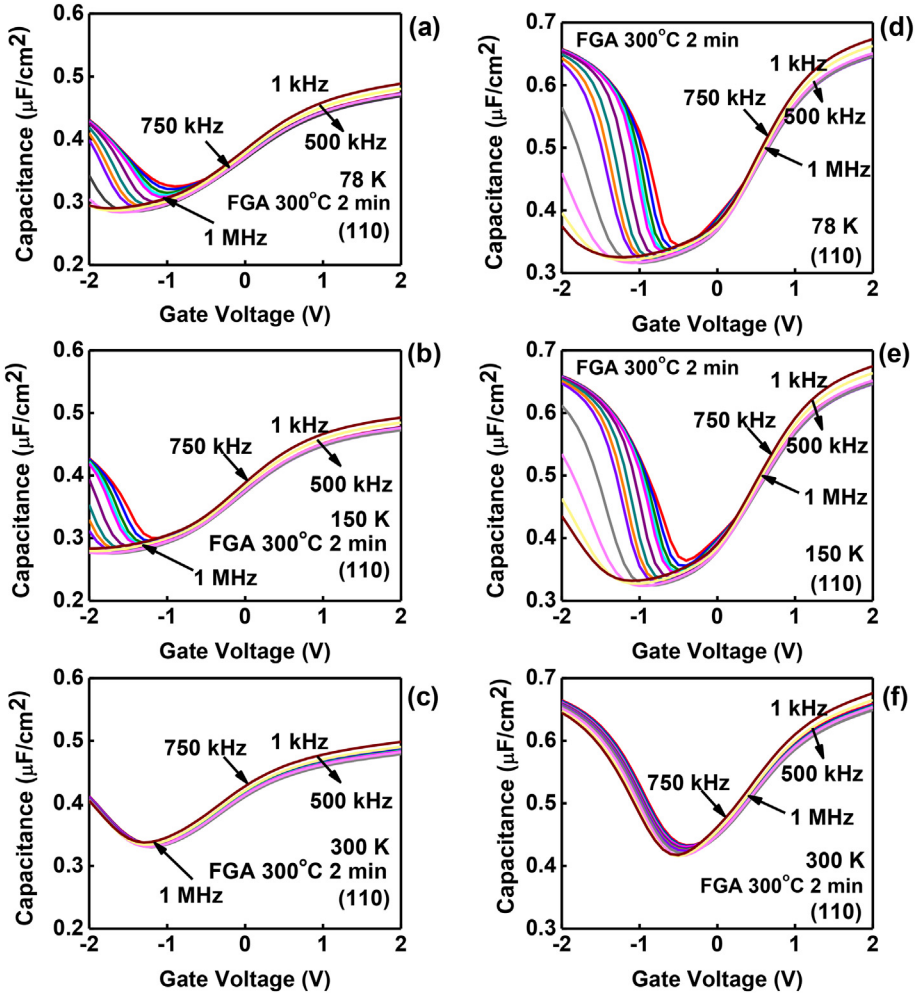

Fig. 4. C–V characteristics of the (110) Ge MOS-C on GaAs *via* an AlAs buffer architecture using two different gate metals. Devices with 100 nm Al/0.4 nm TiN measured at (a) 78 K (Ref. [10]), (b) 150 K and (c) 300 K. Devices with 60 nm Au/40 nm Pt/0.4 nm TiN measured at (d) 78 K, (e) 150 K and (f) 300 K.

4.24 eV to 4.98 eV) have been reported on HfO_2/*p*-Si structures, modified by both annealing conditions and the thickness of the HfO_2 layer. [26, 27] Thus, the *S* value reported here is a lower bound for the pinning parameter. A comparison of D_{it} values for the two different gate metals on (100)Ge devices is shown in Fig. 3(b), where D_{it} was calculated using the conductance method accounting for surface potential. [28, 29] Although the measured D_{it} levels are comparable to those found in some state-of-the-art devices, [30, 31] further reduction of D_{it} may allow for further Fermi-level unpinning and therefore, an improvement of *S*.

Figs. 4(a)–(c) show the C–V characteristics measured at 78 K, 150 K and 300 K, respectively, for the (110)Ge MOS-Cs using the 100 nm Al/0.4 nm TiN gate metal. Similarly, Figs. 4(d)–(f) show the C–V characteristics at 78 K, 150 K and 300 K, respectively, of the (110)Ge MOS-Cs for the 60 nm Au/40 nm Pt/0.4 nm TiN gate metal. Similar to the (100)Ge C–V curves shown in Fig. 2(a) through Fig. 2(f), there is a large shift in V_{FB} observed at all temperatures, as well as a difference in C_{max} between the studied gate metals. One can find from Fig. 4 that the (110)Ge MOS-Cs demonstrated unexpected inversion-like behavior at low overdrive voltage ($V_G - V_{TH}$) across all measurement frequencies, which was not the case for the (100)Ge MOS-Cs shown in Fig. 2. As shown in Fig. 4, only partial suppression of the inversion-like response was observed at cryogenic temperatures (78 K), as would be nominally indicated by the flattening of the high-frequency C–V curves under depletion and weak inversion bias. However, with the large shift in V_{FB} utilizing a Pt gate metal, it is revealed that: (i) minority carrier generation is not completely suppressed at 78 K; (ii) there exist shallow traps distributed throughout the Ge bandgap with sufficiently rapid relaxation times so as to respond to high frequency modulation; (iii) the shift in V_{FB} is sufficiently large so as to reveal the onset of tunneling-dominated gate leakage and the injection of charge into the gate structure; or (iv), a combination thereof. Fig. 5(a) shows the comparison of the 1 MHz curves of the two different-gated (110)Ge MOS-C samples at 300 K, where the red line denotes the sample with the 100 nm Al/0.4 nm TiN gate metal and the blue line denotes the sample with the 60 nm Au/40 nm Pt/0.4 nm TiN gate metal. These curves were normalized to their respective C_{ox} values. The difference in flat-band voltage, ΔV_{FB}, was measured to be ~ 816 mV. Using Eq. (2), an *S* value of 0.596 was estimated, which is slightly higher than the *S* value of 0.512 calculated for the (100)Ge MOS–Cs. Fig. 5(b) shows a comparison of D_{it} values between the two different-gated devices, again showing that the D_{it} values are comparable to state-of-the-art devices [30, 31]. Similar to (100)Ge MOS–C, further improvement in D_{it} would allow for additional unpinning of the Fermi level and an increase in *S*.

In the previous section, we have observed that the temperature dependent C–V curves show drastic discrepancies between (100)Ge and (110)Ge. This can be explain as follows: first, the energy range (within the Ge bandgap) that corresponds to our measurement temperatures extends from approximately 0.025 eV above/below midgap to 0.03 eV below/above the band edge. Second, we note that the suppression of minority carrier (thermal) generation at cryogenic measurement temperatures is responsible for the lack of an inversion-like

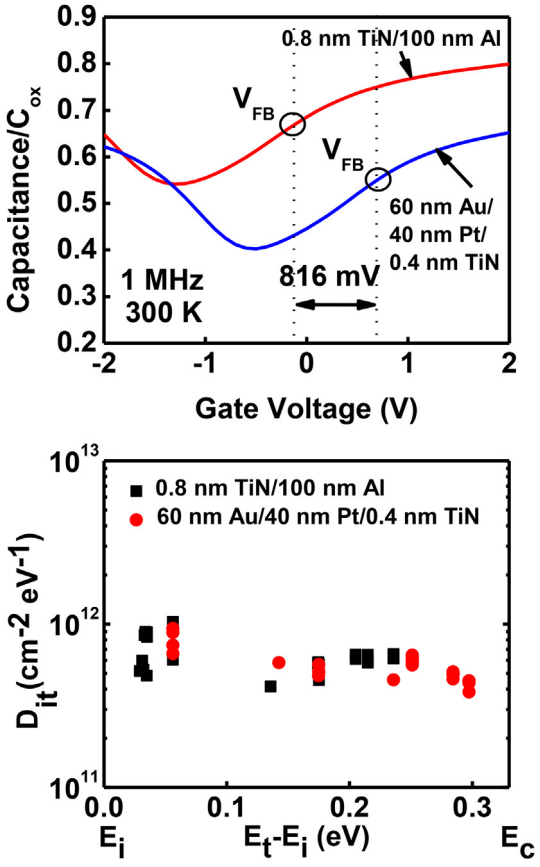

Fig. 5. (a) Comparison of 1 MHz C–V curves measured at 300 K of (110) Ge MOS-C on GaAs *via* an AlAs buffer architecture. Both curves are normalized to their respective oxide capacitance, C_{ox}. (b) D_{it} as a function of energy for Al and Pt gate metals of (110) Ge MOS-C on GaAs *via* an AlAs buffer architecture (D_{it} result for Al gate metal at 78 K and 150 K are taken from Ref. [10]).

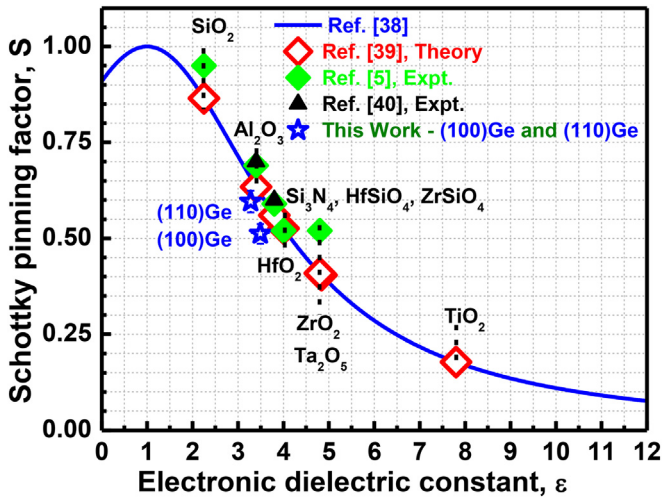

Fig. 6. Comparison of Schottky pinning parameters of oxides as a function of electronic dielectric constant, ϵ_∞, empirically modeled in Refs. [5, 38–40]. Experimentally determined pinning parameters are also included in this figure along with Al_2O_3/GeO_x gate stack used in this work for two different crystallographically orientated epitaxial (100)Ge and (110)Ge.

response in low-bandgap material systems measured as a function of decreasing temperature. However, defect states are understood to also generate an inversion-like response at high defect densities. We therefore posit that the inversion-like response observed on (110)Ge stems from an increasing defect density in close proximity to the band edge (shallow) yet outside of the energy window of our experimental measurement capabilities, as defined above. In addition, one can also find that the value of S is dependent on *both* the D_{it} as well as the dielectric screening of the material(s) of interest. Correspondingly, we have experimentally observed differences in the oxide dielectric (electronic) properties due to crystallographic orientation of Ge, as outlined in our previous work [10]. It is therefore feasible that the discrepancy in D_{it} and S for (100)Ge and (110)Ge stems from the experimentally observed differences in dielectric electronic quality, noting that as the electronic component of the dielectric constant increases, S decreases, *i.e.*, the two are inversely proportional, and that $\varepsilon_r^{(100)} \cong 3.5$ as compared to $\varepsilon_r^{(110)} \cong 3.3$.

It has been widely reported that the work function of metal depends on the atomic arrangement of atoms on the surface of a semiconductor [8] and hence the work function separation of these two metals. The metal work function engineering is more challenging on *n*-type Ge due to FLP and it was attributed due to metal-induced gap states. [3, 4] Nishimura et al. [6] have investigated 12 different work function metals ranging from 3.1 eV (Y) to 5.65 eV (Pt) on *n*-type (100)Ge and found that the Fermi level is pinned close to the valence band of *n*-type Ge, irrespective of the selected metals. Furthermore, they have found that FLP or pinning strength has no relation with the surface orientation of bulk (100)Ge, (110)Ge and (111)Ge materials, [32, 33]and the CNL is fixed to any surface orientation of bulk Ge. This FLP can only be modulated by insertion of a thin insulating layer in between the metal and the *n*-type Ge [34, 35]. However, the oxidizing species (*i.e.*, atomic oxygen, ozone, molecular oxygen) on the *n*-type (100) Ge surface dangling bonds can create different microstructure (*i. e,* Ge_2O_3, GeO_2, GeO), which can influence to the electrical properties of the GeO_2/Ge based MOS devices [36] as well as the FLP even with the insertion of any thin insulating layer. The measured Schottky pinning parameter value of > 0.5 and a ΔV_{FB} shift of ~700–800 mV using Pt and Al gate metals, indicating efficient Fermi level modulation on crystallographically oriented epitaxial (100) and (110)Ge MOS capacitors.

Lastly, we note that the Schottky pinning parameter, S, being a characteristic of the semiconductor, is given by: [5, 37–40]

$$S = \frac{1}{1 + \frac{(e^2 N\delta)}{(\varepsilon\varepsilon_0)}} \tag{3}$$

where e is the electronic charge, ϵ_o is the permittivity of free space, N is the density of intrinsic surface states per unit area, and δ is their extent into the semiconductor. In Eq. (3), N can also be pragmatically interpreted to represent the influence of all extrinsic and intrinsic electronic states at a surface or interface, such as metal-induced-gap states or defect-induced interface states. [39] Various models [37, 39] have been reported to describe the physical nature of such states in parallel with experimental studies on metal-semiconductor junctions. Mönch [38] showed that the $N\delta$ product is dependent on the electronic part of the dielectric constant, ϵ_∞, and scales with $(\epsilon_\infty - 1)^{1.9}$. Therefore, S, which accounts for dielectric screening, can be empirically shown to follow the relation, [5, 37–40]

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2} \tag{4}$$

where ϵ_∞ is the electronic part of the dielectric constant. Thus, the Schottky pinning factor depends on the permittivity of the oxide, density of electronically active surface/interface states per unit area and their extent into the semiconductor. Correspondingly, a value of S from 1 to 0 determines no pinning (S = 1) or full pinning (S = 0) at a semiconductor surface. The above empirical relation of S with ϵ_∞ for Al_2O_3/GeO_x oxide on crystallographically oriented Ge would provide evidence of whether the metal work function engineering herein is effective to shift the flat-band voltage as a function of crystallographic orientation. Fig. 6 shows the modeled Schottky pinning parameter, S, as

a function of the electronic dielectric constant along with experimental data for different high-κ dielectric. We note that the experimental dielectric constant for the combined GeO_x/Al_2O_3 composite gate oxide, extracted *via* combined TEM oxide thickness and C−V capacitance analysis, has been utilized; therefore, any difference in the oxide thicknesses or quality between the two orientations will be reflected in a differing dielectric constant value. Explicitly, the observed difference in dielectric constant (although minimal) is a result of the difference in experimental (i) GeO_x thickness and (ii) GeO_x quality between the two orientations, as detailed extensively in our previous work. [10] One can find from Fig. 6 that the pinning parameter values for the Al_2O_3/GeO_x gate stacks on (100)Ge and (110)Ge are closely predicted by Mönch's empirical model, which are found to be slightly smaller than the pinning parameter for Al_2O_3 on Si. [5, 39] The finite difference between the *S* parameters of these MOS devices suggests that the interface dipole layer formation, and hence extent of pinning, is indeed affected by the crystallographic orientation of the underlying semiconductor, [41] similar to the metal work-function dependence on the atomic arrangement of surface atoms at a metal-semiconductor junction. [8].

4. Conclusions

In summary, the electrical behavior of MOS-Cs using Al and Pt gate metals on crystallographically oriented epitaxial (100)Ge and (110)Ge was used to understand the orientation effect on the change in flat-band voltage, Fermi level pinning factor, and interface induced defect density. Epitaxial Ge layers were grown on GaAs substrates using an intermediate AlAs buffer layer *via* solid source molecular beam epitaxy. A flat-band voltage shift of > 700 mV and Fermi level pinning parameter S > 0.5 have been demonstrated for the *n*-type (100)Ge and (110)Ge MOS−Cs, which are 50% higher than those demonstrated on bulk Ge MOS-C devices reported to-date. [21–23] In addition, D_{it} values of $\sim 6 \times 10^{11}\ cm^{-2}eV^{-1}$ in the energy range of 0.05 eV to 0.3 eV below the conduction band, were demonstrated from *n*-type epitaxial (100)Ge or (110)Ge surfaces, which are comparable to the reported bulk Ge MOS-C value. Overall, the metal work function engineering on device-quality MBE grown crystallographically oriented Ge materials, can offer a promising path for extending the performance and application of Ge-based field-effect transistors for low-power devices.

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