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Interface states density distribution in Au/n-GaAs Schottky diodes on n-Ge and n-GaAs substrates

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Abstract

The current–voltage (I–V) and capacitance–voltage (C–V) characteristics of Au/n-GaAs Schottky diodes on n-Ge substrates are investigated and compared with characteristics of diodes on GaAs substrates. The diodes show the non-ideal behavior of I–V characteristics with an ideality factor of 1.13 and barrier height of 0.735 eV. The forward bias saturation current was found to be large (3×10^{-10} A vs. 4.32×10^{-12} A) in the GaAs/Ge Schottky diodes compared with the GaAs/GaAs diodes. The energy distribution of interface states was determined from the forward bias I–V characteristics by taking into account the bias dependence of the effective barrier height, though it is small. The interface states density was found to be large in the Au/n-GaAs/n-Ge structure compared with the Au/n-GaAs/n^+-GaAs structure. The possible explanation for the increase in the interface states density in the former structure was highlighted. © 2001 Published by Elsevier Science B.V.

Keywords: Current–voltage (I–V); Capacitance–voltage (C–V); Schottky diodes

1. Introduction

A Schottky diode, fabricated from polar material grown on a non-polar substrate, often faces the problem of antiphase domains inside the polar material as well as cross-diffusion at the heterointerface. The electrical transport in Schottky diodes on epi-GaAs grown on Ge substrates has been of considerable interest due to the widespread application of such devices in microwave field effect transistors (FETs), radio-frequency (RF) detectors, and solar cells. In general, the performance and reliability of a Schottky diode is drastically influenced by the interface quality between the deposited metal and the semiconductor surface. The performance and reliability of Schottky microwave devices (MESFETs, detectors, mixers, and varactor diodes) depends on the density of interface states as well as the distribution of such states.

The effect of the presence of both thin and thick interfacial layers and the interface states on the current–voltage (I–V) and capacitance–voltage (C–V) characteristics of Au/n-GaAs Schottky diodes on GaAs has been studied by several authors, although little work has been reported for the specific case of GaAs grown on Ge substrates by metal–organic vapor-phase epitaxy (MOVPE). A diode structure consisting of Au/n-GaAs over Ge often gives a higher ideality factor, lower barrier height, and a soft breakdown voltage due to the misfit dislocations formed inside the GaAs substrate during the heteroepitaxial growth process [1]. Unless the MOVPE growth parameters are precisely controlled, the epi-GaAs over Ge often gives antiphase domains and misfit dislocations, which gives rise to poor electrical transport characteristics [2–7]. In fact, the grown GaAs epilayer over Ge might contribute to the high density of surface states, which increases the surface recombination velocity, decreases the minority carrier lifetime, and increases the leakage at the junction, all of which worsening the GaAs/Ge solar cell performance [6,7].

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This work is an attempt to investigate the detailed electrical transport properties of GaAs Schottky diodes on Ge substrate using forward bias I–V characteristics and reverse bias C–V measurements. The density of interface states was evaluated for the Au/n-GaAs Schottky diode on Ge substrate grown by MOVPE technique using the formula predicted by Card and Rhoderick [8]. Finally, the density of interface states was evaluated for the Au/n-GaAs Schottky diode on GaAs substrate grown by MOVPE technique and compared with Au/n-GaAs/Ge Schottky diodes.

2. Method of analysis

When a metal-semiconductor (MS) contact with an interfacial layer is considered, it is assumed that the forward bias current in a Schottky barrier is due to thermionic emission current corrected by tunneling, which is expressed [8] as

$$I = aA^{**}T^2\exp(-\chi^{0.5}\delta)\exp\left(-\frac{q\Phi_{bo}}{kT}\right)\exp\left(\frac{qV}{nkT}\right) \quad (1)$$

where A^{**} is the Richardson constant, a is the diode area, Φ_{bo} is the zero-bias barrier height, and χ is the mean barrier height presented by the thin interfacial layer of thickness δ. The term $\exp(-\chi^{0.5}\delta)$ is commonly known as the transmission coefficient across the thin interfacial layer. Eq. (1) is valid only for forward biases $V > kT/q$ since the reverse current contribution (due to electrons tunneling from the metal into the semiconductor) has been neglected.

The voltage dependence of the effective barrier height Φ_e, is contained in the ideality factor n through the relation [9]

$$\frac{d\Phi_e}{dV} = \beta = 1 - \frac{1}{n} \quad (2)$$

where β is the voltage coefficient of Φ_e. The effective barrier height is given by [9]

$$\Phi_e = \Phi_{bo} + \beta dV. \quad (3)$$

For metal–insulator–semiconductor (MIS) diode having interface states in equilibrium with the semiconductor, the ideality factor n becomes greater than unity, as proposed by Card and Rhoderick [8], and is given by

$$n = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{W} + qN_{ss}\right) \quad (4)$$

where W is the space charge width, N_{ss} is the density of the interface states and ε_s and ε_i are the permittivities of the semiconductor and the interfacial layer, respectively.

The evaluation of the interface state energy distribution and relative interfacial layer thickness can be performed using the formula derived by Card and Rhoderick [8] and Kolnik and Ozvold [10]. In the case where all of the interface states are in equilibrium with the semiconductor when the diode is forward biased, while in the reverse direction the change of the interface state charge is negligible. The interfacial layer thickness has been evaluated from I–V and C–V measurements by several authors [11–14]. We have determined the value of δ/ε_i from the following equation [10,15].

$$\frac{\delta}{\varepsilon_i} = \left[\frac{\varepsilon_s}{W}\left(\frac{1}{\beta_r} - 1\right)\right]^{-1} \quad (5)$$

where $\beta_r = (kT/q)(d(\ln J)/dV)$ is the slope of the reverse bias I–V characteristics. Therefore, the interfacial layer thickness δ can be evaluated using the interfacial layer permittivity, $\varepsilon_i = 3.5\varepsilon_o$ [16].

In an n-type semiconductor, the energy of the interface states with respect to the bottom of the conduction band at the surface of the semiconductor, E_{ss}, is given by [17–23]

$$E_c - E_{ss} = q(\Phi_e - V). \quad (6)$$

Eqs. (2)–(6), along with the I–V characteristics (forward and reverse direction), can be used for the determination of the interface states density as a function of interface states energy E_{ss}.

3. Experimental procedure

The Au/n-GaAs Schottky diodes were fabricated on HCl/H_2O (1:1) etched Si-doped GaAs epitaxial films (3 μm), grown by low-pressure metal-organic vapor-phase epitaxy (LP-MOVPE) on n-Ge (2×10^{17} cm^{-3}) and n^+-GaAs (2×10^{18} cm^{-3}) substrates, (100) 2° off-oriented towards the [110] direction. The details of the growth procedure can be found elsewhere [24–26]. The back ohmic contact was made depositing Au: Ge and an overlayer of Au and annealing at 450 °C for approximately 2 min in an ultra-high pure (UHP) N_2 flow. It is well known that layer-by-layer growth of native oxide, which is inevitably present on the chemically prepared semiconductor surface, occurs when it is exposed to clean room air [8,19,27–31]. The Schottky contacts were formed by evaporating Au dots of approximate diameter of 400 μm onto mirror smooth surfaces of Si-doped GaAs epitaxial layers grown on Ge and GaAs substrates. All the evaporation processes were carried out in a vacuum coating unit at a pressure of approximately $2–3 \times 10^{-6}$ mbar. The dark I–V and C–V measurements of the samples were performed at 300 K.

4. Results and discussion

4.1. Current–voltage (I–V) characteristics

Fig. 1 shows the experimental forward bias I–V characteristics of the Au/n-GaAs/n-Ge (D1) and Au/n-GaAs/n$^+$-GaAs (D2) samples. The values of 1.13, 0.735 eV and 1.08, 0.838 eV for the ideality factor n and the zero-bias barrier height Φ_{bo} of diodes D1 and D2, respectively were obtained from the linear regions of the forward bias I–V plots, since the effect of series resistance in these linear regions is not significant. It has been reported [8,19,28,29,31] that an effective interfacial layer of non-zero thickness must exist between the metal and semiconductor even when both are in intimate atomic contact. Films of thickness of 10–25 Å usually lead to values of the ideality factor in the range of 1.18–1.30 [8,18,28].

Usually, the forward bias I–V characteristics are linear on a semilogarithmic scale at low forward bias voltages but deviate considerably from linearity due to the effect of series resistance, the interfacial layer, and the interface states when the applied voltage is sufficiently large. The series resistance R_s is significant in the downward curvature (non-linear region) of the forward bias I–V characteristics, but the other two parameters are significant in both the linear and non-linear regions of the I–V characteristics. The lower the interface states density and the series resistance, the greater the range over which the I–V curve yields a straight line [9]. As the linear range of the forward I–V plots is reduced, the accuracy of the determination of Φ_{bo} and n becomes poorer. Here, the ideality factor and the series resistance were evaluated using a method developed by Cheung [32] in the high current range where the I–V characteristic is not linear. The ideality factor and the series resistance were found to be 1.17 and 9 Ω for diode D1, and 1.15 and 5 Ω for diode D2, respectively by using the formula

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right). \tag{7}$$

Thus, it is clearly seen that the value of 1.174 for n obtained from the downward curvature region, series resistance and interface state dominated region is greater than the value of 1.13 obtained from the linear region of the I–V characteristics of diode D1. Not only does series resistance contribute to the deviation from linearity in this region, but also the barrier height in this region becomes bias dependent due to the voltage drop across the interfacial layer and the change of occupied interface states with bias in this concave region of the I–V plot [19].

The downward curvature in the I–V characteristic at high forward bias values is attributed to a continuum of surface states, which are in equilibrium with the semiconductor, apart from the effect of R_s. The interface states energy distribution can thus be determined from the data of this region from the forward bias I–V in Fig. 1. This distribution can be obtained by taking into account the bias dependence of the ideality factor and barrier height, as was mentioned in Eqs. (2) and (3). If we subtract the effect of series resistance in the forward bias I–V characteristic, then the I–V characteristics presented in Fig. 1 show a straight line which has been replotted as a dotted line in Fig. 1 for both of the diodes. The calculated density of interface states determined from this dotted line I–V characteristic, plotted versus E_{ss} is a constant value. However, the actual density of interface states is expected to be higher than this calculated value, since some of the subtracted curvature should be attributable to surface states, rather than series resistance. The I–V data of diodes D1 and D2 shown in Fig. 1 fit well to the equations

$$\text{D1} \qquad I = 3 \times 10^{-10}\exp\left(\frac{qV}{nkT}\right) \tag{8}$$

and

$$\text{D2} \qquad I = 4.32 \times 10^{-12}\exp\left(\frac{qV}{nkT}\right), \tag{9}$$

respectively (solid lines), with the n values given in Table 1 (also plotted in Fig. 1), where 3×10^{-10} A and 4.32×10^{-12} A are the saturation currents of diodes D1

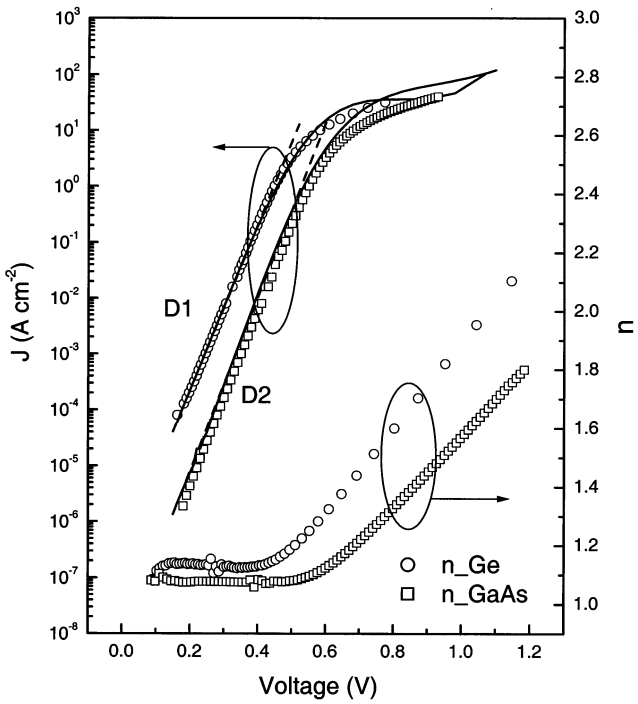

Fig. 1. The current density and ideality factor vs. voltage characteristics of Au/n-GaAs/n-Ge (D1) and Au/n-GaAs/n$^+$-GaAs (D2) diodes at 300 K. The solid line represents the best fit of the experimental values of current to Eqs. (6) and (7) with the reverse saturation current $I_o = 3 \times 10^{-10}$ A and $I_o = 4.32 \times 10^{-12}$ A for D1 and D2 diodes, respectively. The voltage dependence of the ideality factor of both diodes are also shown in this figure.

Table 1
Interface state energy distribution obtained from the forward bias I–V characteristics at 300 K

Au/n-GaAs/n-Ge (D1)					Au/n-GaAs/n-GaAs (D2)				
Voltage (V)	n	Φ_e (eV)	$E_c - E_{ss}$ (eV)	$N_{ss} \times 10^{16}$ ($eV^{-1}m^{-2}$)	Voltage (V)	n	Φ_e (eV)	$E_c - E_{ss}$ (eV)	$N_{ss} \times 10^{16}$ (eV^{-1} m^{-2})
0.182	1.12	0.802	0.620	3.350	0.18	1.08	0.985	0.805	0.908
0.205	1.14	0.802	0.600	3.900	0.20	1.07	0.985	0.785	0.617
0.225	1.14	0.802	0.577	3.841	0.25	1.08	0.985	0.735	0.463
0.246	1.14	0.801	0.555	3.936	0.30	1.08	0.985	0.685	0.505
0.266	1.14	0.801	0.535	3.894	0.35	1.07	0.985	0.635	0.497
0.285	1.13	0.802	0.517	3.715	0.40	1.07	0.985	0.585	0.476
0.305	1.13	0.801	0.496	3.685	0.45	1.08	0.985	0.535	0.400
0.324	1.13	0.802	0.478	3.532	0.50	1.09	0.985	0.485	0.507
0.344	1.13	0.802	0.448	3.508	0.55	1.12	0.985	0.435	0.718
0.364	1.13	0.815	0.437	3.486	0.60	1.17	0.986	0.386	1.195
0.384	1.13	0.801	0.417	3.467	0.65	1.23	0.986	0.336	1.943
0.404	1.12	0.802	0.390	3.497	0.70	1.30	0.986	0.286	2.849
0.425	1.13	0.802	0.377	3.565	0.75	1.37	0.987	0.237	3.837
0.448	1.14	0.802	0.354	3.801	0.80	1.44	0.987	0.177	4.871
0.475	1.15	0.802	0.327	4.353	0.85	1.51	0.988	0.138	5.931
0.510	1.19	0.803	0.293	5.482	0.88	1.55	0.988	0.108	6.931
0.560	1.25	0.805	0.245	7.649	0.89	1.57	0.988	0.098	6.774
0.641	1.38	0.811	0.170	11.894	0.90	1.58	0.988	0.088	6.987
0.679	1.44	0.814	0.135	14.023	0.91	1.59	0.988	0.078	7.200
0.723	1.51	0.818	0.095	16.522	0.92	1.61	0.988	0.068	7.411
0.774	1.60	0.823	0.049	19.450	0.93	1.62	0.988	0.058	7.626

Φ_{bo} (C–V) = 0.800 eV for diode D1 and Φ_{bo} (C–V) = 0.985 eV for diode D2.

and D2, respectively. The saturation current of D2 is almost two orders of magnitude less than the saturation current of diode D1. The increase in the saturation current of the Schottky diodes grown on the Ge substrate compared with the Schottky diode on the GaAs substrate gives rise to a lower open circuit voltage (V_{oc}) and a lower fill factor, which reduces the efficiency of the GaAs/Ge heterojunction solar cell. Hence, it is of technological importance to study and understand the current transport mechanism across a GaAs Schottky diode on Ge substrate.

Fig. 2 shows the reverse bias I–V characteristics of the D1 and D2 Schottky diodes. From the reverse bias characteristics, we have calculated an interfacial layer thickness of 5.74 Å for diode D1 and 12.9 Å for diode D2, respectively, using Eq. (5) and $\varepsilon_i = 3.5\varepsilon_o$. These values were used for the determination of the interface state density of diodes D1 and D2. The extrapolated reverse current of diode D1 is higher than that of diode D2. Ideally, the saturation currents for forward and reverse bias characteristics should be the same. This difference could be due to the effect of interfacial layer thickness, which converts the MS diodes into MIS diodes.

4.2. Capacitance–voltage (C–V) characteristics

Reverse bias capacitance measurements are typically made at a very high frequency ($\sim$1 MHz), so that the interface states are unable to respond to the AC signal. In order to assess the doping concentration and barrier height, C^{-2} versus V_R plots for diodes D1 and D2 (Fig. 3) were obtained from the C–V characteristics (measured at 1 MHz frequency). The C–V relationship applicable to intimate MS Schottky barriers on uniformly doped materials can be written as [28]

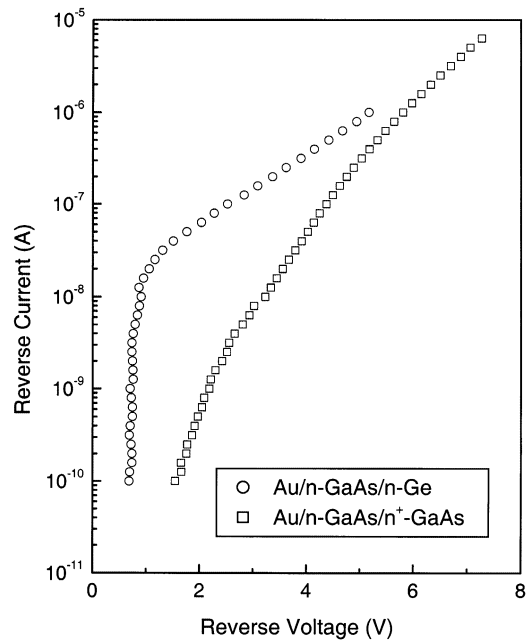

Fig. 2. Reverse bias I–V characteristics of diodes D1 and D2.

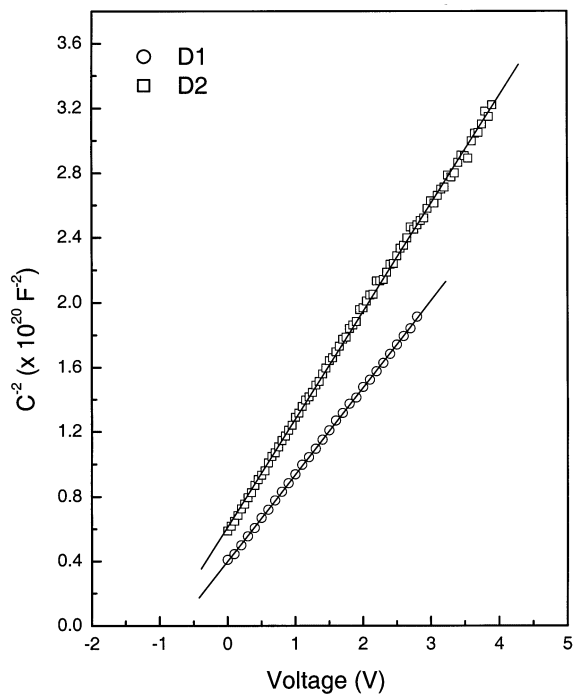

Fig. 3. C^{-2} against V for diodes D1 and D2.

Table 2
Typical parameters of Au/n-GaAs/n-Ge and Au/n-GaAs/n^+-GaAs

Parameter	Au/n-GaAs/n-Ge	Au/n-GaAs/n^+-GaAs
Oxide thickness, δ (Å)	5.74	12.9
Ideality factor, n	1.13	1.08
Saturation current, I_s (A) from forward bias I–V characteristics	3×10^{-10}	4.32×10^{-12}
Reverse saturation current (A) from reverse bias I–V characteristics	1×10^{-10}	1×10^{-8}
Barrier height, Φ_{bo}^{I-V} from I–V characteristics	0.735	0.838
Barrier height, Φ_{bo}^{C-V} from C–V characteristics	0.800	0.985
Zero-bias capacitance (pF)	156.36	130.5
Diode contact area (cm^2)	1.25×10^{-3}	1.25×10^{-3}
Depletion layer width (Å)	906	1090
Slope of C^{-2} vs. V plot (F^{-2} V^{-1})	5.37×10^{19}	6.66×10^{19}
Apparent doping concentration (cm^{-3})	1.3×10^{17}	1.06×10^{17}
C^{-2} vs. voltage intercept, V_o (V)	0.742	0.920

$$\frac{1}{C^2}=\frac{2(V_R+V_o)}{q\varepsilon_s N_D a^2} \tag{10}$$

where V_R is the reverse bias voltage, V_o is the built-in voltage, q is the electronic charge, and N_D is the doping concentration. The diffusion potential or built-in potential is usually measured by extrapolating the C^{-2}–V plot to the V-axis. An insulating film can modify these characteristics if the potential across the film changes with bias. The zero-bias barrier height determined from C–V measurements is defined by

$$\Phi_{bo}=V_o+\frac{kT}{q}+\Phi_n \tag{11}$$

where Φ_n is the Fermi energy measured from the conduction band edge. Similarly, the zero bias barrier height and the doping concentration were determined for the diode D2.

The doping concentration and the zero-bias barrier for diode D1 were 1.3×10^{17} cm^{-3} and 0.800 eV and for diode D2 were 1.06×10^{17} cm^{-3} and 0.985 eV, respectively. The zero-bias barrier height obtained from the I–V characteristic is less compared with that obtained from the C–V measurement for the diodes, as expected. The linearity of C^{-2}–V plot at this frequency indicates that the interface states and the inversion layer charge cannot follow the AC signal at this high frequency and consequently do not contribute appreciably to the diode capacitance. We did not observe any frequency dispersion in the frequency range of 1 kHz^{-1} MHz in either diode D1 or diode D2. The salient parameters of the D1 diode and the reference D2 diode are listed in Table 2.

4.3. Determination of interface state density (N_{ss})

Substituting the values of the voltage dependence of n from Table 1 in Eq. (4), and using $\varepsilon_s=12.8\varepsilon_o$ [28], $\varepsilon_i=3.5\varepsilon_o$ [16], $\delta=5.74$ Å (from reverse bias I–V characteristics), $W=906$ Å (from zero bias capacitance of C–V measurement) for diode D1 and $\delta=12.9$ Å (from reverse bias I–V characteristics), $W=1090$ Å (from zero bias capacitance of C–V measurement) for diode D2, the values of N_{ss} as a function of V were obtained and are given in Table 1. The resulting dependence of N_{ss} was converted to a function of E_{ss} using Eq. (6). N_{ss} versus E_c-E_{ss} is also shown in Table 1 and Fig. 4. The evaluated density of interface states in both of the diodes is a little higher than the value at the interface because we have not considered the effect of R_s in the calculation of N_{ss}. In the forward bias case, the increase of the effective barrier height Φ_e of both of the diodes with bias can be understood as follows: when the diode is forward biased, the quasi-Fermi level (imref) for the majority carriers rises on the semiconductor side. Thus, most of the electrons will be injected directly into the metal forming a thermionic emission current, while some of them are trapped by the interface states. This charge captures process results in an in-

crease in the effective barrier height, thereby reducing the diode current [9,16,20,33].

From Fig. 4 it can be seen that an exponential increase of the interface states density exists from midgap towards the bottom of the conduction band. This rise is less significant for diode D2 compared to diode D1. At any specific energy, the interface states density of diode D2 is less than that of diode D1. This case can be attributed to the fact that diode D2 has a thicker oxide layer (12.9 Å) than diode D1 (5.74 Å), because the dangling bonds on the GaAs surface on the GaAs substrate saturate. The increase in interface states density on the Ge substrate could be due to the defects originating from the heteroepitaxy. However, our recent study [34] on the temperature dependence of the ideality factor and the barrier height of the Au/n-GaAs Schottky diode on the Ge substrate in the temperature range of 80–300 K shows that there are no detectable electrically active defects present inside the GaAs epitaxial film. The shape of the density distribution of the interface states is in the range of $E_c - 0.05$ eV to $E_c - 0.70$ eV. Even if the quality of the GaAs epitaxial layer on the Ge substrate shows an excellent surface, good structural characteristics, and good luminescence properties, however, the electrical transport characteristics are expected to give a better picture of the film quality.

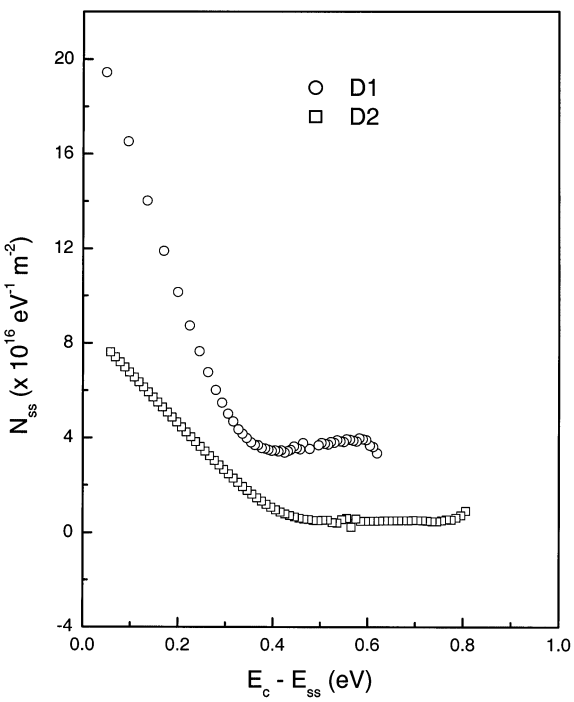

Fig. 4. Density of interface states as a function of $E_c - E_{ss}$ of diodes D1 and D2.

5. Conclusions

Au Schottky diodes were fabricated on n-GaAs epitaxial film at a donor concentration of 1.3×10^{17} cm^{-3}, with a thin 5.74 Å oxide layer on 2° off-oriented Ge substrate. The Au Schottky diodes were made on an epitaxial n-GaAs on GaAs substrate for the reference sample. The current conduction mechanisms across both of the diodes were carried out using $I-V$ and $C-V$ measurements. The non-ideal forward bias $I-V$ behavior observed in the Au/n-GaAs Schottky diodes were attributed to a change in the metal–semiconductor barrier height due to the interfacial layer, interface states, and the series resistance. The saturation current is high in the GaAs/Ge system compared with the GaAs/GaAs system. The bias dependent barrier height, though it is small, is considered for the determination of the interface state density distribution. The interface state density is large in the GaAs/Ge system compared with the GaAs/GaAs system. Hence, it is of technological importance to study the interface state density distribution, especially for the GaAs/Ge heterostructure solar cells.

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