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TBAL: Tunnel FET-Based Adiabatic Logic for Energy-Efficient, Ultra-Low Voltage IoT Applications

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ABSTRACT A novel, tunnel field-effect transistor (TFET)-based adiabatic logic (TBAL) circuit topology has been proposed, evaluated and benchmarked with several device architectures (planar MOSFET, FinFET, and TFET) and AL implementations (efficient charge recovery logic, 2N-2N2P, positive feedback adiabatic logic) operating in the ultra-low voltage ($0.3\ \text{V} \geq V_{DD} \leq 0.6\ \text{V}$) regime. By incorporating adiabatic logic functionality into standard combinational logic, an 80% reduction in energy/cycle was achieved. A further 80% reduction in energy/cycle was demonstrated by utilizing near broken-gap TFET devices and simultaneous scaling of supply voltage to 0.3 V, resulting in a 96% reduction in energy/cycle as compared to conventional Si CMOS. Extension of operating frequency beyond 10 MHz, coupled with sub-threshold circuit operation, shows the feasibility of TBAL for energy-efficient Internet of Things applications.

INDEX TERMS Adiabatic logic, FinFETs, strained Ge/InGaAs heterojunctions, tunnel field-effect transistors, TBAL.

I. INTRODUCTION

With the proliferation of connected computing devices into consumer, medical, and communication application spaces (*i.e.*, the Internet of Things, IoT), device-circuit co-design has become increasingly relevant to the development of energy-efficient embedded electronics. Similarly, power dissipation has become a key issue for portable and embedded systems in which supply power is limited due to limited battery lifetimes. An effective approach to reduce power dissipation has been a continual reduction in supply voltage, thereby quadratically scaling active power dissipation. However, as state-of-the-art silicon (Si) CMOS devices enter sub-threshold operation in the ultra-low supply voltage regime, their drive current is noticeably degraded. Consequently, additional transistors must be incorporated in order to maintain low voltage circuit functionality [1]–[4]. As a result of the large number of functional blocks in modern integrated circuits (ICs), these extra transistors contribute to significant additional power dissipation, thereby nullifying the benefits gained from supply voltage reduction. However, irrespective of supply voltage reduction, a theoretical bound to the minimum required energy consumption for a single computation operation exists. Based on Landauer's principle [5], a corresponding entropy is needed to complete any logically irreversible manipulation of information, such as bit erasure. The energy loss associated with such an operation is $kTln2$ (Joule), where k is Boltzmann's constant and T is the temperature. However, current combinational logic operates at energy expenditures three orders of magnitude in excess of Landauer's limit [6]. Thus, a new form of energy-efficient logic must be introduced in order to solve the fundamental problem of power management.

Adiabatic logic is an alternative approach to conventional combinational logic wherein a logical operation is, ideally, a reversible adiabatic process. Consequently, the energy consumption per function is scaled in proximity to Landauer's limit. Given sufficient time, the change in energy level in an adiabatic logic circuit is significantly lower than that of conventional combinational logic, leading to almost no energy dissipation. Within the adiabatic

regime, there are two types of logical operations: reversible and partially adiabatic. Although reversible adiabatic logic is attractive from the standpoint that it is a fully adiabatic process, partial adiabatic logic remains more practical due to its simplicity and lower spatial footprint. Furthermore, partial adiabatic logic operates efficiently at frequencies below 1 GHz, making it a suitable candidate for IoT applications demanding moderate frequency requirements (*e.g.*, RFID ~13.56 MHz) [4], [7], [8].

Lastly, in the ultra-low voltage regime (V_{DD} < 0.5 V), thermionic injection-based devices (*i.e.*, standard MOSFETs, BJTs) [9]–[12] operate in the sub-threshold regime, resulting in the failure of functional blocks due to insufficient FET drive current. Recently, tunnel field-effect transistors (TFETs) have been proposed [13], [14] for ultra-low voltage operation due to their low threshold voltage (V_{th}), low OFF-state leakage (I_{OFF}), and applicability to both logic and memory circuits [15], [16]. Hence, in this work, we introduce TFET-based adiabatic logic (TBAL) in order to demonstrate energy-efficient logic building blocks operating under ultra-low supply voltage. This approach leverages the steep sub-threshold dynamics of TFETs with the energy efficiency of adiabatic logic to achieve low energy/cycle logic functionality, thus providing an effective solution for the realization of future ultra-low voltage IoT ICs.

II. DEVICE CHARACTERISTICS AND TBAL CELL DESIGN

A. TFET, FINFET, AND MOSFET OPERATING CHARACTERISTICS

In this work, heterojunction TFETs (H-TFETs) were used to evaluate the performance of competing adiabatic logic implementations operating at or below 0.6 V supply voltage. TFETs can be described as gated *p-i-n* diodes in which the gate, residing over the channel, controls the tunneling probability at the source/channel junction through an applied gate voltage. The electrons (or holes) tunneling from source-to-channel experience a heterostructure-dependent tunneling barrier, thereby affecting their tunneling probability and hence the device current. The detailed TFET device simulation methodology utilized herein can be found in our previously reported work [13]. Due to their asymmetric device structure, TFETs also exhibit unidirectional behavior, as illustrated in Fig. 1. From Fig. 1, one can find that drain current is limited to leakage current with reverse bias application for both *p*- and *n*-TFETs. Consequently, one must account for the unidirectionality of TFETs when designing TFET-based adiabatic logic circuits. Thus, in this work, we will propose a solution to overcome the unidirectional nature of TFETs and realize functional TFET-based adiabatic logic.

Furthermore, in order to investigate the performance impact of TFET design on adiabatic logic circuit operation, both staggered-gap (SG) and near broken-gap (NBG) TFETs were considered in this work. In these TFETs, the effective tunneling barrier height, E_{beff}, is described by the energy band alignment at the source/channel interface and plays a key role in determining ON- and OFF-state current. For

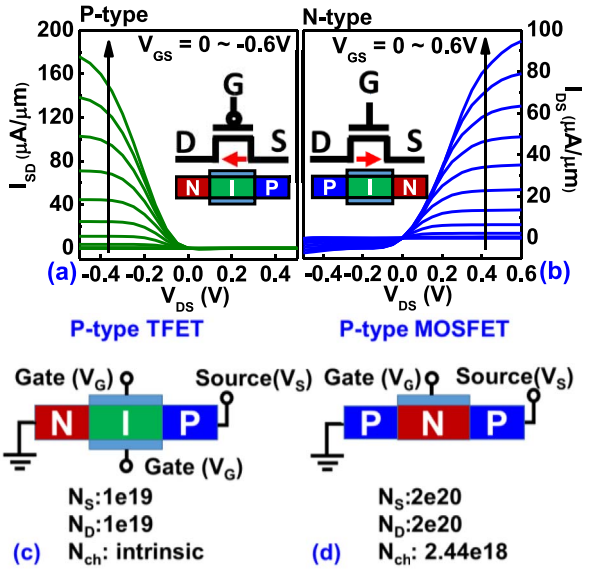

FIGURE 1. (a-b) Output characteristics of strain and bandgap engineered staggered-gap Ge/InGaAs *p*- and *n*-TFETs exemplifying their unidirectional nature. (c-d) An example schematics for p-type TFET and MOSFET.

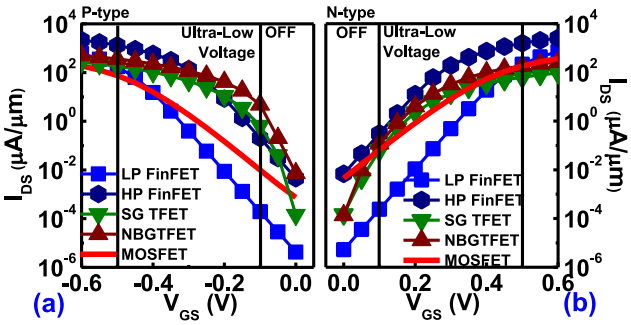

FIGURE 2. I_{ds}-V_{GS} characteristics ($|V_{DS}|$ = 0.6 V) for the *p*- and *n*-type FETs.

SG TFETs, E_{beff} is smaller than the bandgap of either source or channel material. On the other hand, for NBG TFETs, E_{beff} approaches zero. Fig. 2 highlights the drain current versus gate voltage (I_{DS}-V_{GS}) characteristics of *n*- and *p*-type 45 nm high-performance (HP) MOSFETs [17], 20 nm low-power (LP) FinFETs [17], 20 nm HP FinFETs [17], strain and bandgap engineered SG TFETs (2.0% tensile-strained Ge/InGaAs) [13], and NBG TFETs (3% tensile-strained Ge/InGaAs) [13]. LP FinFETs were found to maintain similar I_{ON} as compared to planar MOSFETs (*SS*~110 mV/dec) and simultaneously suppress I_{OFF} due to enhanced gate control, thereby leading to improved subthreshold behavior (*SS*~62 mV/dec). Conversely, LP FinFETs could not supply sufficient I_{ON} below $V_{DD} = 0.4$ V. Alternatively, HP FinFETs exhibited increased I_{ON} at the penalty of degraded I_{OFF} due to their lower *SS* (~64 mV/dec). However, SG TFETs exhibited superior subthreshold dynamics (*SS*~38 mV/dec), leading to reduced I_{OFF} and comparable I_{ON} under low-voltage operation. Moreover, the

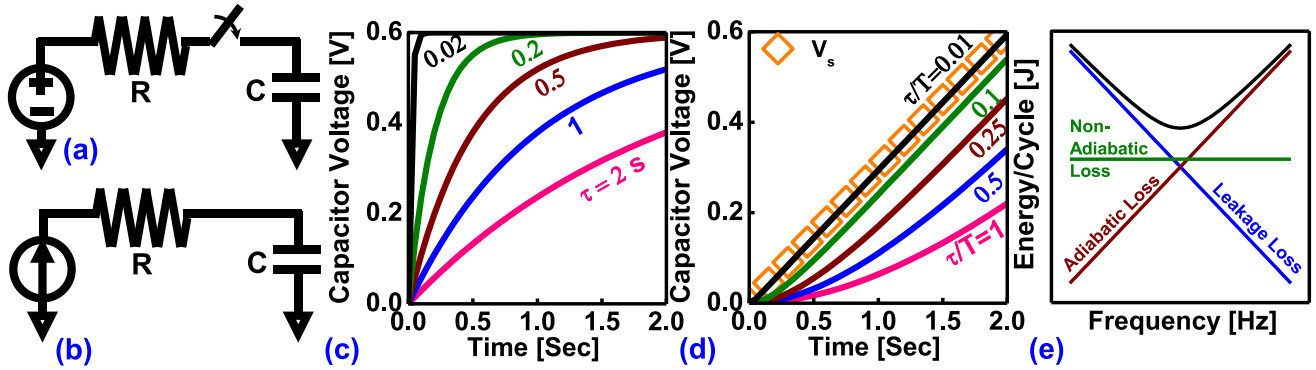

FIGURE 3. RC circuit model of (a) a conventional inverter and (b) an adiabatic switch. Capacitor voltage charging of the (c) conventional inverter and (d) adiabatic switch as a function of charging time and time constant. (e) Frequency dependence of the three energy loss mechanisms in AL.

TABLE 1. Device performance summary.

Device Type	I_{OFF}	I_{ON}	
		Ultra-low Voltage (<0.5V)	Normal Voltage (> 0.5V)
LP FinFET	Low	Low	Comparable
HP FinFET	High	High	High
SG TFET	Low	High	comparable
NBG TFET	Comparable	High	High

constrained tunneling probability at higher operating voltages was found to limit SG TFET I_{ON} above V_{DD} = 0.6 V. Similarly, NBG TFETs (SS∼34 mV/dec) were observed to provide high I_{ON}, due to the near-zero tunneling barrier, and low I_{OFF}. Table 1 summarizes the device characteristics of the FETs investigated in this work for low and conventional operating voltages, noting that all devices are compared against planar MOSFETs. From this comparison, one can find that TFETs offer a potential route for the development of energy-efficient adiabatic logic circuits.

B. THE ADIABATIC SWITCH

The energy dissipation in conventional combinational logic can be understood *via* a simple case study: the CMOS inverter. In a basic inverter circuit, the pull-up network, pull-down network, and load capacitance can be modeled as an ideal switch in series with a resistor (R) and load capacitor (C) supplied by a constant voltage source (V_s), as shown in Fig. 3(a). Throughout the duration of the switching process, V_s transfers a charge Q (equal to CV_{DD}) and energy E (CV_{DD}^2) to the load capacitor. However, the capacitor can only store an energy equivalent to $\frac{1}{2}CV_{DD}^2$. Thus, half of the system's energy loss occurs during the charge transfer from V_s to the load (*i.e.*, during the charging process). Likewise, the remainder of the energy dissipation occurs during the pull-down, or discharging, process. As a result, the entirety of the energy supplied is consumed during each switching cycle. Fig. 3(c) shows the capacitor voltage as a function of time for different time constants (τ). One can find from Fig. 3(c) that only the charging speed is affected by the system's time constant. Thus, the resistance of the pull-up and pull-down networks of a conventional combinational logic circuit only affect the circuit's charging and discharging time, and not its dynamic power dissipation.

Alternatively, an adiabatic switch can be modeled as a constant current source in series with a resistor (R) and capacitance (C), as shown in Fig. 3(b). Unlike conventional combinational logic, adiabatic logic circuits gradually ramp the supply voltage. As long as the ramping period is sufficiently large (several times larger than the time constant of the system), the voltage drop across R becomes arbitrarily small and the source provides virtually constant current. Thus, the capacitor voltage (V_C) in the system can be expressed as:

$$\frac{V_S(t) - V_C(t)}{R} = C\frac{dV_C(t)}{dt}$$
$$\frac{dV_C(t)}{dt} + \frac{1}{RC}V_C(t) = \frac{V_{DD}}{TRC}t \tag{1}$$

where V_S is the voltage of the ramped supply source and $\tau = RC$. By applying non-homogeneous, first-order linear differential equations [18], V_C, the voltage drop across resistance R (V_R), and the current $i(t)$ can be expressed as:

$$V_C(t) = V_{DD}\left(\frac{t}{T}\right) + V_{DD}\left(\frac{\tau}{T}\right)\left[e^{-\frac{t}{\tau}} - 1\right], \tag{2}$$
$$V_R(t) = V_{DD}\left(\frac{\tau}{T}\right)\left[1 - e^{-\frac{t}{\tau}}\right], \tag{3}$$
$$i(t) = V_{DD}\left(\frac{C}{T}\right)\left[1 - e^{-\frac{t}{\tau}}\right], \tag{4}$$

where T is the switching period (*i.e.*, ramping interval). From the above, one can find that smaller time constants reduce V_R, which acts as the source of power dissipation in this model. Fig. 3(d) shows V_C as a function of time for different τ/T ratios, wherein V_s is ramped to 0.6 V in a 2.0 s interval. For small τ/T, V_C closely follows V_s due to the direct relation between V_R and τ/T. This result explicitly reinforces the previous assumption regarding the necessity of sufficiently long ramping intervals for the supply. Subsequently, the voltage source can be treated as a constant current source through

the following expression:

$$i(t) = C\frac{dV_c(t)}{dt} = C\frac{dV_S(t)}{dt} = C\frac{V_{DD}}{T}. \quad (5)$$

To further estimate the energy dissipation in an adiabatic switch, the energy of the entire system can be expressed as:

$$E_{AL} = \int_0^T p(t)dt = \int_0^T V_S(t)i(t)dt,$$
$$= \int_0^T [V_R(t) + V_C(t)]i(t)dt. \quad (6)$$

Since capacitors store energy, the total energy dissipation through an ideal capacitor for an entire switching cycle is zero. Thus, the energy dissipation through the resistor R is given by:

$$E_{AL} = \int_0^T V_R(t)i(t)dt = \int_0^T R \cdot i^2(t)dt,$$
$$= \int_0^T R\frac{C^2V_{DD}^2}{T^2}dt = \frac{RC}{T}CV_{DD}^2. \quad (7)$$

Furthermore, full adiabatic logic consists of two phases: energy supply and energy recovery. It is important to note that each phases dissipates the same amount of energy; thus, the total energy dissipation is $E_{AL} = 2\frac{RC}{T}CV_{DD}^2$. This is in comparison to a conventional CMOS inverter, wherein the energy dissipation is $E_{CMOS} = CV_{DD}^2$. Comparing the expressions for energy dissipation between adiabatic and conventional combinational logic, one can find that the adiabatic implementation introduces a new degree of freedom, time, thereby permitting additional reductions in energy dissipation. The necessary condition for which the energy dissipation of an adiabatic implementation is lower than that of a conventional implementation is given by:

$$E_{AL} < E_{CMOS},$$
$$2\frac{RC}{T}CV_{DD}^2 < CV_{DD}^2,$$
$$T > 2RC. \quad (8)$$

This result reveals that the adiabatic switch conserves more energy with respect to the conventional switch under two conditions: (i) a long switching period (*i.e.*, a lower clock frequency), and (ii) a lower time constant. Furthermore, the channel resistance (*i.e.*, ON resistance) plays an important role in dictating energy dissipation in an adiabatic switch, as compared to its non-existent influence on conventional combinational logic energy dissipation.

In any circuit, leakage power cannot be recovered; therefore, the estimated power loss due to all leakage mechanisms is also an important figure of merit. To this end, the totality of leakage mechanisms in a system can be combined into an average leakage current, I_{leak}, which leads to the leakage-dependent energy dissipation given by:

$$E_{leak} = V_{DD}I_{leak}T = V_{DD}I_{leak}\frac{1}{f}. \quad (9)$$

Since the leakage current is predominately independent of time, the energy dissipation is constant as a function of time. However, additional energy would accumulate during increased operational time (*i.e.*, at lower frequencies). In addition to energy dissipation due to leakage current, another form of energy dissipation that cannot be recovered is non-adiabatic loss, as given by [19] and [20]:

$$E_{NAL} = \frac{1}{2}CV_{th,p}^2. \quad (10)$$

Fig. 3(e) illustrates all of the energy dissipation mechanisms heretofore discussed as a function of frequency. One can find that an optimal frequency exists at which a minimum energy dissipation occurs. This is a result of the opposing linear dependencies of the adiabatic and non-adiabatic losses on frequency. Thus, the challenge is to design adiabatic circuits at an optimal frequency (f_{op}) for IoT applications.

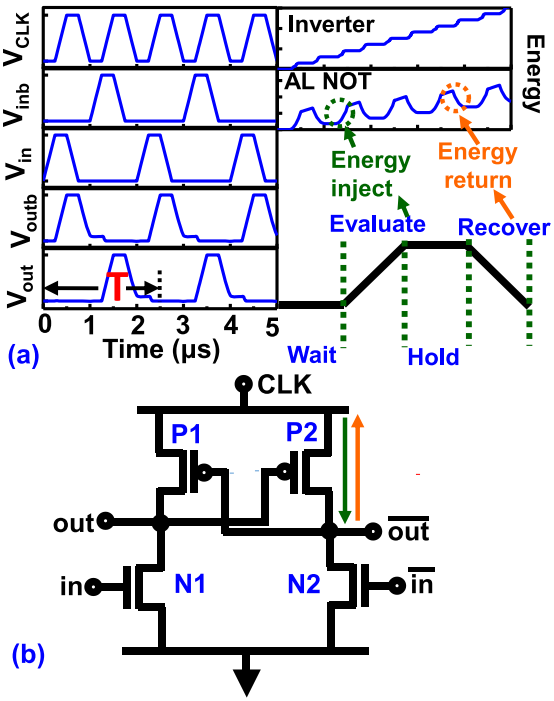

FIGURE 4. (a) Output waveforms and four-phase operation CLK for HP FinFET PFAL. Energy is injected from CLK to output (green) in the evaluate phase and returned to CLK during the recovery phase. (b) ECRL circuit schematics. The returned current and injected current are illustrated by orange and green arrows.

C. FOUR-PHASE POWER CLOCKED ADIABATIC LOGIC

One method of establishing a ramping voltage source is to use a power clock as opposed to a constant voltage supply. Four-phase power clocks have been widely used in several adiabatic logic implementations [21]–[27]. In order to demonstrate the operation of adiabatic logic, efficient charge recovery logic (ECRL) is considered here. Fig. 4 shows the waveforms and schematic circuit representation of an ECRL inverter. Each power clock cycle consists of four phases having the same duration, that is: wait, evaluate, hold, and recover. Initially, the power clock (CLK) and $\overline{in}$ are low, the complementary output (*out*, $\overline{out}$) are low, and *in* is awaiting

an input signal. During the wait phase, P1 and P2 are OFF due to CLK being connected to ground, thus *out* and $\overline{out}$ are also low. During the evaluation phase, the input signal is evaluated and generates a corresponding output. When *in* remains high and $\overline{in}$ remains low, N1 and N2 are ON and OFF, respectively. As CLK is ramped above $V_{th,p}$, P1 and P2 are turned ON. Conversely, *out* remains unchanged due to N1 remaining ON. This ensures that P2 remains on during the evaluation phase and $\overline{out}$ mirrors the ramping supply voltage. During the hold phase, all signals are kept at their current status, thereby supplying subsequent logic gates with stable inputs. Finally, in the recovery phase, CLK is ramped from V_{DD} to ground. Since the voltage at $\overline{out}$ is now higher than CLK, current flows from $\overline{out}$ to CLK. However, $\overline{out}$ requires a minimum voltage, $V_{th,p}$, such that P2 remains ON; thus, a minimum, non-adiabatic energy ($\frac{1}{2}CV_{th,p}^2$) remains at $\overline{out}$ for reuse during the next cycle.

The energy dissipation of conventional CMOS and adiabatic inverters as a function of time is shown in Fig. 4(a). One can find that the energy dissipation in a conventional CMOS inverter accumulates with increasing operation cycles. However, under adiabatic operation, the energy injected into the system during the evaluation phase is returned to the voltage source during the recovery phase. Thus, the effective energy consumption of the adiabatic inverter is significantly reduced compared to that of the conventional CMOS inverter. Furthermore, the critical path in adiabatic circuit operation can be identified as the pull-up network, which functions as the current injection (Fig. 4(a), green arrow) and recovery (Fig. 4(a), orange arrow) route for the ECRL circuit.

D. DESIGN OF TFET-BASED ADIABATIC LOGIC

In this section, we will discuss adiabatic logic circuit topologies utilizing TFET devices. Three major implementations of adiabatic logic (ECRL, PFAL, and 2N-2N2P) were considered in this work, as illustrated in Fig. 5. In contrast to the bidirectional current flow in conventional MOSFETs, TFETs provide unidirectional current, as discussed in Section II-B. Consequently, the pull-up network in an adiabatic circuit requires additional design considerations in order to provide a pathway for charge injection and recovery. In this work, we propose the incorporation of additional recovery transistors to provide a charge recovery path to the supply source, as highlighted in red in Fig. 5. Unlike conventional MOSFETs, wherein the drain and source regions are distinguished by the applied voltage (*i.e.*, they are ambipolar), H-TFETs utilize distinct drain and source materials, thus they behavior as unipolar, asymmetric devices. As a result, current flow is restricted to the *n*- or *p*-type H-TFET during injection or recovery, thus correct adiabatic logic circuit functionality is only realizable when utilizing both polarities in the adiabatic pull-up network.

Fig. 5(a) shows a schematic diagram of an ECRL circuit consisting of a set of latched pull-up transistors supplied by a power clock. It should be noted that the ECRL

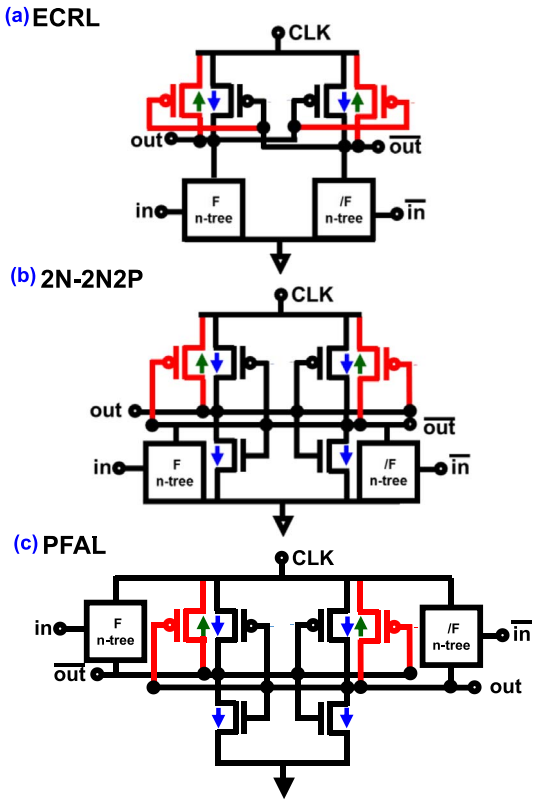

FIGURE 5. Circuit schematics of (a) ECRL, (b) 2N-2N2P, and (c) PFAL. The 'black boxes' represent *n*-type function trees. Red FETs indicate an additional TFET added to compensate for TFET unidirectionality.

configuration utilizes the fewest transistors; however, during the wait phase, all outputs remain floating, potentially resulting in incorrect signal chains or soft errors during operation [4]. In order to mitigate this issue, the 2N-2N2P topology was proposed [24]. Fig. 5(b) diagrammatically illustrates a 2N-2N2P circuit wherein two cross-coupled *n*-TFETs are added in parallel to the *n*-function blocks. Here, the added transistors behave similar to a latch cell used in static random-access memory (SRAM) designs, providing a path to ground as well as avoiding floating nodes during operation. However, due to the additional transistors and push-pull functionality, 2N-2N2P exhibits increased energy dissipation as compared to ECRL.

Lastly, Fig. 5(c) shows a schematic diagram of the final adiabatic logic implementation investigated in this work: positive feedback adiabatic logic (PFAL) [23], [25]. A key difference between PFAL and 2N-2N2P is that the *n*-tree function blocks are in parallel with the pull-up network as opposed to the pull-down network. As a result, the overall resistance decreases during node charging [4], thereby reducing the energy dissipation due to adiabatic losses. Table 2 summarizes the advantages and disadvantages of the adiabatic logic designs proposed in this work.

III. RESULTS AND DISCUSSION

To more accurately compare the performance of the proposed adiabatic logic circuits (*i.e.*, ECRL, 2N-2N2P, and

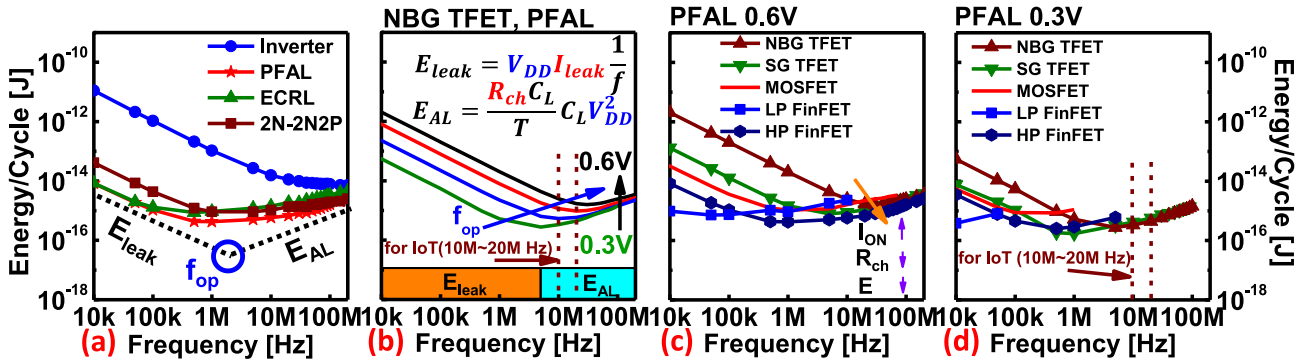

FIGURE 6. Energy/cycle for (a) all studied HP AL designs, (b) NBG TFET PFAL architecture for 0.3 V < V_{DD} < 0.6 V, (c) and (d) frequency optimization for all investigated FET types using the PFAL architecture operating under 0.6 V and 0.3 V V_{DD}.

TABLE 2. Adiabatic logic performance summary.

Circuit Type	Advantage	Drawback
ECRL	Fewest transistors	Floating nodes
2N-2N2P	No floating nodes	Extra transistors
PFAL	Lowest resistance	Extra transistors

PFAL), the geometry of all FETs has been optimized to provide matching drive currents at $V_{DD} = 0.5$ V and equivalent rise and delay times at an operational frequency of 500 MHz. We note that the load capacitance was set to a nominal value of 20 fF [19]. Due to the four-phase operation of the investigated adiabatic circuits, instantaneous and average power consumption do not reflect the true energy dissipation within the circuit. Hence, in this work, the energy dissipation per cycle as a function of frequency is used as a performance metric for comparison between the applicability of each adiabatic logic design towards low power applications.

A. PERFORMANCE ANALYSIS OF TBAL

Fig. 6(a) shows the energy dissipation per cycle for each investigated adiabatic logic design implemented using HP FinFETs operating at $V_{DD} = 0.6$ V. According to Eq. (9), leakage-related losses are dominate at lower frequencies due to the extended operation time. On the other hand, at higher operating frequencies, one can find that the energy dissipation of a conventional inverter remains constant due to the absence of adiabatic processes. Conversely, the energy dissipation per cycle of the adiabatic logic circuits is observed to increase with increasing frequency. This is due to a breakdown in the adiabatic process at higher frequencies (lower T), as detailed in Eqs. (7) and (8). A complete breakdown of adiabatic operation occurs when the load capacitance cannot be effectively charged following the source voltage. Additionally, PFAL exhibited the lowest energy per cycle due to its minimal ON resistance. Consequently, we will next investigate the impact of operational voltage ($V_{DD} = 0.3$ V and 0.6 V) and device architecture (*e.g.*, MOSFET, FinFET, TFET) on the energy dissipation in PFAL circuits.

The energy dissipation per cycle for PFAL implemented using NBG TFETs operating at 0.3 V < V_{DD} < 0.6 V is shown as a function of frequency in Fig. 6(b). The resulting energy dissipation can be decomposed into two main constituents: energy loss due to leakage and energy loss due to adiabatic losses. With respect to the former, the energy per cycle decreases for decreasing operating voltage due to a reduction in I_{leak} and the linear dependence of E_{leak} on V_{DD}. On the other hand, adiabatic losses decrease as a function of V_{DD}^2. Thus, although channel resistance increases as the supply voltage is reduced, the quadratic dependence of adiabatic losses on operating voltage dominates their associated energy dissipation. Additionally, one can find that the optimized working frequency (f_{op}) shifted to higher frequencies with increasing supply voltage. However, the corresponding increase in the energy dissipation minima negates the benefit of TBAL adoption. Thus, it becomes critical to estimate the energy dissipation per cycle within a select range of f_{op} required by IoT applications, *e.g.*, 10 MHz – 20 MHz.

After investigating the impacts of adiabatic logic architecture and operating voltage on energy dissipation per cycle, we will now discuss the role of device architecture (*i.e.*, MOSFET, FinFET, TFET) on adiabatic circuit performance. Fig. 6(c) shows the energy per cycle as a function of frequency for PFAL implemented using five different device types (*i.e.*, planar MOSFET, LP FinFET, HP FinFET, SG TFET and NBG TFET) operating at $V_{DD} = 0.6$ V. As previously discussed, the energy per cycle arcs in Fig. 6(c) can be decomposed into their leakage and adiabatic loss contributions. With regards to leakage-dominated losses, one can find that the LP FinFET-based PFAL circuit exhibited minimal energy dissipation due to the low leakage current device design (see Fig. 2). Similarly, for $V_{DD} = 0.6$ V, both FinFET architectures exhibited lower leakage, as compared to their TFET counterparts, due chiefly to the superior gate control of the FinFET devices. In terms of adiabatic losses, LP FinFETs exhibited the highest energy dissipation of all investigated devices due to the drive current sacrifice made during device design (*i.e.*, the *SS*-limited trade-off between I_{ON} and I_{OFF}). Consequently, the channel resistance (R_{ch}) increase in LP FinFET devices directly correlated with increased energy per cycle. Conversely, HP FinFETs exhibited the lowest adiabatic losses due to their high I_{ON} (low R_{ch}) at $V_{DD} = 0.6$ V. As

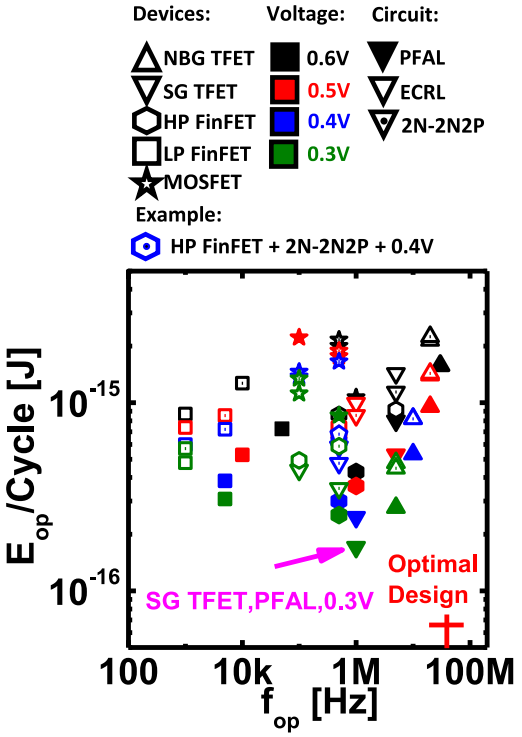

FIGURE 7. Optimized energy/cycle for each AL design, device-type, and operating voltage highlighting f_{op}. Optimal design located in bottom-right (red cross). SG TFET-based PFAL shows the lowest energy consumption at 0.3 V.

a result, the HP FinFET-based PFAL circuit demonstrated the lowest energy per cycle for all investigated device types ($V_{DD} = 0.6$ V) due to the reduced adiabatic and leakage losses.

Similarly, Fig. 6(d) shows the energy per cycle for PFAL implemented using each aforementioned device type operating at $V_{DD} = 0.3$ V. From Fig. 6(d), one can find that both MOSFET- and LP FinFET-based PFAL circuits failed to function as designed beyond $f = 1$ MHz due to the limited I_{ON} (increased R_{ch}) of both devices when operating in the subthreshold bias regime. As a result of the degraded ON current and R_{ch}, both MOSFET- and LP FinFET-based circuits exhibit larger time constants ($\tau = RC$), resulting in adiabatic breakdown at lower frequencies relative to the HP FinFET- and TFET-based designs. Similarly, HP FinFET-based PFAL was also observed to be limited to $f < 10$ MHz due to the subthreshold operation and loss of drive current at $V_{DD} = 0.3$ V. On the contrary, both SG and NBG TFET-based PFAL circuits were found to be capable of operating at ultra-low voltage, demonstrating a minimum in energy dissipation comparable or lower than that observed for the HP FinFET devices at $V_{DD} = 0.3$ V or 0.6 V. Moreover, as compared to the NBG TFET-based PFAL design, the SG TFET-based PFAL circuits exhibited less energy dissipation at lower operating frequencies due to the reduced leakage current of the SG TFET architecture (see Fig. 2).

Fig. 7 benchmarks the lowest energy per cycle (E_{op}) for all investigated device (MOSFET, LP FinFET, HP FinFET, SG TFET, and NBG TFET), circuit (ECRL, 2N-2N2P, and PFAL), and operating voltage ($V_{DD} = 0.3$ V, 0.4 V, 0.5 V, and 0.6V) combinations as a function of frequency. The optimal design solution space, *i.e.*, that which exhibits the lowest energy per cycle at the highest operating frequency, is indicated at the bottom-right of Fig. 7. One can find that FinFET- and TFET-based circuits outperformed planar MOSFET-based designs under all investigated operating conditions. However, LP FinFET-based adiabatic logic circuits exhibit relatively low optimal operational frequencies due to their limited drive currents and corresponding increase in adiabatic losses. Conversely, HP FinFET-based adiabatic logic designs exhibit low energy dissipation per cycle, but fail to function at higher frequencies when operating in the ultra-low voltage regime. Both SG TFET- and NBG TFET-based adiabatic logic circuits solve these challenges, providing low energy per cycle at operating frequencies above 1 MHz when utilized at $V_{DD} = 0.3$ V. However, due to their enhanced drive current at low operating voltages as compared to SG TFETs, NBG-TFET-based adiabatic logic designs exhibit the lowest energy dissipation in the targeted 10 MHz – 20 MHz frequency range utilized in many IoT applications. To further clarify these results, we will next investigate the impact of device and circuit architecture in the 0.3 V $< V_{DD} <$ 0.6 V supply range for a designated working frequency of 10 MHz.

B. VOLTAGE-DEPENDENT TBAL PERFORMANCE ANALYSIS (F = 10 MHZ)

Unlike the previous discussion, we will now quantify the impact of operating voltage, device type, and circuit topology explicitly in the adiabatic loss regime. Thus, given identical load capacitances (20 fF), the resistance in each system will become the most significant factor that will affect the energy dissipation of a given adiabatic logic circuit. Correspondingly, the differing drive currents (and thus R_{ch}) of each device type (for a given V_{DD}) are expected to correlate to the energy per cycle exhibited by the adiabatic circuit. However, at ultra-low voltage, we note that the drive current of thermionic emission based MOSFETs is governed by the subthreshold current, as given by [3] and [19]:

$$I_{sub} = Ae^{\frac{q(V_{GS}-V_{th})}{mkT}}\left(1 - e^{\frac{-q(V_{DS})}{kT}}\right), \tag{11}$$

where A is a device related factor, V_{th} is the threshold voltage, T is the temperature, k is Boltzmann's constant, and m is the body effect factor. The channel resistance can then be derived from Eq. (11), leading to:

$$R_{ch} = \frac{dV_{ds}}{dI_{sub}} = \frac{1}{A'}e^{-\frac{q}{kT}\left(\frac{1}{m}(V_{GS}-V_{th})-V_{DS}\right)}, \tag{12}$$

Thus, the adiabatic loss of thermionic emission-based devices can be calculated by inserting Eq. (12) into Eq. (7) and replacing V_{GS} with V_{DD}, *i.e.:*

$$E_{AL} = \frac{CR_{ch}}{T}CV_{DD}^2 = \frac{C^2}{A'T}e^{-\frac{q}{kT}\left(\frac{1}{m}(V_{DD}-V_{th})-V_{DS}\right)}V_{DD}^2 \tag{13}$$

$$E_{AL} \propto e^{-\frac{q}{kT}(V_{DD})} \times V_{DD}^2. \tag{14}$$

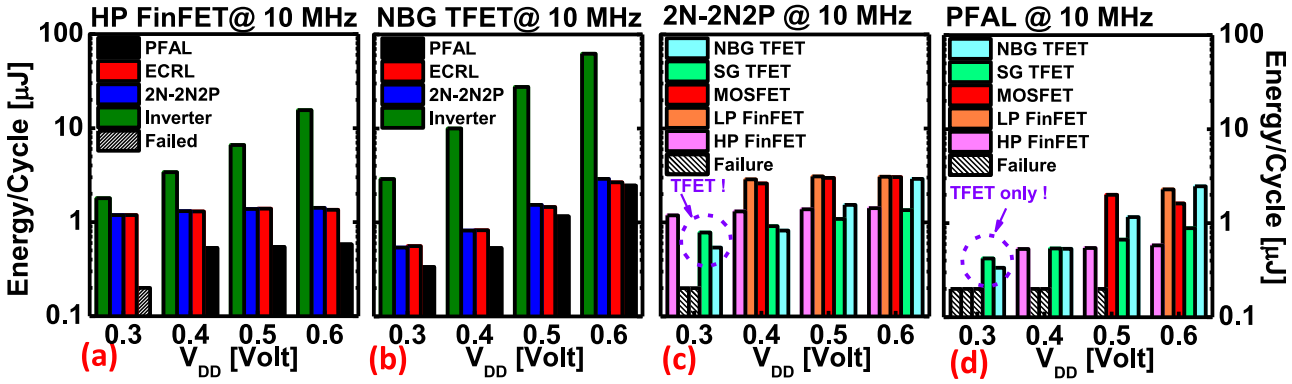

FIGURE 8. Energy per cycle as function of V_{DD} for (a) HP FinFET and (b) NBG TFET AL designs at 10 MHz. Comparison of energy consumption for (c) 2N-2N2P and (d) PFAL using different devices as function of supply voltage at 10 MHz.

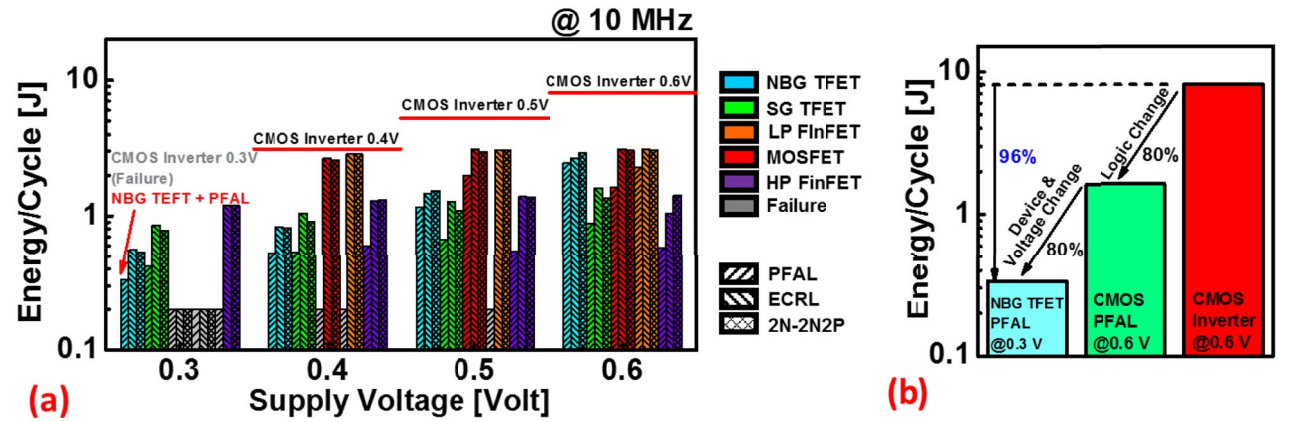

FIGURE 9. (a) Energy dissipation for each AL design, device-type and operating voltage for $f = 10$ MHz (*i.e.*, IoT application frequency). NBG TFET-based PFAL exhibits the lowest energy consumption at 0.3 V. (b) Optimized TBAL energy/cycle benchmarked with conventional logic.

From Eq. (14), one can clearly observe that the adiabatic energy loss term simultaneously depends quadratically on V_{DD} as well as decays exponentially in proportion to V_{DD}. In other words, the increased channel resistance negates the quadratic reduction in energy loss due to V_{DD} scaling, resulting in a weak dependence of the energy per cycle in HP FinFET-based adiabatic logic on the supply voltage, as shown in Fig. 8(a). Conversely, from Fig. 8(a) one can find that the energy per cycle of a conventional inverter decreases with decreasing V_{DD} due to the nominal quadratic dependence of energy dissipation on V_{DD} for non-adiabatic processes. On the other hand, NBG TFET-based adiabatic logic exhibited a significant decrease in energy per cycle as a function of reducing supply voltage, as shown in Fig. 8(b). As previously discussed, this is a result of the low threshold voltage of TFET devices, allowing for device operation in the saturation regime at ultra-low operating voltages. Consequently, and unlike thermionic emission-based FETs, TFETs do not experience an exponential increase in channel resistance when operating at $V_{DD} < 0.6$ V, resulting in reduced adiabatic losses.

Figs. 8(c) and 8(d) shown the energy dissipation per cycle for 2N-2N2P and PFAL designs utilizing each device type and operating voltage hitherto mentioned. As discussed above, thermionic emission-based devices exhibited a weak relation between supply voltage and energy dissipation. On the contrary, tunneling-based devices exhibited continued voltage scaling of energy dissipation due to their enhanced drive currents at ultra-low operating voltages. Moreover, at $V_{DD} = 0.4$ V and below, NBG TFET-based adiabatic logic was found to provide the lowest energy dissipation due to the high I_{ON}, and therefore lower channel resistance, of NBG TFET devices.

C. OPTIMAL TBAL DESIGN CONSIDERATIONS

Fig. 9(a) benchmarks the energy/cycle as a function of FET-type and adiabatic logic circuit design for an operational frequency of 10 MHz. The horizontal red lines are a guide for the eye representative of the baseline energy dissipation of planar CMOS inverters at each investigated V_{DD}. One can find that at $V_{DD} = 0.3$ V, the high channel resistance of conventional MOSFET devices significantly increased the adiabatic circuit charging and discharging times such that the output node could neither be fully charged nor discharged, thereby leading to functional failure. In contrast, the more optimal TFET-based designs, in particular the NBG TFET-based PFAL design, provided unhindered adiabatic logic circuit functionality at low operating voltages due to the increased I_{ON} and lower channel resistance of TFET devices operating at low V_{DD}.

IV. CONCLUSION

A novel, tunnel FET-based adiabatic circuit topology has been proposed and evaluated based upon its energy dissipation per cycle. By incorporating adiabatic logic functionality into standard combinational logic, an 80% reduction in energy/cycle was realized as compared to standard combinational logic. In addition, a further 80% reduction in energy/cycle was demonstrated by utilizing NBG TFET devices, resulting in a 96% reduction in energy/cycle as compared to conventional Si CMOS. Through co-optimization at the device and circuit levels, this work aims to enable energy-efficient computing architectures for IoT applications.

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