

Single-junction InGaP/GaAs Solar Cells Grown on Si Substrates with SiGe Buffer Layers

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Single junction InGaP/GaAs solar cells displaying high efficiency and record high open-circuit voltage values have been grown by metal–organic chemical vapor deposition on Ge/graded SiGe/Si substrates. Open-circuit voltages of 980 mV under AM0 conditions have been verified to result from a single GaAs junction, with no evidence of Ge-related sub-cell photoresponse. AM0 efficiencies close to 16% have been measured for a large number of small-area cells, the performance of which is limited by non-fundamental current losses due to significant surface reflection resulting from >10% front-surface metal coverage and wafer handling during the growth sequence for these prototype cells. It is shown that at the material quality currently achieved for GaAs grown on Ge/SiGe/Si substrates, namely a 10 ns minority-carrier lifetime that results from complete elimination of anti-phase domains, and maintaining a threading dislocation density of $\sim 8 \times 10^5 \text{ cm}^{-2}$, 19–20% AM0 single-junction GaAs cells are imminent. Experiments show that the high performance is not degraded for larger-area cells, with identical open-circuit voltages and higher short-circuit current (due to reduced front metal coverage) values being demonstrated, indicating that large-area scaling is possible in the near term. Comparison with a simple model indicates that the voltage output of these GaAs-on-Si cells follows the ideal behavior expected for lattice-mismatched devices, demonstrating that unaccounted-for defects and issues that have plagued other methods to epitaxially integrate III–V cells with Si are resolved by using SiGe buffers and proper GaAs nucleation methods. These early results already show the enormous and realistic potential of the virtual SiGe substrate approach for generating high-efficiency, lightweight and strong III–V solar cells. Copyright © 2002 John Wiley & Sons, Ltd.

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INTRODUCTION

The development of high-efficiency III–V compound solar cells grown on Si substrates has received sustained interest in the photovoltaics community for more than two decades.^{1–3} The attractiveness of III–V/Si solar cells stems from combining optimum photovoltaic materials, such as InGaP, GaAs and AlGaAs with an optimum substrate material, Si. Compared with Ge, currently the dominant substrate for III–V space photovoltaics, Si possesses far superior substrate properties with respect to mass density, mechanical strength, thermal conductivity, cost, wafer size and availability. Unfortunately, the 4% mismatch in lattice constant between Si and GaAs, generates a high density of threading dislocations in III–V overlayers grown on Si, severely reducing GaAs material quality, carrier lifetimes, and III–V solar cell performance. Nevertheless, many groups have recognized the potential benefits of epitaxial III–V/Si solar cells, and III–V/Si integration in general, leading to investigations of many methods to control and reduce dislocation densities in this highly mismatched heterostructure. These approaches include the insertion of various III–V intermediate layers based on compositionally graded III–V buffers and strained layer superlattices, and the use of thermally cycled annealing of intermediary layers prior to cell growth. Each has been successful in reducing threading dislocation densities in the III–V overlayers from $\sim 10^9$ – 10^{10} cm⁻² for direct GaAs-on-Si epitaxy, to the 10^7 cm⁻² range.^{3–8} While impressive, this dislocation density still limits the minority-carrier lifetime in GaAs to 1–4 ns, even after post-growth defect passivation treatments via hydrogenation.^{7,8} These values are not high enough to yield high-efficiency III–V cells, and those cells that have been fabricated suffer from low open-circuit voltages, typically of the order of 900 mV or lower under AM0 conditions for single-junction GaAs, providing an ultimate limit on cell efficiency.

Each of the approaches highlighted above involve some form of strain management and dislocation filtering within the III–V layers, and they tend to approach a similar final threading dislocation density and minority-carrier lifetime for GaAs-on-Si after optimization. This observation has motivated the development of an alternative approach in which the surface lattice constant of the Si substrate itself is engineered prior to any III–V epitaxy by growth of compositionally graded SiGe buffers, rather than dealing with the mismatch only within the III–V epitaxial layers. In this way, the lattice mismatch is addressed in a material system and under growth conditions that are independent from growth of the III–V solar cell region. Recently, this ‘virtual Ge substrate’ approach has resulted in threading dislocations as low as 8×10^5 cm⁻² within relaxed GaAs overlayers, demonstrating that the SiGe buffer approach has broken through a barrier that has limited the progress of III–V buffer approaches for GaAs on Si for more than ten years.^{9,10} The impact of this lower dislocation density value on electronic material quality is evident by yielding the highest minority-carrier lifetimes reported to date for GaAs grown on Si, with values in excess of 10 ns being demonstrated in *n*-type GaAs.^{9,10} At this lifetime value, high-efficiency III–V solar cells can be expected, and the use of SiGe buffers for generating high-efficiency III–V cells on Si for space photovoltaics is extremely promising.¹¹ Recently, we reported GaAs solar cells grown on Ge/SiGe/Si that displayed high efficiency and the highest open-circuit voltages reported to date for GaAs cells grown on Si substrates.¹ In this paper, we extend these early results in an ongoing project to describe a quantitative picture of cell performance dependence on dislocation density, report on larger cell area development and investigate potential activity of the GaAs/Ge interface region for *p*-on-*n* GaAs cells on Ge/SiGe/Si substrates.

EXPERIMENTAL DETAILS

InGaP/GaAs single-junction, *p*-on-*n* configuration solar cells were grown by low-pressure MOCVD on Ge/graded SiGe/Si wafers. The step-graded SiGe buffers¹² were grown on (001) Si wafers offcut by 6° toward the in-plane [110] direction by ultra-high-vacuum chemical vapor deposition (UHVCVD) using SiH₄ and GeH₄ as source gases, at an average grading rate of 10% Ge/μm. Plan-view and cross-sectional transmission electron microscopy (TEM), electron-beam-induced current (EBIC), and etch pit density (EPD) measurements confirmed an average TDD (threading dislocation density) = 0.8 – 1.5×10^6 cm⁻² present in the relaxed Ge cap layer for a large number of growth runs. EPD measurements made on GaAs overlayers grown on the Ge/SiGe/Si substrates revealed an identical TDD value as obtained for the Ge cap layers, indicating negligible

dislocation nucleation by III–V growth and the formation of an ideal low-mismatched GaAs/Ge interface on these substrates. That is, the graded SiGe layers were successful in forming a virtual Ge substrate on an actual Si wafer. The methodology used to eliminate additional problematic issues that are specifically related to the GaAs/Ge interface, namely anti-phase domain (APD) formation and cross-diffusion leading to autodoping, can be found in earlier publications.^{10,11,13} The *p*-on-*n* configuration InGaP/GaAs single-junction cells were grown via low-pressure MOCVD at 620°C following transfer to the MOCVD growth system. The basic, non-optimized single-junction cell designs reported here are shown in Figure 1. Au/Cr was used for the *p*-type GaAs contact in all cases; *n*-type contacts of Au/Sb and Al were used for cells grown on Ge and Ge/SiGe/Si substrates, respectively. Certain cells were coated with a dual layer MgF₂/ZnS anti-reflection coating.

ROLE OF DISLOCATION DENSITY ON GaAs/Ge/SiGe/Si CELL PROPERTIES

The impact of threading dislocation density on minority-carrier diffusion length L_p , and hence minority-carrier lifetime τ_p , has been well documented.^{3,14} However, the detailed, quantitative dependence of cell V_{OC} and J_{SC} on TDD is less obvious, and requires greater scrutiny to generate optimum device designs for GaAs on Si solar cells with the significant reduction in TDD that has been established with SiGe graded buffers, compared with previous efforts. The average spacing between threading dislocations¹⁴ can be approximated by:

$$L_{TDD} = (\pi(\text{TDD}))^{-1/2} \quad (1)$$

where for simplicity it is assumed that all dislocations are uniformly spaced, perpendicular to the growth plane. Thus, this is a rough approximation of the actual network of 60° threading dislocations present in mismatched GaAs. To understand the implication of dislocation density, the average dislocation spacing must be compared with the minority-carrier diffusion length, which for *n*-GaAs is given by:

$$L_p = (D_p \tau_p)^{1/2} \quad (2)$$

where, accounting for doping and TDD,¹⁴

$$D_p = 7.347 \times 10^6 / (6.697 \times 10^5 + n^{1/3}) \quad (3)$$

$$1/\tau_p = 1/\tau_{p0} + \pi^3 D_p (\text{TDD}) / 4 \quad (4)$$

| | |
|--------------------------|---------|
| p+ - GaAs cap | (1000Å) |
| p - InGaP | (500Å) |
| p - GaAs emitter | (5000Å) |
| n - GaAs base | (2 μm) |
| n - InGaP BSF | (1000Å) |
| n - GaAs Buffer | (1000Å) |
| n - Ge/GeSi/Si substrate | |

Figure 1. Basic *pn* single-junction InGaP/GaAs solar cell structure grown by MOCVD on Ge and Ge/SiGe/Si substrates

and the other terms have their usual meanings, noting that the carrier mobilities at typical base doping levels are not influenced by TDD for values less than $\sim 10^8 \text{ cm}^{-2}$. Figure 2 shows the average dislocation spacing, plotted as a function of TDD following Equation (1), along with a plot of the expected dependence of minority-carrier hole diffusion length on TDD for n -type GaAs doped at $1 \times 10^{17} \text{ cm}^{-3}$. The diffusion length dependence was calculated from Equations (2–4). For the latter, a value for the non-dislocation-limited lifetime τ_{po} for minority carrier holes of 20 ns was used, based on time-resolved photoluminescence studies on $n = 1 \times 10^{17} \text{ cm}^{-3}$ GaAs grown on Ge substrate wafers at 300 K, for which dislocation density was not a factor.¹¹ As seen from the figure, for TDD values greater than $\sim 2 \times 10^6 \text{ cm}^{-2}$, the diffusion length is limited by TDD spacing. That is, above this value, the average dislocation spacing is of the order of or less than one diffusion length. For TDD values lower than $1 \times 10^6 \text{ cm}^{-2}$, the average dislocation spacing becomes much larger than a diffusion length, and recombination is limited by non-dislocation-related processes, which at this typical base doping value are primarily bulk Shockley–Read–Hall recombination. Note that these calculations are for one value of n -type GaAs doping. The position of the knee in the curve in Figure 2, and therefore the TDD threshold required to achieve ‘dislocation-independent’ minority-carrier lifetimes and diffusion lengths, shifts to lower values as GaAs doping is reduced due to the higher lifetimes and longer diffusion lengths for lightly doped material. This must be a consideration for achieving optimum lattice-mismatched cell designs.

The effect of TDD on J_{SC} of GaAs/Si cells is largely dependent on the cell base thickness, which, owing to the large absorption coefficient of GaAs, can be designed to be less than a typical GaAs minority-carrier diffusion length without significantly compromising current collection due to incomplete optical absorption. Hence, the TDD limitation is somewhat relaxed by proper cell design. For instance, a TDD value of $1 \times 10^6 \text{ cm}^{-2}$ leads to an average dislocation spacing of $5.5 \mu\text{m}$, almost twice the hole diffusion length in n -GaAs at a doping of $1 \times 10^{17} \text{ cm}^{-3}$. To absorb more than 95% of the incident AM0 light requires a total GaAs thickness of approximately $2 \mu\text{m}$. For p -on- n cell configurations that typically include an emitter thickness of approximately $0.5 \mu\text{m}$, a base thickness of $2 \mu\text{m}$ is easily sufficient to avoid dislocation-limited collection. Hence, optimal base thickness can scale with TDD, as long as significant optical absorption is not compromised. Indeed, this approach was verified by earlier work, where high J_{SC} values for GaAs/Si cells, having a base thickness of $1.3 \mu\text{m}$, were reported to be comparable to values obtained for GaAs/GaAs homoepitaxial cells, in spite of reported TDD values of $\sim 5 \times 10^6 \text{ cm}^{-2}$ that led to minority-carrier lifetimes³ of only 1–3 ns. In comparison, for the GaAs/Ge/SiGe/Si system discussed here, for which minority-carrier lifetimes in excess of 10 ns have been demonstrated, ideal J_{SC} values should be achievable with a more conventional base thickness, allowing for more complete absorption of the solar flux. This is confirmed by Figure 3, which shows a comparison of external quantum

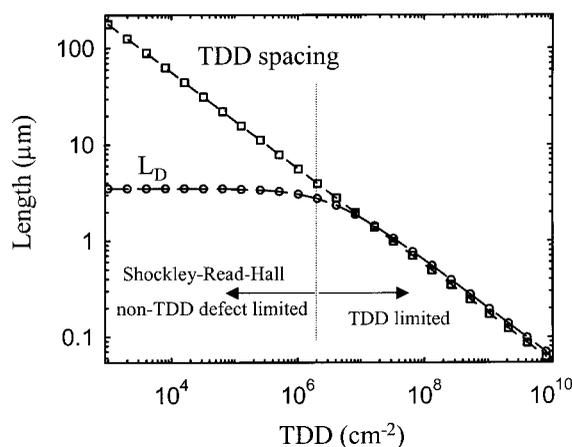


Figure 2. Calculated spacing of parallel threading dislocations as a function of threading dislocation density is shown with calculated minority-carrier hole diffusion lengths based on a measured starting (non-dislocation-limited) minority-carrier lifetime of 20 ns for GaAs grown on Ge wafers, assuming an n -type doping of $1 \times 10^{17} \text{ cm}^{-3}$. TDD- and non-TDD-limited regions are shown

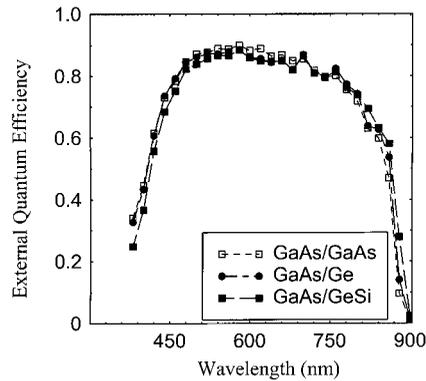


Figure 3. Spectral response measurements made on identical GaAs cell structures grown on GaAs, Ge and Ge/SiGe/Si substrates by MBE, indicating identical collection efficiency independent of substrate and lattice mismatch

efficiency (EQE) data collected for single-junction GaAs solar cells with a 2.5- μm -thick base grown on GaAs, Ge, and GeSi substrates by molecular beam epitaxy. Photon collection efficiencies are seen to be independent of substrate choice, indicating that, even for a conventional base thickness in a p -on- n configuration, no impact of TDD on J_{SC} is observed, consistent with the low TDD values, and confirming that long diffusion lengths are maintained after complete cell processing.

While creative device designs can be used to minimize the impact of TDD on J_{SC} , a flexibility that is in part due to the strong absorption coefficient for GaAs, the open-circuit voltage is less forgiving and, along with fill factor, has proven to be the key efficiency limiting parameters for III-V cells grown on mismatched substrates. TDD will impact V_{OC} through several means. For the ideal Schockley diode solar cell model, TDD increases the D/L ratio since the diffusion coefficient D will not be limited by dislocation spacing whereas the diffusion length L , is limited by dislocation spacing. High D/L values leads to increased saturation current densities J_0 and lower V_{OC} through the expression:

$$V_{\text{OC}} = (kT/q)\ln(J_{\text{SC}}/J_0) \quad (5)$$

A more likely limitation on V_{OC} is via dislocation-related recombination within the depletion region that can generate appreciable recombination current and, for higher TDD values, will generate an array of low-resistance shunt paths across the junction. It is the combination of these reasons that, until this work, has typically limited measured V_{OC} values for GaAs cells grown on Si to less than ~ 900 mV under AM0 conditions, far less than the typical 1 V values observed for GaAs/GaAs and GaAs/Ge single-junction cells. For cells where the dominant dark current is due to depletion region recombination, the V_{OC} expression¹⁴ can be written as:

$$V_{\text{OC}} = (2kT/q)\ln(J_{\text{SC}}/J_{0r}) \quad (6)$$

where

$$J_{0r} = qn_i W D_p / 2L_p^2 \quad (7)$$

Figure 4 shows the theoretical dependence of V_{OC} on TDD based on these assumptions, with measured data from several groups, shown along with data from our work. All are for p/n configured cells. In all prior cases significant deviation from this model is observed. This is indicative of several possibilities. First is that V_{OC} in the earlier reports was limited by other factors not included in this simplistic model, possibly shunt currents or anti-phase domains that have been observed to reduce carrier lifetimes and diffusion lengths dramatically. Second is the question of accurately measured TDD values. Below approximately 10^7 cm^{-2} , cross-sectional TEM measurements are not useful, and dislocation densities must be measured by techniques with lower resolution

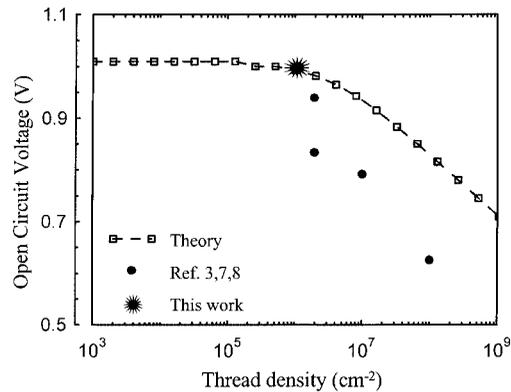


Figure 4. Plot of calculated AM0 V_{OC} values for a single GaAs junction p/n cell as a function of threading dislocation density based on Equations (6) and (7). Also shown are measured V_{OC} values from prior work^{3,7,8} and from cells on Ge/SiGe/Si as reported here. Note the close match between theory and our data, indicating that unaccounted limitations have been resolved

(larger fields of view) such as etch pit density or electron-beam-induced current, in conjunction with plan-view TEM. With either of these methods, however, it is difficult to distinguish between dislocation pileups, a common occurrence for graded buffer layers, and individual threading dislocations, and counting errors can be expected. Moreover, dislocation pileups will be far more deleterious than isolated dislocations, since they can act as significant segregation sites for dopants and other impurities. A third possible explanation for the observed low V_{OC} values that was suggested by authors of the earlier studies was an increased depletion region generated by the intersection of dislocation cores with interfaces and surfaces, leading to unaccounted recombination currents.^{7,8}

In contrast to these prior reports, close agreement between this simple model and actual results have been achieved for GaAs cells on Ge/SiGe/Si substrates. Figure 5 shows light $I-V$ AM0 data obtained for a particular set of p/n cells having the same design, grown by MOCVD on both Ge and Ge/SiGe/Si substrates. Nearly identical cell parameters are observed for both substrates, demonstrating that the current TDD value is not limiting the device performance, consistent with the discussions above, and that ideal, low-mismatched GaAs/Ge growth has been achieved on SiGe/Si. Through several sets of cell growth and fabrication cycles, more than 100 of such high-performance GaAs cells on Ge/SiGe/Si have been demonstrated, with AM0 V_{OC} values ranging from 950 to 1030 mV for structures having TDD values between 9×10^5 and 2×10^6 cm⁻². These V_{OC} values are the highest ever achieved for GaAs cells grown on a Si substrate by any method to date. The close match to

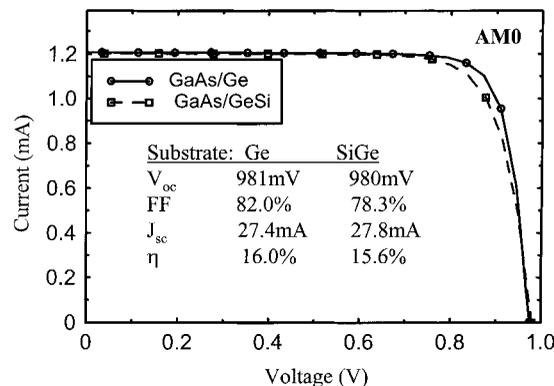


Figure 5. Calibrated AM0 light $I-V$ response for representative 0.2×0.2 cm single-junction p/n InGaP/GaAs cell grown on Ge/SiGe/Si and Ge substrate wafers. Efficiencies are based on total area

the theoretical curve of Figure 4 signifies that the performance of cells grown on SiGe virtual substrates is limited by dislocation-related recombination currents in the depletion region, with no apparent complications from other unaccounted defects or loss mechanisms. This is corroborated by dark I - V analysis that showed an increase in the diode ideality factor from ~ 1.5 to 2 for GaAs diodes grown on Ge and Ge/SiGe/Si substrates, respectively, which is probably responsible for the reduction in fill factor for the cells on Ge/SiGe/Si, as compared with those on Ge in Figure 5. It can be concluded that, at our current TDD values, the primary limitation on cell performance is simple depletion region recombination that impacts fill factor.

PERFORMANCE AND ANALYSIS OF GaAs/Ge/SiGe/Si CELLS

The light I - V data of Figure 5 were obtained on small-area, 0.2×0.2 cm cells, which suffered from a large front-contact grid coverage of $>10\%$, and a loss of J_{SC} due to incomplete carrier collection deep within the base that is a consequence of a wafer handling step between GaAs nucleation on the Ge/SiGe/Si substrate and growth of the complete cell by MOCVD for the devices reported here. This step is currently being eliminated from our initial process as we evolve our cell development program. The spectral response data of Figure 6 clearly shows the effect of the wafer handling step. The response for cells grown on Ge and SiGe, both of which received the same handling step, are identical, whereas the cell grown on a GaAs substrate that did not require wafer handling displays improved collection at long wavelengths. Calibrated AM0 light I - V measurements indicate a J_{SC} loss of ~ 1.7 mA/cm² as a result of this process. By accounting for this non-fundamental loss, and assuming a grid coverage of 4% typical for larger-area cells, single-junction AM0 efficiencies close to 20% are feasible at the V_{OC} values measured for these cells. Preliminary attempts to increase cell area are now in progress. Cells having areas of 0.6×0.6 cm (nine-fold increase in area) display improved J_{SC} due to decreased grid coverage from 10.5 to $\sim 8\%$, leading to an increase in J_{SC} from 28.5 mA/cm² to 29.7 mA/cm². Accounting for the J_{SC} loss from the wafer handling step leads to a realistically expected J_{SC} value of ~ 31 –32 mA/cm², which becomes 32–33 mA/cm² after reducing from metal grid coverage to 4%, identical to values expected for high efficiency ($> 20\%$ AM0) homoepitaxial GaAs cells. More impressive, however, given the historical limitation on V_{OC} , is that V_{OC} values of the larger-area cells are identical, and may even be slightly higher than the first series of small-area cells, indicating that incorporating more dislocations (but at the same dislocation density) within the active cell region does not impact performance, and that scaling to large cell areas should be feasible, this is currently under development.

To investigate whether the Ge cap of the virtual substrate generates a photoresponse within our measurements, since this is a well known issue for all III-V/Ge cells, a test set-up was assembled to measure the open-circuit photovoltage under filtered illumination that passes photons having energies less than the GaAs

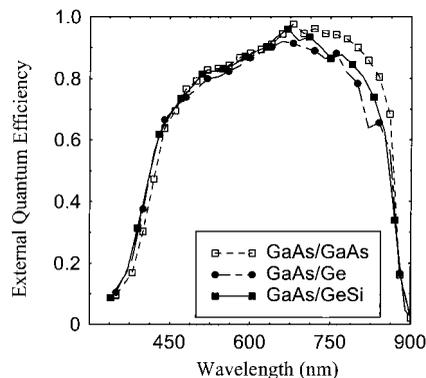


Figure 6. Spectral response results for identical InGaP/GaAs single-junction cell structures grown by MOCVD on GaAs, Ge and Ge/SiGe/Si substrates. Similar collection is seen for the cells on Ge and Ge/SiGe/Si and the reduction in quantum efficiency for these cells, as compared with the cell on GaAs, is due to growth interruption and wafer handling in our developing growth process

bandgap. A stack of conventional Si wafers or a thick (3 mm) Si wafer was inserted between a tungsten simulator lamp and the cells under test to filter out photons with wavelengths greater than 1050 nm. The V_{OC} values measured under the unfiltered tungsten lamp were comparable to V_{OC} values obtained under calibrated AM0 testing. A light shield was assembled to block any stray light from entering and skewing the experiment. Control tests made on homoepitaxial GaAs cells indicated that no photovoltage was generated underneath the Si long-pass filter stack. Another control experiment made on a bare Ge test cell revealed photovoltages of the order of 110–150 mV, confirming that the set-up should detect whether a buried Ge cell has been formed as a result of our GaAs/Ge/SiGe/Si process. The cells of Figure 5 were tested in this set-up, revealing a measured open-circuit photovoltage of 0.05 mV, equivalent to the noise floor measured for homoepitaxial GaAs cells, and insignificant with respect to the AM0 V_{OC} values, or 980 mV. To further verify this, and to ensure that systematic errors such as light leakage were not factors, a Ge wafer was inserted as a long-pass filter for both homoepitaxial and GaAs/Ge/SiGe/Si cells since in theory none of the junctions should produce a photovoltage under the Ge window, which blocks out wavelengths below ~ 1900 nm. The same noise floor result was obtained, confirming that the results presented here reflect the photoresponse of a single-junction GaAs cell grown on Ge/SiGe/Si substrates having a V_{OC} value of 980 mV, with no activity that can be associated with inadvertent sub-cell formation. This conclusion is consistent with our earlier findings from SIMS investigations that showed negligible interface diffusion of As, Ga and Ge after complete cell growth on Ge/SiGe/Si substrates, using the growth process we have described previously.^{10,11} Recently, however, we have fabricated p/n cells with even higher V_{OC} values, reaching up to 1030 mV and AM0 efficiencies as high as 17.1% with fill factors of 0.805 for 0.2×0.2 cm cells with the same current limitations (grid coverage) as those described here. This result is shown in Figure 7, along with a control cell grown on GaAs (the difference in J_{SC} as seen is due to the wafer handling issue discussed above). While impressive, there is evidence of slight Ge junction activity for this particular growth series, which appears to be due to inadvertent *p*-type doping of the Ge cap under the *n*-type GaAs base for these runs. Detailed analysis of these cells, the solution to this problem, and a complete description of the methodology to quantify buried junction activity will be presented in a forthcoming publication.¹⁵

CONCLUSION

High-performance GaAs single-junction solar cells have been fabricated on Si substrates with graded SiGe interlayers to achieve a virtual Ge substrate for high-quality InGaP/GaAs single-junction cell growth by MOCVD. Record high open-circuit voltages for single-junction GaAs cells on Si have been achieved, with

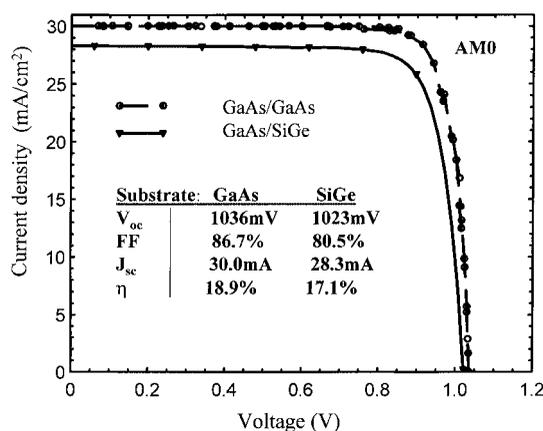


Figure 7. Calibrated AM0 light I - V response for a representative cell of a different series of InGaP/GaAs cell (0.2×0.2 cm) growths. The lower J_{SC} value is due to the wafer handling step. The high V_{OC} , now in excess of 1 V, but still below that of the GaAs/GaAs control, displays evidence of a very small sub-gap photoresponse, indicative of an active GaAs/Ge interface that is now under evaluation

values in excess of 980 mV under AM0 conditions, yielding AM0 cell efficiencies close to 16% for more than 50 cells to date. The high voltages were confirmed to be from a single GaAs junction by filtered light I - V experiments. The breakthrough V_{OC} values are directly related to achieving low TDD values, coupled with elimination of other severe loss mechanisms associated with anti-phase domains. Conservative calculations show that the efficiencies of these first prototype cells are limited by non-fundamental issues, a large grid obscuration ($>10\%$) and a loss in current output due to wafer handling during the growth sequence. Calculations that account for these losses predict that GaAs single-junction cell efficiencies between 19 and 20% (AM0) are already achievable with our current state of material quality. Identical V_{OC} and improved J_{SC} values, the latter by virtue of decreased front metal grid coverage, were obtained for our first generation of larger-area cells, indicating that scaling to large-area cell fabrication is feasible and imminent. Unlike all prior reports on p/n GaAs/Si cells, cell V_{OC} values for the first time match a simple theory where cell V_{OC} is limited only by depletion region recombination due to the presence of a low dislocation density, and not by other unaccounted-for material defects and quality issues that have drastically lowered V_{OC} values in the past. These results also confirm that the record high minority-carrier lifetimes and TDD values for GaAs grown on Ge/SiGe/Si reported in earlier publications are reflected in completed solar cells, indicating the robust nature of the GaAs/Ge/SiGe/Si heterostructure.

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