

# Gate length scaling study of InAlAs/InGaAs/InAsP composite channel HEMTs

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Received 14 April 2006; received in revised form 28 March 2007; accepted 15 April 2007

The review of this paper was arranged by Prof. A. Zaslavsky

## Abstract

The dependence of direct current and microwave performance of InGaAs/InAsP composite channel HEMTs on gate length is presented experimentally. Composite channel HEMTs with gate length from 1.13  $\mu\text{m}$  to 0.15  $\mu\text{m}$  were fabricated. Device characterization results showed the extrinsic transconductance increased from 498 mS/mm for 1.13  $\mu\text{m}$  devices to 889 mS/mm for 0.15  $\mu\text{m}$  gate devices, while the unity current gain cutoff frequency increased from 24 GHz to 190 GHz. A simple delay time analysis is employed to extract the effective carrier velocity ( $v_{\text{eff}}$ ) of the composite channel. The  $v_{\text{eff}}$  is determined to be  $1.9 \times 10^7$  cm/s. To our knowledge, this is the first systematic study on gate length scaling effect of composite channel HEMTs.

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*Keywords:* InP; InAsP; High electron mobility transistors; Composite channel

## 1. Introduction

InP-based InAlAs/InGaAs high electron mobility transistors (HEMTs) have demonstrated excellent high frequency and low noise performances. However, because of the small band gap of InGaAs channel, they suffer from strong impact ionization in the channel layer such as kink effect and low on-state breakdown voltage. To improve the device breakdown performance, larger bandgap materials such as InP and InAsP have been used as the channel materials for HEMT devices [1–3]. However, the electron mobility in InP and InAsP is lower than that in InGaAs. Therefore, to utilize the high mobility in InGaAs and high breakdown field in InP and InAsP, composite channel HEMTs in which the channel is consisted of InGaAs with high mobility and a sub-channel with high breakdown field

have been proposed to improve the breakdown voltage and power performance [4–8]. Under a low electric field, electron transport is confined in the high mobility InGaAs main channel. Under a high electric field, electrons gain enough energy to transfer into the sub-channel, which has a larger bandgap thus higher breakdown field. Materials that have been considered for the sub-channel include InP [4], InAsP [5] and InGaAs with lower indium composition [6]. InP so far has received most of the research attention [4,7,8]. However, InAsP is more preferable as compared with InP because it has a smaller conduction band offset at the InGaAs/InAsP interface, thus electrons can be more easily transferred into the InAsP sub-channel. Also, the composition of InAsP can be varied to optimize device performance. We have reported 0.25  $\mu\text{m}$  In<sub>0.52</sub>Al<sub>0.48</sub>As/In<sub>0.53</sub>Ga<sub>0.47</sub>As/InAs<sub>0.3</sub>P<sub>0.7</sub> composite channel HEMTs with a unity current gain cutoff frequency ( $f_T$ ) of 115 GHz [9]. In this paper, we present a systematic study on the gate length scaling of In<sub>0.53</sub>Ga<sub>0.47</sub>As/InAs<sub>0.3</sub>P<sub>0.7</sub> composite channel HEMTs. The performances of device with gate lengths ranging from

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1.13  $\mu\text{m}$  to 0.15  $\mu\text{m}$  are reported. Electron saturation velocity is extracted and compared based on the delay time analysis.

## 2. Device structure and fabrication

The epilayer structure in this study was grown by a 2-inch Varian Gen II molecular beam epitaxy (MBE) system at a substrate temperature of 520  $^{\circ}\text{C}$ . Molecular forms of  $\text{As}_2$  and  $\text{P}_2$  were generated from valved cracker sources for arsenic and phosphorus, respectively. On the Fe-doped semi-insulating (100) InP substrate, an  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  buffer with InGaAs/InAlAs superlattices was first grown. The channel consisted of, from bottom to top, 40  $\text{\AA}$  of strained  $\text{InAs}_{0.3}\text{P}_{0.7}$  doped to  $2 \times 10^{18} \text{ cm}^{-3}$ , 40  $\text{\AA}$  of undoped  $\text{InAs}_{0.3}\text{P}_{0.7}$  and 70  $\text{\AA}$   $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , followed by 30  $\text{\AA}$  thick  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  spacer, Si-planar doping ( $6 \times 10^{12} \text{ cm}^{-2}$ ) and 100  $\text{\AA}$   $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  Schottky barrier layer. A thin layer (60  $\text{\AA}$ ) of InP is used as the etching stop layer to improve uniformity of gate recess etching. Finally, a 400  $\text{\AA}$  heavily doped  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  ( $1 \times 10^{19} \text{ cm}^{-3}$ ) cap layer was grown for Ohmic contacts. The doping in the bottom  $\text{InAs}_{0.3}\text{P}_{0.7}$  channel layer was designed to: (1) act as an extra carrier contribution layer to increase the sheet electron density in the 2-dimensional electron gas (2DEG); and (2) adjust the conduction band edge to form a triangle quantum well at the  $\text{InAs}_{0.3}\text{P}_{0.7}$  and  $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$  interface. From the Vegard's law, the amount of compressive strain is around 0.97% at this arsenic composition. Hall measurement showed that the layer had a two-dimensional sheet carrier density of  $3 \times 10^{12} \text{ cm}^{-2}$  and a Hall electron mobility of 7300  $\text{cm}^2/\text{Vs}$  at room temperature.

The device fabrication started with mesa isolation by dry etching using  $\text{Cl}_2/\text{Ar}$  plasma in an inductively coupled plasma reactive ion etching system (ICP–RIE). Ge/Au/Ni/Au Ohmic contacts with Ge to Au atomic ratio of 12% were deposited by electron beam evaporation and annealed at 360  $^{\circ}\text{C}$  for 1 min in a furnace in  $\text{N}_2$  ambient. Using transmission line model technique, Ohmic contact resistance is determined to be 0.03  $\Omega \text{ mm}$ . The specific contact resistivity is  $1.2 \times 10^{-7} \Omega \text{ cm}^{-2}$ . Mushroom shaped gate with different lengths were patterned using a tri-layer resist scheme by electron beam lithography followed by a two-step gate recess etching process. The InGaAs contact cap was first etched using a selective etchant of citric acid/ $\text{H}_2\text{O}_2$  mixture. Then the InP etching stop layer was removed by Ar plasma in ICP–RIE. Finally, Ti/Pt/Au was deposited as Schottky gate contacts. The actual gate lengths of devices are 0.15, 0.34, 0.58, 0.85 and 1.13  $\mu\text{m}$ , respectively. The devices are not passivated. The drain to source spacing is 2  $\mu\text{m}$ . The device gate width is 100  $\mu\text{m}$ .

## 3. Results and discussion

The DC characteristics of the composite channel HEMTs were measured on wafer using an Agilent 4156 Semiconductor Parameter Analyzer. Fig. 1a shows the typ-

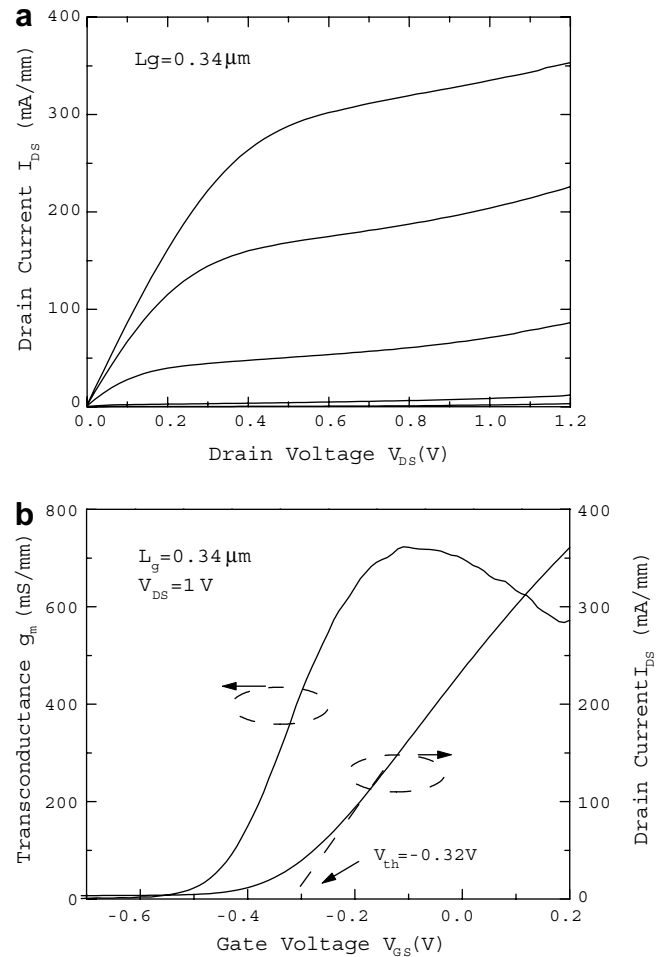


Fig. 1. (a) The current–voltage characteristics of a typical composite channel HEMT with  $L_g = 0.34 \mu\text{m}$  and  $W_g = 100 \mu\text{m}$ . The gate–bias was swept from  $-0.6 \text{ V}$  to  $0.2 \text{ V}$  in a step of  $0.2 \text{ V}$ . (b) Extrinsic transfer characteristics of a typical composite channel HEMT with  $L_g = 0.34 \mu\text{m}$  and  $W_g = 100 \mu\text{m}$  at  $V_{ds} = 1 \text{ V}$ .

ical  $I$ – $V$  characteristics of 0.34  $\mu\text{m}$  gate devices. No kink effect is observed in the  $I$ – $V$  characteristics, which is a clear sign that the impact ionization in  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  is successfully suppressed by the  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InAs}_{0.3}\text{P}_{0.7}$  composite channel structure. The maximum drain current is measured to be 353  $\text{mA}/\text{mm}$  at bias of  $V_{ds} = 1.2 \text{ V}$  and  $V_{gs} = 0.2 \text{ V}$ . The devices are well pinched off at  $V_{gs} = -0.5 \text{ V}$ . Extrinsic transfer characteristic at  $V_{ds} = 1 \text{ V}$  for a device with 0.34  $\mu\text{m}$  gate length is shown in Fig. 1b. The threshold voltage, which is defined as the gate–bias intercept by linearly extrapolating drain current curve from the peak  $g_m$  position in transfer characteristics, is determined to be  $-0.32 \text{ V}$ . The DC parameters of devices with different gate lengths are compared. When the gate length shrank from 1.13  $\mu\text{m}$  to 0.15  $\mu\text{m}$ , the maximum current increased from 179  $\text{mA}/\text{mm}$  (bias at  $V_{ds} = 2 \text{ V}$ ,  $V_{gs} = 0.2 \text{ V}$ ) to 421  $\text{mA}/\text{mm}$  (bias at  $V_{ds} = 1 \text{ V}$ ,  $V_{gs} = 0.2 \text{ V}$ ). The threshold voltage shifted from  $-0.14 \text{ V}$  to  $-0.32 \text{ V}$ . Fig. 2 shows the dependence of maximum extrinsic transconductance ( $g_m$ ) on gate. The peak  $g_m$  values range from

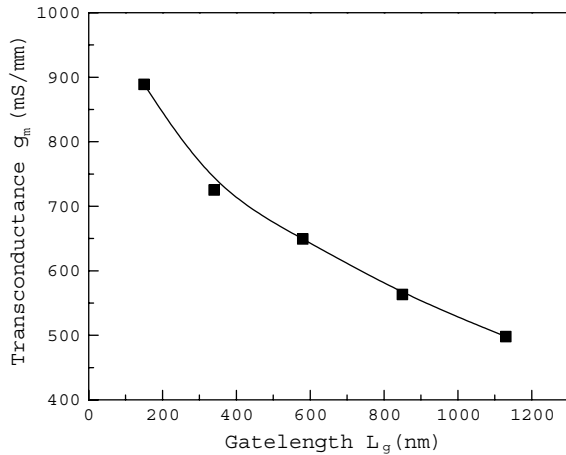


Fig. 2. Dependence of peak extrinsic transconductance on gate length.

498 mS/mm for 1.13  $\mu\text{m}$  devices to 889 mS/mm for 0.15  $\mu\text{m}$  devices.

The microwave characterization of the devices was performed on-wafer by  $S$ -parameter measurement with an Agilent 8510C network analyzer from 1 GHz to 40 GHz. The  $f_T$  and maximum oscillation frequency ( $f_{\text{max}}$ ) were determined by extrapolating the  $|H_{21}|^2$  and maximum available gain (MAG)/maximum stability gain (MSG) at a  $-20$  dB/decade slope using least square fitting. Fig. 3 shows the dependence of  $f_T$  and  $f_{\text{max}}$  on gate length. The  $f_T$  increases exponentially from 24 GHz to 190 GHz with the gate length decreasing from 1.13  $\mu\text{m}$  to 0.15  $\mu\text{m}$ . The  $f_{\text{max}}$  values range from 54 GHz to 150 GHz for devices with the same gate length range. The inset is a typical microwave characteristics with  $f_T = 86$  GHz and  $f_{\text{max}} = 110$  GHz for the 0.34  $\mu\text{m}$  gate length devices.

To estimate the saturation electron velocity in the composite channel layer, a simple delay time analysis is employed [10]. The total delay time  $\tau_{\text{total}}$  can be calculated by:

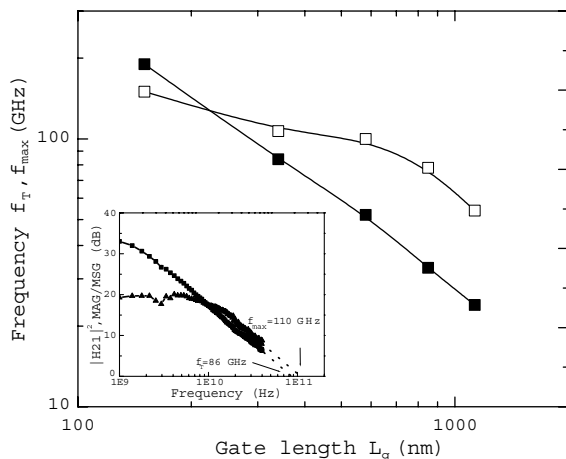


Fig. 3. Dependence of  $f_T$  (filled) and  $f_{\text{max}}$  (hollow) on gate length. Inset: microwave performance of 0.34  $\mu\text{m}$  gate length HEMT. Extrapolation at 20 dB/decade gives  $f_T = 86$  GHz and  $f_{\text{max}} = 110$  GHz.

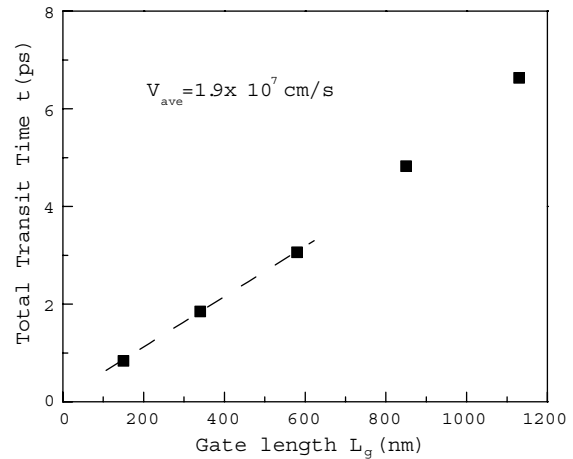


Fig. 4. Dependence of total delay time on gate length of InGaAs/InAsP composite channel HEMTs.

$$\tau_{\text{total}} = \frac{1}{2\pi f_T} = \tau_{\text{cc}} + C_{\text{gd}}(R_s + R_d) + \frac{\Delta L}{v_{\text{eff}}} + \frac{L_g}{v_{\text{eff}}} = \tau_{\text{cc}} + \frac{L_g}{v_{\text{eff}}}. \quad (1)$$

Here  $\Delta L$  is the extension of the effective gate length and is treated as a constant in this range of gate length,  $v_s$  is the effective carrier velocity in the channel,  $\tau_{\text{cc}}$  is the channel charging time, and  $C_{\text{gd}}$  is the feed back capacitance and the  $R_s$  and  $R_d$  are parasitic source and drain resistance. By plotting the  $\frac{1}{2\pi f_T}$  as a function of gate length, we can extract the effective carrier velocity ( $v_s$ ) and  $\tau_{\text{cc}}$  from the slope and intercept of linear fitting. Fig. 4 shows the dependence of  $\tau_{\text{total}}$  on gate length. In the  $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}/\text{InAs}_{0.3}\text{P}_{0.7}$  composite channel, a larger critical field is expected than that in  $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}$  ( $\sim 5$  kV/cm). So, the onset gate length of the saturation velocity model could be much shorter than the case of  $\text{In}_{0.52}\text{Ga}_{0.48}\text{As}$  channel [11]. The  $\tau_{\text{total}}$  for 0.15, 0.34 and 0.58  $\mu\text{m}$  gate devices were used in the calculation. The  $v_s$  is estimated to be  $1.9 \times 10^7$  cm/s, while  $\tau_{\text{cc}}$  is 0.74 ps. Despite the excellent  $f_T$  and  $f_{\text{max}}$  performance, as expected, the effective carrier velocity of our  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InAs}_{0.3}\text{P}_{0.7}$  composite channel HEMTs is lower than the reported value ( $2.7 \times 10^7$  cm/s) for lattice-matched  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  single-channel HEMTs [10,12], but close to the reported value ( $2.1 \times 10^7$  cm/s) for pseudomorphic  $\text{InAs}_{0.6}\text{P}_{0.4}$  single-channel devices [1]. It is most likely due to the n-type doping in the bottom layer of composite channel, which introduces ionized impurity scattering.

#### 4. Conclusion

The dependence of direct current and microwave performance of  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InAs}_{0.3}\text{P}_{0.7}$  composite channel HEMTs on gate length is presented. Composite channel HEMTs with gate lengths from 1.13  $\mu\text{m}$  to 0.15  $\mu\text{m}$  have been fabricated and characterized. The devices exhibited an extrinsic transconductance of 498 mS/mm for 1.13  $\mu\text{m}$  devices, and 889 mS/mm for 0.15  $\mu\text{m}$  devices. The  $f_T$  values

range from 24 GHz to 190 GHz and the  $f_{\max}$  values are in the range of 54–150 GHz. The effective carrier velocity extracted based on the delay time method is  $1.9 \times 10^7$  cm/s. To our knowledge, this is the first report of gate length scaling study on the performance of composite-channel HEMTs.

### Acknowledgement

This work was supported by National Science Foundation FRG Grant DMR-0313468.

### References

- [1] Hong W-P, Hayes JR, Bhat R, Lin PSD, Nguyen C, Lee HP, et al. Novel pseudomorphic InP/InAs<sub>0.6</sub>P<sub>0.4</sub> quantum-well HEMT's. *Int Electr Dev Meet Tech Dig* 1991;243–6.
- [2] Medjdoub F, Zaknounge M, Wallart X, Gaquiere C, Dessenne F, Thobel J-L, et al. InP HEMT downscaling for power applications at W band. *IEEE Trans Electr Dev* 2005;52:2136–43.
- [3] Medjdoub F, Zaknounge M, Wallart X, Gaquiere C, Theron D. 94 GHz high power performances of InAs<sub>0.4</sub>P<sub>0.6</sub> channel HEMTs on InP. *Electr Lett* 2005;41:769–71.
- [4] Enoki T, Arai K, Kohzen A, Ishii Y. InGaAs/InP double channel HEMT on InP. *Proceedings of 4th InP related materials conference*; 1992;14–7.
- [5] Ouchi K, Mishima T, Kudo M, Ohtal O. Gas-source molecular beam epitaxy growth of metamorphic InP/In<sub>0.5</sub>Al<sub>0.5</sub>As/In<sub>0.5</sub>Ga<sub>0.5</sub>As/InAsP high-electron-mobility structures on GaAs substrates. *Jpn J Appl Phys* 2002;41:1004–7.
- [6] Chertouk M, Heiss H, Xu D, Kraus S, Klein W, Bohm G, et al. Metamorphic InAlAs/InGaAs HEMTs on GaAs substrates with a novel composite channels design. *IEEE Electr Dev Lett* 1996;17:273–5.
- [7] Meneghesso G, Neviani A, Oesterholt R, Matloubian M, Liu T, Brown T, et al. On-state and off-state breakdown in GaInAs/InP composite-channel HEMTs with variable GaInAs channel thickness. *IEEE Trans Electr Dev* 1999;346:2–9.
- [8] Boudrissa M, Delos E, Wallaert X, Theron D, Jaeger J. A 0.15- $\mu$ m 60-GHz high-power composite channel GaInAs/InP HEMT with low gate current. *IEEE Electr Dev Lett* 2000;22:257–9.
- [9] Liu D, Hudait M, Lin Y, Kim H, Ringel SA, Lu W. In<sub>0.53</sub>Ga<sub>0.47</sub>As/InAs<sub>0.3</sub>P<sub>0.7</sub> composite channel high electron mobility transistors. *Electr Lett* 2006;42:307–9.
- [10] Suemitsu T, Enoki T, Yokoyama H, Ishii Y. Improved recessed-gate structure for sub-0.1- $\mu$ m-gate InP-based high electron mobility transistors. *Jpn J Appl Phys* 1998;37:1365–72.
- [11] Enoki T, Arai K, Ishii Y. Delay time analysis for 0.4 to 5- $\mu$ m-gate InAlAs-InGaAs HEMTs. *IEEE Electr Dev Lett* 1990;11:502–4.
- [12] Enoki T, Tomizawa M, Umeda Y, Ishii Y. 0.05- $\mu$ m-gate InAlAs/InGaAs high electron mobility transistor and reduction of its short-channel effects. *Jpn J Appl Phys* 1994;33:798–803.