Ultrahigh-Speed 0.5 V Supply Voltage $In_{0.7}Ga_{0.3}As$ Quantum-Well Transistors on Silicon Substrate

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***Abstract*—The direct epitaxial growth of ultrahigh-mobility InGaAs/InAlAs quantum-well (QW) device layers onto silicon substrates using metamorphic buffer layers is demonstrated for the first time. In this letter, 80 nm physical gate length depletion-mode InGaAs QW transistors with saturated transconductance g_m of 930 $\mu S/\mu m$ and f_T of 260 GHz at $V_{DS} = 0.5$ V are achieved on 3.2 μm thick buffers. We expect that compound semiconductor-based advanced QW transistors could become available in the future as very high-speed and ultralow-power device technology for heterogeneous integration with the mainstream silicon CMOS.**

***Index Terms*—Heterogeneous integration, InGaAs/InAlAs, low power, quantum-well (QW) devices, silicon, III–V materials.**

I. Introduction

CONTINUED physical scaling of mainstream silicon CMOS technology following Moore's Law has resulted in unprecedented increase in single-core and multicore performance of modern-day microprocessors. However, the rising gate count on a single chip has also increased the power consumption, making the performance per watt as the key figure-of-merit for today's high-performance microprocessors. Energy efficiency is the central tenet of today's high-performance microprocessor technology at both the architectural level and discrete transistor level. Supply voltage scaling while maintaining the transistor and circuit performance is an obvious route in reducing the overall power dissipation. To that effect, compound semiconductor-based quantum-well (QW) transistors provide a promising device option, since III–V semiconductors have excellent low-field and high-field electron transport properties resulting in ultrahigh-speed switching at very low supply voltages [1]. Deep submicrometer gate length $In_{0.7}Ga_{0.3}As$ high electron mobility transistors (HEMTs), with current gain cutoff frequency of 562 GHz [2], intrinsic gate delay of 0.42 ps, I_{ON}/I_{OFF} ratios in excess of 10^5, and subthreshold slope of 90 mV/dec, have been experimentally demonstrated [3], [4] at 0.7-V supply voltage. When benchmarked against the state-of-the-art silicon MOSFETs, these devices exhibited more than an order of magnitude improvement in energy-delay product, confirming their potential for ultrahigh-speed low-power logic applications [4]. However, there remain several significant challenges prior to the implementation of III–V materials for logic [5], including their heterogeneous integration with the Si substrate. A seamless robust heterogeneous integration of high-performance $In_{0.7}Ga_{0.3}As$ QW transistors on Si substrate would avoid the prohibitively expensive need in developing large diameter (300 mm and beyond) InP or GaAs substrates, significantly reduce manufacturing costs, and realize the ultimate vision of high switching activity factor low-voltage high-speed III–V-based logic circuit blocks coupled with the functional density advantages provided by the Si CMOS platform.

In this letter, we report on the heteroepitaxial growth of high-mobility and low dislocation density modulation-doped $In_{0.7}Ga_{0.3}As$ metamorphic QW device layers on silicon substrate. The electrical characteristics of the $In_{0.7}Ga_{0.3}As$ epilayers and the RF and dc performance of 80 nm physical gate length transistors fabricated from this material are presented.

II. Materials Growth and Device Fabrication

$In_{0.7}Ga_{0.3}As$ epitaxial QW transistor structures were grown on 4° off-axis (100) p-type Si substrates using metamorphic GaAs and $In_xAl_{1-x}As$ buffer layers grown using solid source molecular beam epitaxy (MBE). The significance of using wide band-gap materials for the buffer layers is to reduce the residual carrier concentration, provide high resistivity buffer for device isolation, and reduce junction leakage. The buffer layers also need to have low dislocation density at the end of grading and an atomically smooth surface template for active device layer growth. The epitaxial structure used in this letter consists of a 2-μm GaAs buffer layer, 1.2-μm $In_xAl_{1-x}As$ buffer [6], 13-nm pseudomorphic $In_{0.7}Ga_{0.3}As$ channel layer, 5-nm $In_{0.52}Al_{0.48}As$ spacer layer, Si delta-doping ($5-8 \times 10^{12}$ cm^{-2}), 8-nm $In_{0.52}Al_{0.48}As$ barrier layer, 6-nm InP etch stop layer, and a 20-nm Si-doped ($1-2 \times 10^{19}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ cap layer which are grown on Si substrate. The InGaAs channel with high indium content (0.7) is limited to 13 nm in thickness to prevent strain relaxation and allow the formation of 2-D electron gas in the high indium content channel. The TEM micrograph of Fig. 1 shows a high contrast at the graded buffer layers with no discernable threading dislocations observable in the $\mathbf{In_{0.7}Ga_{0.3}As}$ QW. As shown in Fig. 1(b), the active channel $\mathbf{In_{0.7}Ga_{0.3}As}$ is coherently strained to the metamorphic buffer layer and virtually defect-free except for a residual amount of threading dislocations

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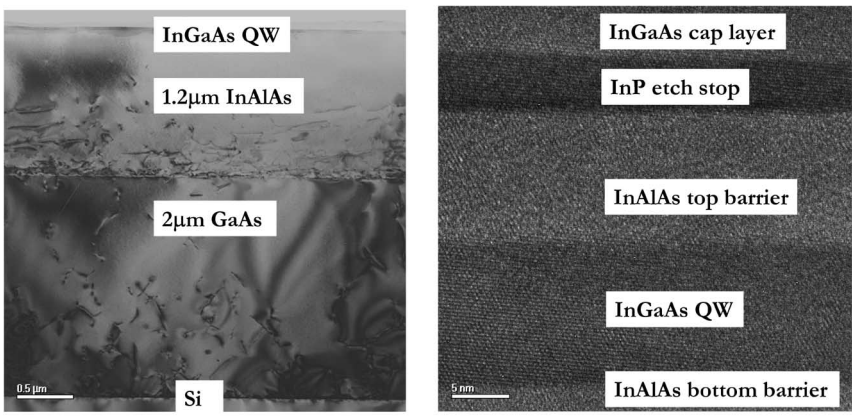

Fig. 1. Cross-sectional TEM images of $In_{0.7}Ga_{0.3}As$ QW structures on Si using metamorphic buffer architecture: (a) Entire layer structure. (b) High magnification of $In_{0.7}Ga_{0.3}As$ QW along with bottom and top barrier layers. The misfit dislocations are predominantly contained in the buffer layer.

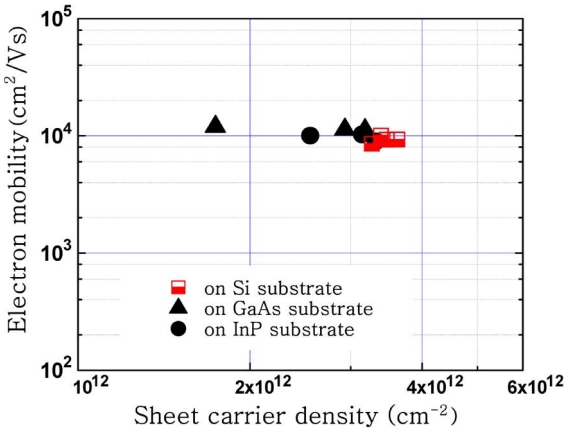

Fig. 2. Electron mobility versus sheet carrier density in n-channel $In_{0.7}Ga_{0.3}As$ QW device layers grown on Si, GaAs, and InP substrates. In all cases, $In_{0.52}Al_{0.48}As$ is the bottom and top barrier layer.

which could not be determined from the cross-sectional TEM image analysis. Single field Hall mobility measurements using the Van der Pauw method and field-dependent quantitative mobility spectrum analysis were carried out at both 77 K and 300 K to ascertain the electrical qualities (mobility and sheet carrier density) of the films before proceeding with device fabrication. The Hall mobilities were measured at 300 K to be 9000–10 000 $cm^2/V \cdot s$ for the sheet carrier concentrations in the range of $3.3-3.6 \times 10^{12}$ cm^{-2} and about 25 000 $cm^2/V \cdot s$ at 77 K for sheet carrier density of 3.2×10^{12} cm^{-2}. These mobility values are comparable to the metamorphic and pseudomorphic $In_{0.7}Ga_{0.3}As$ HEMT structures grown previously on GaAs and InP substrates, respectively, as illustrated in Fig. 2 [7], [8].

Depletion-mode $In_{0.7}Ga_{0.3}As$ HEMTs were fabricated using the material grown onto the Si substrate. Source and drain ohmic contacts were first defined using e-beam lithography and e-beam evaporated using NiGeAu. The contacts were annealed at 400 °C for 30 s. The source–drain separation was 0.75 μm. CrAu Schottky gates were then defined using the e-beam lithography and recessed down to the InP etch stop using citric acid and hydrogen peroxide wet etch chemistry. A wet etch using phosphoric acid, hydrogen peroxide, and DI water was used to perform mesa isolation and to leave air-bridged gate and drain metal feeds.

III. DC Characteristics

Typical output and transfer characteristics obtained for the 80 nm physical gate length $\mathbf{In_{0.7}Ga_{0.3}As}$ QW transistors that are fabricated from 3.2 μm buffer material on Si are shown in Fig. 3(a) and (b), respectively. The device is a depletion mode with a threshold voltage V_T of -0.56 V and a peak transconductance g_m of 930 $\mu S/\mu m$ at $V_{DS} = 0.5$ V. The negative threshold voltage is expected due to the large gate-to-channel separation distance of 19 nm. The subthreshold slope was 155 mV/decade, and the drain-induced barrier lowering (DIBL) value was 150 mV/V at $V_{DS} = 0.5$ V. Inversion mode surface channel silicon NMOS transistors with 80 nm physical gate length will exhibit a subthreshold slope of 80 mV/decade and DIBL of less than 60 mV/V at $V_{DS} = 1.3$ V [1]. Further reduction of the gate-to-channel distance by recess etching of the top $\mathbf{In_{0.52}Al_{0.48}As}$ barrier, including the InP etch stop layer prior to Schottky gate metal formation, will improve short channel effects in these $In_{0.7}Ga_{0.3}As$ QW transistors and result in enhancement mode transistor operation. The dc performance of the $\mathbf{In_{0.7}Ga_{0.3}As}$ QW transistors fabricated here on Si is very similar to the depletion-mode pseudomorphic $\mathbf{In_{0.7}Ga_{0.3}As}$ HEMTs fabricated previously on InP substrates with similar gate-to-channel separation [3].

IV. RF Performance

S-parameter measurements were performed at frequencies up to 50 GHz using an HP 8510C network analyzer. The Si wafer resistivity was 5–20 $\Omega \cdot$ cm, and short/open on-wafer deembedding structures were used to determine the parasitic capacitance of the probe pads and to deembed the short circuit current gain $|h_{21}|$. Extrapolating the deembedded data from 40 GHz at -20 dB/dec resulted in f_T of 260 GHz at $\mathbf{V_{DS}} = 0.5$ V. Fig. 4 shows a plot of the intrinsic cutoff frequency as a function of the dc power dissipation of 80 nm L_g $\mathbf{In_{0.7}Ga_{0.3}As}$ HEMTs on both InP [3], [4] and Si

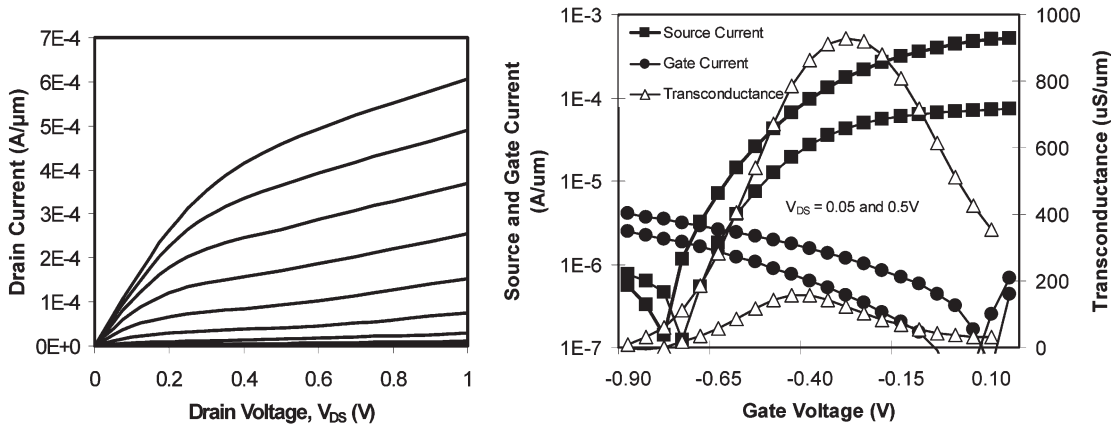

Fig. 3. (a) Output characteristic for 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistor on 3.2-μm metamorphic buffer on silicon (gate voltage V_G is swept from 0.0 to -0.8 V in -0.1-V steps). (b) Transfer characteristic for 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistor on 3.2-μm buffer on silicon with $V_{\rm DS} = 0.5$ and 0.05 V. Peak transconductance $g_{\rm m}$ for this device was 930 $\mu S/\mu m$ at $V_{\rm DS} = 0.5$ V.

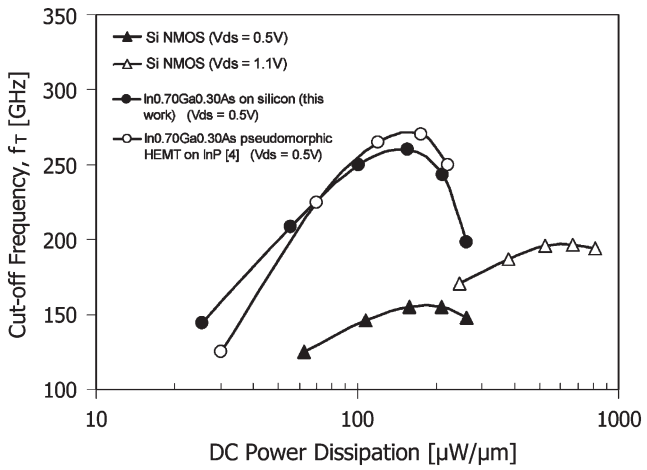

Fig. 4. Plot of deembedded unity gain cutoff frequency as a function of dc power dissipation for 0.5-V $V_{\rm DS}$ 80-nm L_g $In_{0.7}Ga_{0.3}As$ QW transistors on both silicon and InP substrates, benchmarked against 60-nm L_g silicon NMOS transistors at $V_{\rm DS} = 0.5$ and 1.1 V.

substrates, and it is compared with the 60-nm L_g silicon NMOS transistors. The $\mathbf{In_{0.7}Ga_{0.3}As}$ on Si QW transistors along with the pseudomorphic $\mathbf{In_{0.7}Ga_{0.3}As}$ on InP HEMTs show over $10\times$ reduction in dc power dissipation at the same performance or $2\times$ gain in performance at the same power compared to the silicon NMOS transistors. The RF performance of the metamorphic $\mathbf{In_{0.7}Ga_{0.3}As}$ on Si QW transistors closely matches that of the pseudomorphic devices previously demonstrated on semi-insulating InP substrates [3], [4].

V. Conclusion

In conclusion, high-quality $\mathbf{In_{0.7}Ga_{0.3}As}$ metamorphic QW structures on Si substrates have been grown using solid source MBE with excellent electrical properties with a total buffer thickness of 3.2 μm. Depletion-mode $In_{0.7}Ga_{0.3}As$ transistors fabricated from this material exhibit a saturated peak transconductance of 930 $\mu S/\mu m$ and intrinsic f_T of 260 GHz at 0.5 V $V_{\rm DS}$. These heterogeneous III–V transistors on silicon substrate show performance characteristics equal to those previously achieved on pseudomorphic $\mathbf{In_{0.7}Ga_{0.3}As}$ HEMTs on InP substrate. In this letter, we have presented a feasibility demonstration of the future heterogeneous integration of ultrahigh-speed low supply voltage $\mathbf{In_{0.7}Ga_{0.3}As}$ transistors onto silicon substrate.

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