Carrier Transport in High-Mobility III–V Quantum-Well Transistors and Performance Impact for High-Speed Low-Power Logic Applications

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***Abstract*—DC and high-frequency device characteristics of $In_{0.7}Ga_{0.3}As$ and InSb quantum-well field-effect transistors (QWFETs) are measured and benchmarked against state-of-the-art strained silicon (Si) nMOSFET devices, all measured on the same test bench. Saturation current (I_{on}) gain of 20% is observed in the $In_{0.7}Ga_{0.3}As$ QWFET over the strained Si nMOSFET at $(V_g - V_t) = 0.3$ V, $V_{ds} = 0.5$ V, and matched I_{off}, despite higher external resistance and large gate-to-channel thickness. To understand the gain in I_{on}, the effective carrier velocities (ν_{eff}) near the source-end are extracted and it is observed that at constant $(V_g - V_t) = 0.3$ V and $V_{ds} = 0.5$ V, the ν_{eff} of $In_{0.7}Ga_{0.3}As$ and InSb QWFETs are 4–5× higher than that of strained silicon (Si) nMOSFETs due to the lower effective carrier mass in the QWFETs. The product of ν_{eff} and charge density (n_s), which is a measure of "intrinsic" device characteristics, for the QWFETs is 50%–70% higher than strained Si at low-voltage operation despite lower n_s in QWFETs. Calibrated simulations of $In_{0.7}Ga_{0.3}As$ QWFETs with reduced gate-to-channel thickness and external resistance matched to the strained Si nMOSFET suggest that the higher ν_{eff} will result in more than 80% I_{on} increase over strained Si nMOSFETs at $V_{ds} = 0.5$ V, $(V_g - V_t) = 0.3$ V, and matched I_{off}, thus showing promise for future high-speed and low-power logic applications.**

***Index Terms*—Effective carrier velocity, InGaAs, InSb, quantum-well devices, silicon, III–V materials.**

I. Introduction

As SILICON CMOS technology continues to scale in accordance with Moore's Law, energy efficiency becomes increasingly important. A common method of curtailing the rising power consumption that accompanies an increasing number of transistors per chip is to scale supply voltage while maintaining transistor and circuit performance. III–V compound semiconductor-based quantum-well field-effect transistors (QWFETs) have been proposed as a promising device option because of high-speed switching at very low supply voltages enabled by the excellent low- and high-field electron transport properties of III–V semiconductors [1]. At supply voltages of less than 0.7 V, III–V QWFETs have shown a significant reduction in energy-delay product compared to state-of-the-art silicon nMOSFETs [2], [3]. To quantify the power-performance advantage of short channel III–V devices with respect to current state-of-the art strained Si, we investigate the role of effective carrier velocity in the channel and its impact on transistor drive current.

In this letter, effective carrier velocities at the source end of $In_{0.7}Ga_{0.3}As$ and InSb QWFETs are extracted and benchmarked against state-of-the-art strained Si nMOSFETs. These Si devices incorporate high-κ and metal gates [4]. DC and high-frequency device characteristics of QWFETs are also analyzed and benchmarked against the strained Si nMOSFETs all measured on the same test bench. Both measurement and simulation data are used to show the potential drive current benefits of $In_{0.7}Ga_{0.3}As$ QWFETs over Si at low-voltage operation.

II. Effective Carrier Velocity and Its Extraction

Effective carrier velocity (ν_{eff}) is determined from the intrinsic saturated transconductance and capacitance [5]

$$\nu_{eff} = g_{mi}/(WC_{gi}) \tag{1}$$

where g_{mi} is the saturated transconductance corrected for parasitic resistance (R_{sd}), W is the width of the device, and C_{gi} is the intrinsic gate capacitance per unit area. The value of C_{gi} for III–V devices cannot directly be measured since they use Schottky gates. In this letter, both C_{gi} and g_{mi} for both the Si and III–V devices are determined using high-frequency measurements and a small signal equivalent circuit model [6], [7]. The high-frequency response was measured from 1 to 50 GHz. Fig. 1(a) shows that the simulated S parameters based on the small signal equivalent circuit model are equivalent to the measured S parameters, and that the measured and extracted gate-source capacitance (C_{gs}) is independent of frequency. The rms error of less than 2% between measured and modeled S parameters, and the frequency independent signature of small signal circuit elements allow for accurate extraction of g_{mi} and the total gate capacitance $(C_{gs} + C_{gd})$, where (C_{gd}) is the gate-drain capacitance. C_{gi} is determined from the slope of

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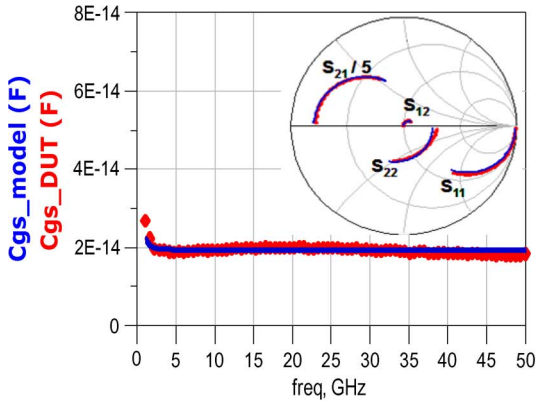

(a)

	V_{ds}	V_g-V_t	Cgi @ V_{ds}=0.05V	n_s	g_m	g_{mi}
Material System	[V]	[V]	[μF/cm²]	[n_s/cm²]	[μS/μm]	[μS/μm]
InGaAs_T_{ins} = 8nm	0.5	0.3	0.78	7.9E+11	1245	1650
InGaAs_T_{ins} = 6nm	0.5	0.3	0.94	9.6E+11	1400	2190
InSb_T_{ins} = 9nm	0.5	0.3	0.55	6.2E+11	903	1620
Strained Si	0.5	0.3	2.54	2.8E+12	1210	1450

(b)

Fig. 1. (a) Inset depicts simulated S parameters based on the small signal equivalent circuit model compared to the measured S parameters from 1 to 50 GHz. Gate to source capacitances $(C_{\rm gs})$ simulated by the circuit model and extracted from the measured S parameters of the device are shown to be independent of frequency. The rms error of less than 2% between measured and modeled S parameters and the frequency independent signature of all small signal circuit elements allow for accurate extraction of $g_{\rm mi}$ and $C_{\rm gi}$. (b) Table shows the bias conditions, $C_{\rm gi}$, n_s as defined by $(C^*_{\rm gi}(V_g - V_t)/{\rm q})$, measured g_m, and $g_{\rm mi}$ of the different material systems at a constant DIBL of 150 mV/V ± 5 mV/V.

$(C_{\rm gs} + C_{\rm gd})/W$ versus the various physical gate lengths of the devices. The table in Fig. 1(b) shows the bias conditions, $C_{\rm gi}$, n_s, measured g_m, and extracted $g_{\rm mi}$ of the different material systems. The larger correction from g_m to $g_{\rm mi}$ in the III–V QWFET cases compared to the strained Si is due to 2–3× higher total external resistance $(R_{\rm sd})$ in the former.

The intrinsic drive current $(I_{\rm oni})$ is related to the effective carrier velocity $\nu_{\rm eff}(x_0)$ in the channel by [8]

$$I_{\rm oni}/W = \nu_{\rm eff}(x_0)^* C^*_{\rm gi}(V_g - V_t) = \nu_{\rm eff}(x_0)^* n_s \qquad (2)$$

where x_0 corresponds to the conduction band peak at the source side of the channel, V_t is the transistor threshold voltage using the standard linear peak transconductance extraction method, and n_s is channel charge density at the source end. Because full $C_g - V_g$ curves are not available for III–V QWFETs, n_s is approximated using $(C^*_{\rm gi}(V_g - V_t)/{\rm q})$, where $C_{\rm gi}$ is the channel capacitance at Vds = 0.05 V. The $\nu_{\rm eff}$ determined from the intrinsic transconductance method as defined in (1) can be used as an approximation of $\nu_{\rm eff}(x_0)$ with the understanding that $\nu_{\rm eff}(x_0)$ may be overestimated by 15%–30% [8].

III. Devices

The InSb and $In_{0.7}Ga_{0.3}As$ quantum-well transistors were fabricated using standard processing techniques [1], [3]. For the InSb QWFETs, the InSb quantum well is 20 nm thick with a room-temperature Hall mobility of 20 000–30 000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at a sheet carrier density of 1.3×10^{12} cm^{-2}. The physical gate insulator thickness $(T_{\rm ins})$, which is the wide band-gap semiconductor thickness between the Schottky gate and the quantum well of the device, is ∼9 nm. For the two $In_{0.7}Ga_{0.3}As$ QWFET cases, the physical gate insulator thickness is ∼6 and ∼8 nm. The quantum well is 13 nm thick with a room-temperature Hall mobility of 10 000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at a sheet carrier density of 3.5×10^{12} cm^{-2}. The physical gate length of the InSb and $In_{0.7}Ga_{0.3}As$ QWFETs ranges from 60 to 200 nm. The strained Si nMOSFET devices have thin gate oxide and physical gate lengths ranging from 30 to 60 nm.

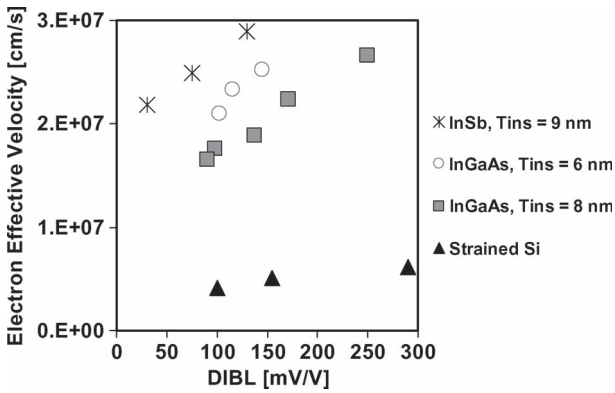

Fig. 2. Effective electron velocity versus DIBL for $In_{0.7}Ga_{0.3}As$ with $T_{\rm ins}$ of 6 and 8 nm, InSb with $T_{\rm ins}$ of 9 nm and strained Si nMOSFET at $V_{\rm ds} = 0.5$ V and a gate overdrive of $(V_g - V_t) = 0.3$ V. At a constant DIBL of 150 mV/V, $In_{0.7}Ga_{0.3}As$ (8 nm), $In_{0.7}Ga_{0.3}As$ (6 nm), and InSb (9 nm) show 3.7×, 4.1×, and 5× increase in $\nu_{\rm eff}$ over strained Si, respectively.

IV. Results and Discussion

The effective carrier velocities of the various devices are shown versus DIBL in Fig. 2. At a constant DIBL of ∼150 mV/V, the 8-nm $T_{\rm ins}$ $In_{0.7}Ga_{0.3}As$, the 6-nm $T_{\rm ins}$ $In_{0.7}Ga_{0.3}As$, and the 9-nm $T_{\rm ins}$ InSb QWFETs show 3.7×, 4.1×, and 5× increase in $\nu_{\rm eff}$, respectively, over that of the strained Si nMOSFET. This increase in $\nu_{\rm eff}$ occurs despite a reduction in charge density (n_s) in the $In_{0.7}Ga_{0.3}As$ and InSb QWFETs compared to the Si nMOSFET. As the gate insulator thickness is scaled for $In_{0.7}Ga_{0.3}As$ QWFETs from 8 to 6 nm, the effective velocity increases by 20% at a constant DIBL and at a constant $I_{\rm off}$ due to the combination of gate length and insulator thickness scaling. Because both $\nu_{\rm eff}$ and charge density increase in the QWFET devices with insulator scaling, significant increase in device performance is expected with continued $T_{\rm ins}$ reduction.

In Fig. 3(a), the $\nu^*_{\rm eff} n_s$ product, which is proportional to intrinsic $I_{\rm oni}$, is shown versus gate overdrive $(V_g - V_t)$ of (1) the 6-nm $T_{\rm ins}$$In_{0.7}Ga_{0.3}As$ QWFET and (2) the strained Si nMOSFET at matched $I_{\rm off}$ and DIBL. For low-voltage operation targeted at $V_{\rm ds} = V_{\rm gs} = 0.5$ V and an ideal V_t of ∼0.2 V

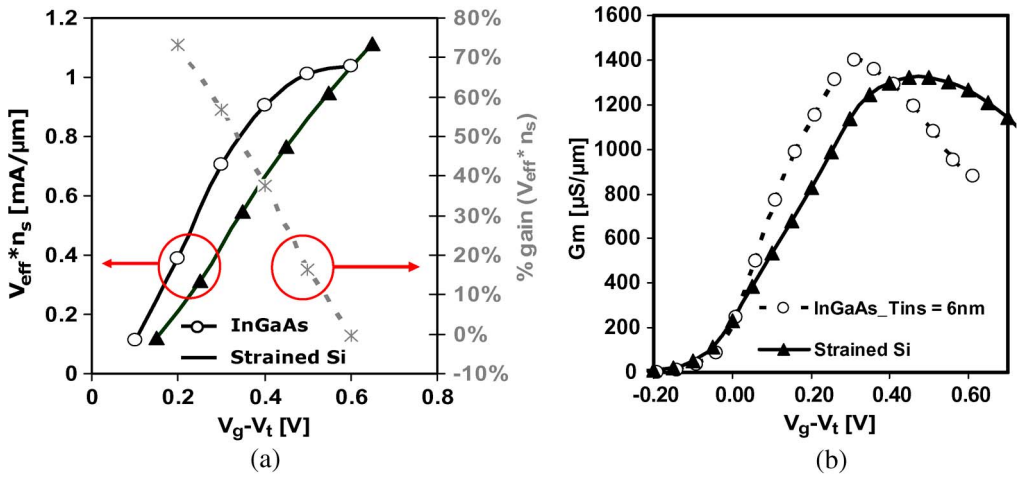

Fig. 3. (a) Primary y-axis depicts the $v_{\rm eff}^{*}n_s$ product and the (right) secondary y-axis shows the percentage gain in $I_{\rm on}$ of the $In_{0.7}Ga_{0.3}As$ QWFET ($T_{\rm ins} = 6$ nm) over that of the strained Si nMOSFET versus gate overdrive ($V_g - V_t$). (b) Measured transconductance of $In_{0.7}Ga_{0.3}As$ QWFET and strained Si nMOSFET versus gate overdrive. In both Fig. 3(a) and (b), DIBL is ~150 mV/V, $I_{\rm off}$ is equivalent, and $V_{\rm ds} = 0.5$ V for both material systems.

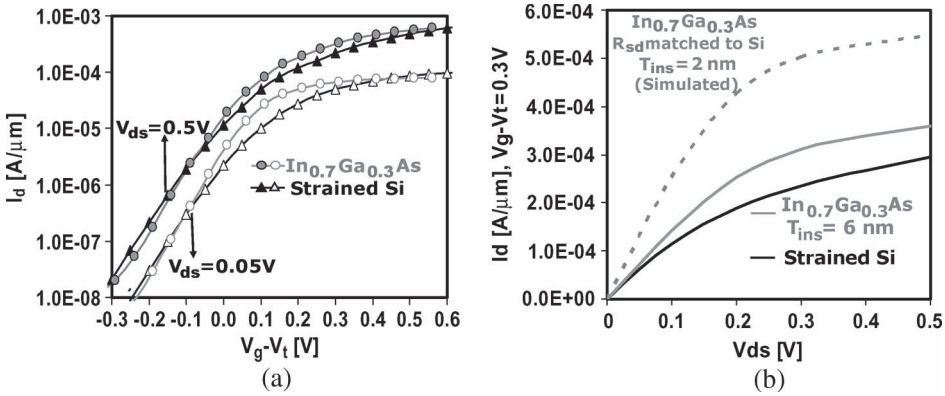

Fig. 4. (a) $I_d - (V_g - V_t)$ for 80-nm L_g $In_{0.7}Ga_{0.3}As$ ($T_{\rm ins} = 6$ nm) quantum-well transistor and 40-nm L_g strained Si nMOSFET at matched $I_{\rm off}$ with $V_{\rm ds} = 0.5$ V and 0.05 V. DIBL for both devices is matched at 150 mV/V (±5 mV/V) and subthreshold slope is matched at 90 mV/decade (±3 mV/decade). (b) $I_d - V_{\rm ds}$ for 80-nm L_g $In_{0.7}Ga_{0.3}As$ ($T_{\rm ins} = 6$ nm) QWFET and 40-nm L_g strained Si nMOSFET with matched $I_{\rm off}$ and DIBL of ~150 mV/V. The dotted line represents simulated $In_{0.7}Ga_{0.3}As$ data with external resistance ($R_{\rm sd}$) matched to that of the strained Si and gate-to-channel separation ($T_{\rm ins}$) scaled to 2 nm.

for logic applications, the resulting gate overdrive is ~0.3 V. At Vg − Vt = 0.3 V, the $In_{0.7}Ga_{0.3}As$ QWFET shows a ~55% gain in $I_{\rm oni}$ over the strained Si nMOSFET [Fig. 3(a)]. This demonstrates that despite lower n_s, III–V QWFETs can exhibit higher $I_{\rm on}$ than strained Si due to higher $\nu_{\rm eff}$. In addition, Fig. 3(b) shows that g_m of the $In_{0.7}Ga_{0.3}As$ QWFET peaks at a lower $(V_g - V_t)$ value compared to that of the strained Si nMOSFET. This indicates that III–V QWFETs have a performance advantage over strained Si at low-voltage operation.

Finally, the room temperature transfer and output characteristics obtained for the 80-nm physical gate length $In_{0.7}Ga_{0.3}As$ QWFET ($T_{\rm ins} = 6$ nm) and the 40-nm physical gate length strained Si nMOSFET are shown in Fig. 4(a) and (b), respectively. Because the Si device has a V_t of 0.36 V and the $In_{0.7}Ga_{0.3}As$ has a V_t of 0.1 V, the transfer characteristics are shown versus $V_g - V_t$. V_t is calculated in all cases using the standard linear peak transconductance extraction method. In Fig. 4(a) and (b), DIBL and subthreshold slope of the $In_{0.7}Ga_{0.3}As$ and Si devices are matched at ~150 mV/V and ~90 mV/dec, respectively. At $V_{\rm ds} = 0.5$ V and $V_g - V_t =$ 0.3 V, $I_{\rm on}$ for the $In_{0.7}Ga_{0.3}As$ and Si devices is 0.36 and 0.29 mA/μm, respectively. This occurs despite the fact that with current processing conditions, $In_{0.7}Ga_{0.3}As$ devices exhibit a thicker gate-to-channel separation and ~2× higher external resistance ($R_{\rm sd}$) than the Si nMOSFETs. To further examine performance benefits, simulation based on a coupled 2-D Poisson and a single effective mass-based nonequilibrium Green's function method [9], [10] was first calibrated to the $In_{0.7}Ga_{0.3}As$ QWFET data. Next, with $R_{\rm sd}$ matched to strained Si and $T_{\rm ins}$ scaled down to 2 nm, the simulation projects that the $In_{0.7}Ga_{0.3}As$ QWFET can exhibit > 80% improvement in $I_{\rm on}$ over the Si device at equivalent $I_{\rm off}$ as shown in Fig. 4(a).

V. Conclusion

The effective carrier velocities for InSb and $In_{0.7}Ga_{0.3}As$ QWFETs, and state-of-the-art strained Si nMOSFET devices are extracted using an intrinsic transconductance method. It is observed that despite lower charge density, the effective carrier velocities of the high-mobility $In_{0.7}Ga_{0.3}As$ and InSb QWFETs exhibit a 4.1× and 5× increase, respectively, over that of strained Si nMOSFETs at a constant DIBL. The increase in $\nu_{\rm eff}$

in the $In_{0.7}Ga_{0.3}As$ QWFET translates to 20% improvement in I_{on} over the strained Si nMOSFET at matched DIBL, I_{off}, $(V_g - V_t) = 0.3$ V, and at $V_{ds} = 0.5$ V, despite a thick T_{ins} and $\sim 2\times$ higher R_{sd}. At R_{sd} matched to strained Si and T_{ins} scaled to 2 nm, it is possible for the $In_{0.7}Ga_{0.3}As$ QWFET to exhibit $> 80\%$ I_{on} increase over the strained Si nMOSFET, making the III–V QWFET a promising candidate for future high-speed and ultralow-power logic applications.

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