*Solid State Phenomena Vols. 145-146 (2009) pp 165-167*
*online at http://www.scientific.net*


# Surface preparation and passivation of III-V substrates for future ultra-high speed, low power logic applications

Willy Rachmady [1], James Blackwell, Gilbert Dewey, Mantu Hudait, Marko Radosavljevic, Robert Turkot Jr., and Robert Chau

Components Research, Technology and Manufacturing Group, Intel Corporation
Mail Stop RA3-252, 5200 N.E. Elam Young Parkway, Hillsboro, Oregon 97124-6497 USA

[1]willy.rachmady@intel.com

**Keywords:** III-V, surface passivation, dielectric integration.

## Introduction

III-V compound semiconductors have been recognized among the potential options for continuing transistor power-performance scaling owing to their ultra high charge carrier mobility. In order to realize their potential in high performance and lower-power digital logic applications, there must be strong gate control and a high Ion-Ioff ratio, achieved by integrating a stable, ultra thin high-K dielectric between the semiconductor and the gate [1, 2]. Unlike Si, which has long benefited from its very stable native oxide, III-V materials suffer from their poor native oxides that cause charge traps and Fermi level pinning at the semiconductor-oxide interface. Attempts to deposit high-K directly on III-V often produce MIS structures with fast surface state and CV instability [3].

In this presentation we will focus on III-V surface preparation for ex-situ high-K dielectric deposition because of its manufacturability and compatibility with the current state of art of device fabrication. We will review fundamental requirements for enabling high-K dielectric integration with III-V materials, analyze the challenges in preparing and passivating III-V surfaces, and discuss recent progress in this area.

## Gate Dielectric for Logic Applications

Lack of gate dielectrics on III-V transistors has limited the device placement in logic applications. As an example, although the InSb transistor shows much improved n-channel intrinsic speed (CV/I) as compared to standard Si devices, it suffers from a low Ion-Ioff ratio caused by high gate leakage, shown in Figures 1 and 2. Beside the fact InSb is a narrow-bandgap semiconductor, this high gate leakage is primarily due to the low barrier height at the Schottky metal-semiconductor junction.

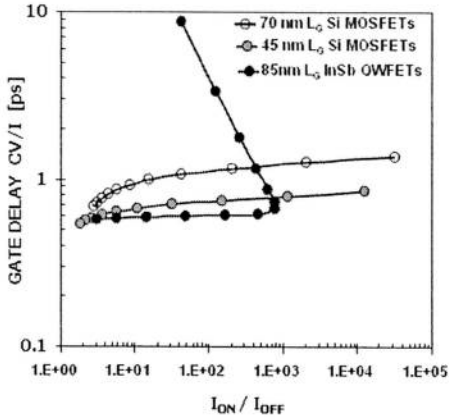


Figure 1. Gate delay (intrinsic device speed) CV/I versus on-to-off state current ration $I_{ON}/I_{OFF}$ of Si NMOS transistors with physical gate length $L_G$ = 70 and 45nm, and an InSb n-type quantum-well FET with LG = 85nm [3].

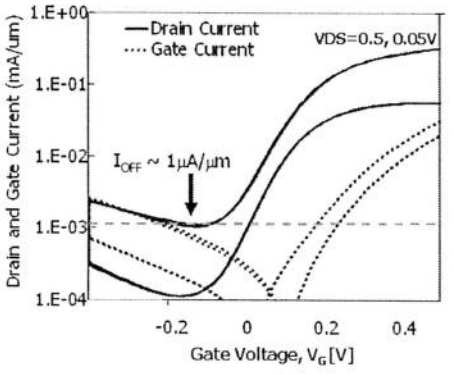


Figure 2. Drain current $I_{DS}$ and gate leakage current $I_G$ versus gate voltage $V_{GS}$ of an InSb n-type quantum-well FET with LG = 85nm. $I_G$ is the Schottky gate leakage due to the absence of gate dielectric [3].

It is evident that a high-K gate dielectric is required in order to solve the aforementioned problem. The dielectric film must be sufficiently thin so as to maintain short-channel performance and extend device scalability. With the continued scaling towards Tox less than 20A, Fermi level pinning and oxide growth at the interface can be the showstoppers and therefore must be appropriately addressed in order to achieve a gate stack with electrostatic characteristics acceptable for logic CMOS applications.

**Surface Preparation and Passivation**

The challenge of integrating high-K dielectric begins at the preparation of the surface. As native oxides on III-V compound semiconductors are intrinsically detrimental to the electrical properties of the high-K/III-V interface, they must be removed before any dielectric is deposited or grown. Both thermal desorption and chemical etching have been proposed but chemical etching using halide acids, such as HF and HCl, have been shown consistently to efficiently remove III-V oxides without significantly restructuring the underlying surface. HCl is more importantly found to protect the surface from re-oxidation as shown in Figure 3.

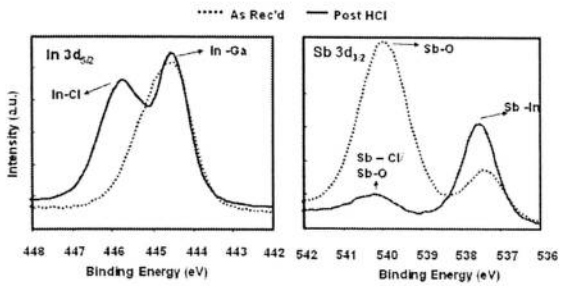


Figure 3. XPS spectra of In $3d_{5/2}$ and Sb $3d_{3/2}$ for InSb (100) wafer as-received and post HCl clean. After a brief exposure to ambient air, very little of re-oxidation of In and Sb is observed.

As atomic layer deposition (ALD) has been identified as a practical method to deposit high-K dielectric film, it also becomes very important for III-V surfaces to be properly terminated with functional groups reactive to the ALD precursors. For example, hydroxyl and chlorine functional groups are some of the surface termination species that are stable and can initiate ALD reactions. In the case of an HCl clean on InSb, HCl has a threefold purpose: remove native oxides, protect the surface from oxidation, and activate the surface for ALD reaction.

Achieving all of the above conditions is necessary to obtain an abrupt, native-oxide-free interface between $Al_2O_3$ and InSb but it is insufficient to deliver an electrically good interface. Although a $Al_2O_3$/InSb MOSCAP with minimal interfacial oxide and with electrical oxide thickness equivalent to Al2O3/Si stack is achieved, the C-V characteristics of the gate stack still exhibit Fermi level pinning at the interface. Changing the metal electrode work-function from Al to TiN does not show the expected 600 mV shift of the flat-band voltage, as apparent in Figure 4.

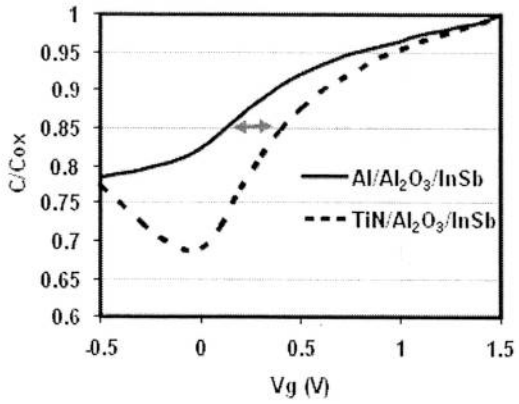


Figure 4. C-V curves of $Al/Al_2O_3/InSb$ and $TiN/Al_2O_3/InSb$ MOS capacitors. A shift of ~ 250mV of the flat-band voltage is seen between Al and TiN metal electrodes.

It has been recognized that bare III-V surfaces obtained after an oxide removal step inherently contain sites responsible for mid-gap states and charge traps [4]. Passivation of these sites is obviously necessary so as to unpin the Fermi level at the interface, and it is one of the grand challenges to be overcome in order to enable III-V logic devices.

The chemical and electronic structures of these sites are far from understood, but chemical passivation shows promise in improving the interface. Sulfur chemisorption has been the most dominant approach and most widely studied. Recently, sulfur passivation applied in the fabrication of $HfO_2$/InGaAs stack has been demonstrated to reduce interface state densities down to 7-9 x $10^{11}/cm^2$ - eV with obvious improvement

in frequency dispersion [5]. In addition, chemisorbed sulfur has also been shown to inhibit reoxidation [6], therefore, providing a convenient approach in preparing III-V for *ex-situ* high-K dielectric deposition.

Another approach that has held promise is incorporating a thin layer of amorphous silicon between the semiconductor and the dielectric. III-V MOSCAP structures with a low hysteresis and interfacial state densities have been demonstrated with this technique [7]. The approach however will need to be optimized to deliver a gate stack with equivalent oxide thickness (EOT) below 20A, in order to be practical for $L_G$ scaling and short-channel effect (SCE) control.

**Summary**

The inherent complexity of the dielectric/III-V interface is a major technical challenge for enabling high-K dielectric integration on III-V materials. Although interface quality of high-K/III-V systems reported to date are still far from those of high-K/Si systems in the state-of-the-art CMOS devices, renewed interests in the III-V surface preparation and passivation have resulted in significant progress towards realizing III-V potentials in continuing CMOS power-performance scaling beyond Si technology.

## References:

[1] S. Datta and R. Chau, Proceedings of 2005 International Conference on Indium Phosphide and Related Materials, Glasgow, Scotland, p. 7-8 (2005).

[2] R. Chau, J.Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, Microelectronic Engineering, **80**, p. 1-6, (2005).

[3] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. Wallis, P. Wilding, and R. Chau, IEDM Technical Digest, p. 763-766 ( 2005).

[4] H. Hasegawa, and T. Sawada, IEEE Transactions on Electron Devices, 27, p.1055-1061 (1980).

[5] N.Goel., P. Majhi, C.O. Chui, W. Tsai,. D. Choi, and J.S. Harris, Applied Physics Letters, **89**, 163517 (2006).

[6] D.Y. Petrovykh, M.J. Yang, L.J. Whitman, Surface Science, **523**, p.231–240 (2003).

[7] InJo Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J. Yum, S. Koveshnikov, W. Tsai, V. Tokranov, M. Yakimov, S. Oktyabrsky, and J.C. Lee, J. Vac. Sci. Technol. B 25, p.1491- 1492 (2007).