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Study of the inversion behaviors of $Al_2O_3/In_xGa_{1-x}As$ metal–oxide–semiconductor capacitors with different In contents

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ABSTRACT

$In_xGa_{1-x}As$ III–V compound semiconductor metal–oxide–semiconductor field-effect transistors have become a popular topic recently due to the higher drift velocity, and lower effective mass of the $In_xGa_{1-x}As$ materials. The impact of In content on the accumulation and inversion behaviors of the $Al_2O_3/In_xGa_{1-x}As$ capacitors is investigated in this study. For the various $In_xGa_{1-x}As$ materials studied, the Al_2O_3/InAs MOS system showed the strongest inversion phenomena due to the shorter response time of minority carrier of InAs compared to other $In_xGa_{1-x}As$ materials. Also, very low gate leakage current in the 10^{-8} A/cm^2 range was observed for these capacitors. These results demonstrate that Al_2O_3/InAs MOS system with strong inversion phenomena and low leakage gate current is potential candidate for future high-performance low power logic MOSFET applications.

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1. Introduction

Future scaling of complimentary metal–oxide–semiconductor (CMOS) in accordance with Moore's law will require various non-traditional solutions such as high-κ dielectrics, metal gates, and high-mobility channels. Interest has recently been focused on III–V based material systems as likely n- and p-channel ultimate scaling solutions because of their superior transport properties. $In_xGa_{1-x}As$ materials have great potential to meet the high-performance requirements due to their high-mobility in comparison with silicon. The study of p-MOS behavior for $In_xGa_{1-x}As$ is of interest due to the possibility of the integration of p- and n-channel $In_xGa_{1-x}As$ CMOS device for logic applications [1]. The inversion behavior of the $In_xGa_{1-x}As$ p-MOS has not been extensive studied yet. The understanding of the inversion behavior of the $In_xGa_{1-x}As$ p-MOS capacitor will be helpful in the future research for III–V/Si integration for low power logic applications. However, the major problem using of III–V compound semiconductor devices for low power logic application is the lack of high quality high-κ dielectric with low interface trap density. Atomic layer deposition (ALD) technique is a widely used for high-κ material deposition for Si CMOS technology. Al_2O_3 gate dielectric has high bandgap energy (~9 eV), high breakdown field (5 ~ 10 MV/cm), high dielectric constant (8.6–10), and high thermal stability (up to at least 1000 °C), also it remains amorphous under typical process conditions [2–4]. Even though many groups have reported $In_xGa_{1-x}As$ MOS capacitors with ALD Al_2O_3 as the gate dielectrics for n-InGaAs MOSFET [5,6], there is no report studying the variation of the $In_xGa_{1-x}As$ MOS capacitor characteristics with In content up to 100% (InAs) in the literature. In this study, we use Al_2O_3 as the gate dielectric for the $In_xGa_{1-x}As$ MOS capacitors. The In content varies from $In_{0.53}Ga_{0.47}As$ (53%) up to InAs (100%). The gate current density versus gate voltage (J_G–V_G) and capacitance versus voltage (C–V) characteristics of the $In_xGa_{1-x}As$ MOS capacitors with these different In contents were investigated. The formation mechanisms

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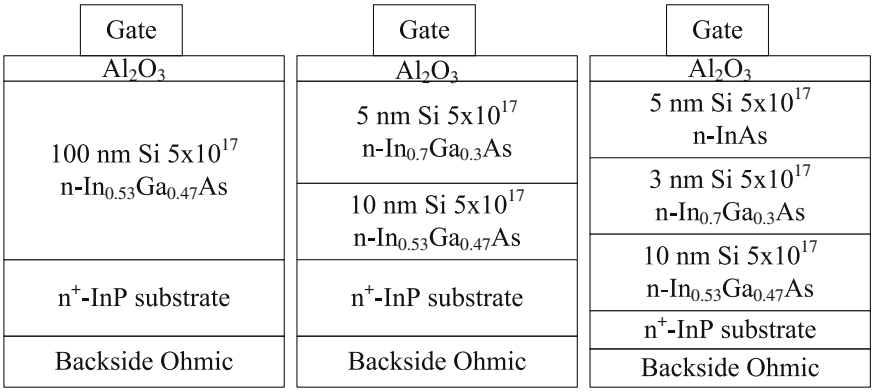

Fig. 1. Epitaxial structures of the $In_xGa_{1-x}As$ MOS capacitors with different In contents.

of inversion regions of these $In_xGa_{1-x}As$ MOS capacitors are studied. The understanding of the characteristics of these MOS capacitors is very important for the development of the III–V based MOSFETs.

2. Experimental

The epitaxial structures of the $In_xGa_{1-x}As$ MOS capacitors with different In contents of 0.53, 0.7, and 1.0 in this study are as shown in Fig. 1. These structures were grown on a 3-inch n^+-InP substrate by MBE method. The n^+-InP substrates were used for easy Ohmic formation on the backside. For all the $In_xGa_{1-x}As$ layers in these structures, the Si doping concentration was $5 \times 10^{17}/cm^3$. For higher In content structures, the structures were graded from $In_{0.53}Ga_{0.47}As$ to $In_{0.7}Ga_{0.3}As$, and then to InAs to adjust the lattice mismatches between the $In_xGa_{1-x}As$ epitaxial layers with different In contents. Al_2O_3 films were deposited on these epitaxial structures using ALD method as high-κ dielectric for the MOS capacitor study. After HCl (10%) solution etch for 1 min, $(NH_4)_2S_x$ treatment at 60 °C for 30 min [7,8] was used to passivate the surface and reduce $In_xGa_{1-x}As$ surface native oxides [9]. The sulfur treatment of MOS capacitors can reduce the leakage current and improve the *C–V* characteristics of the MOS capacitor [10]. After $(NH_4)_2S_x$ treatment, the growth of ALD Al_2O_3 was carried out at 300 °C, using Trimethylaluminum (TMA) and H_2O as the precursors, and purged with N_2 gas. Al_2O_3 layers of 16 nm were deposited on these epitaxial layers for MOS capacitor formation. Postdeposition annealing for Al_2O_3 layers was performed at 500 °C for 60 s in the forming gas ambient. Then, Ti/Pt/Au metal was deposited as gate metal by lift-off process. The backside Ohmic contacts were formed by Au/Ge/Ni/Au evaporation followed by rapid thermal annealing at 450 °C for 30 s. The schematics of the cross sections of the MOS capacitors are as shown in Fig. 1.

3. Results and discussion

To study the formation mechanisms of the accumulation and inversion regions of the $In_xGa_{1-x}As$ MOS capacitors, $In_xGa_{1-x}As$ layers with different In contents of 0.53, 0.7, and 1.0 were grown on the n^+-InP substrate with structures as shown in Fig. 1, and the capacitance–voltage (*C–V*) characteristics as a function of frequency were measured for these $In_xGa_{1-x}As$ MOS capacitors. For these measurements, the dc voltage was swept from negative to positive voltages (−4 to 4 V) on these capacitors. The dc voltage was swept slowly at a fixed step of 0.05 V to allow the inversion charges to respond to the ac probe frequency to obtain low-frequency curve. However, if the dc voltage was swept slowly to allow the inversion charge to form but the ac probe frequency was too high for the inversion charges to respond, then the high-frequency curve obtained will be of very low capacitance even at high negative gate bias [11]. Fig. 2 shows the *C–V* characteristics of the 16-nm Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor. The capacitor demonstrates strong inversion at 1 kHz frequency. However, as the capacitor was measured at 500 kHz and 1 MHz, deep-depletion curve was observed. The deep-depletion phenomena resulted from the fact that the inversion charges can not respond fast enough to

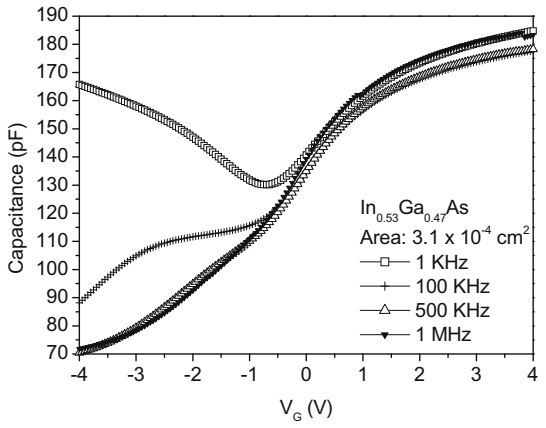

Fig. 2. *C–V* characteristics for $In_{0.53}Ga_{0.47}As/n^+$-InP MOS capacitors under various frequencies from 1 kHz to 1 MHz.

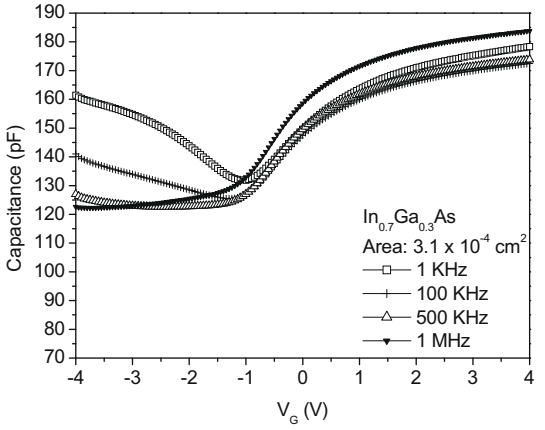

Fig. 3. *C–V* characteristics for $In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As/n^+$-InP MOS capacitors under various frequencies from 1 kHz to 1 MHz.

the applied ac signal at high-frequency due to higher lifetime of the charges in n-$In_{0.53}Ga_{0.47}As$. The Al_2O_3/n-$In_{0.7}Ga_{0.3}As$ MOS capacitor in this study also showed evidences of electron accumulation for positive biases and hole inversion for negative biases, however, the material does not show tendency of deep-depletion when measured at higher frequencies as shown in Fig. 3. Compared to the *C–V* data of the Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor in Fig. 2, hole inversion was observed even when measured at 500 kHz, which was due to the shorter lifetime of the charges in n-$In_{0.7}Ga_{0.3}As$.

Fig. 4 shows the *C–V* curves of the 16-nm Al_2O_3/n-InAs MOS capacitor at various applied ac signal frequencies for the InAs

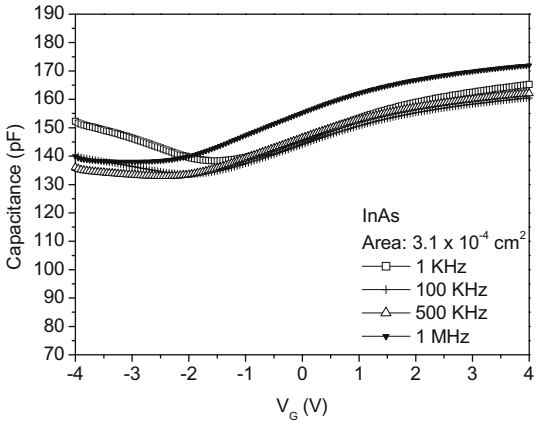

Fig. 4. *C–V* characteristics for InAs/$In_{0.7}Ga_{0.3}As$/$In_{0.53}Ga_{0.47}As$/n^+-InP MOS capacitors under various frequencies from 1 kHz to 1 MHz.

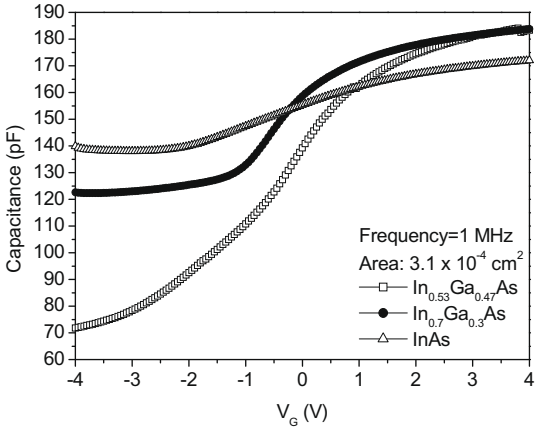

Fig. 5. Comparisons of *C–V* characteristics at 1 MHz for $In_xGa_{1-x}As$ MOS capacitors.

capacitor, strong inversion was observed even when measured at 1 MHz. The inversion capacitance ($V_G = -4$ V) to accumulation capacitance ratio (C_{inv}/C_{acc}) of 87.5% at 100 kHz and of 81.27% at 1 MHz were observed. The presence of the strong inversion layer is evident from these data. The higher C_{inv}/C_{acc} ratio for the n-InAs capacitor is mainly due to the short lifetime, the higher mobility of the charges in the inversion layer and the high thermal generation rate for the InAs material ($E_g \sim 0.36$ eV) [12]. The *C–V* curves of the $In_xGa_{1-x}As$ MOS capacitors with different In contents of 0.53, 0.7, and 1.0 at higher frequency operations are shown in Fig. 5, the inversion charges were able to gradually respond to the high-frequency ac signals with the increase of In content in the MOS capacitors, and the strong inversion phenomena can be observed even at 1 MHz for the InAs MOS capacitors. The reason that strong inversion charges in the InAs channel can respond at high-frequency operation was mainly due to its higher drift velocity and the shorter response time of the minority carriers in the InAs layer. The response time of the minority carrier can be comprehended by the relationship $\tau_R \propto \tau_T/n_i$ [13], where τ_R is the response time of minority carrier, τ_T is the lifetime of minority carrier [14], and n_i is the intrinsic carrier concentration. At room temperature, n_i in InAs is in the range of 1×10^{15} cm^{-3} which is roughly three orders of magnitude higher than n_i in $In_{0.53}Ga_{0.47}As$ which is of $\sim 10^{12}$ cm^{-3} due to the lower bandgap of InAs material. Compared to τ_R of $In_{0.53}Ga_{0.47}As$, τ_R of InAs is extracted to be shorter. Because of the shorter response time of minority carrier in InAs, a strong inversion layer is formed and can response to the high-frequency external ac signals [15]. On the other hand, for the operation of MOSFETs, the inversion voltage V_i and the maximum depletion width d_p can be expressed as the following equations [16]:

$$V_i = \frac{2kT}{e}\ln\left(\frac{N_a}{n_i}\right) \quad \text{and} \quad d_p = \left\{\frac{2\varepsilon_s V_i}{eN_a}\right\}^{1/2}$$

where n_i is the intrinsic carrier concentration, N_a is the doping concentration, and ε_s is the substrate dielectric constant. From the two equations above, small V_i and d_p in InAs can be obtained because of the high intrinsic carrier concentration. Therefore, the *C–V* curve for InAs at 1 MHz exhibits strong inversion due to the high intrinsic carrier concentration for narrow band gap InAs material [12].

These results are in agreement with the data shown in Table 1, i.e., as the In content increases in the $In_xGa_{1-x}As$ film, the C_{inv}/C_{acc} ratio at 1 MHz becomes larger due to the shorter response time of the minority carriers [17]. The stronger inversion efficiency with higher C_{inv}/C_{acc} ratio was observed for InAs capacitor at 100 kHz and 1 MHz. Table 1 also exhibits that inversion layer capacitance $\Delta C_{inv,\ 1K-1M}$ ($C_{inv,\ 1K}$–$C_{inv,\ 1M}$) which is defined as the difference in inversion capacitance between the frequency of 1 kHz and 1 MHz for $In_xGa_{1-x}As$ layers. Overall, InAs has the smallest inversion capacitance difference of 12.41 pF as compared to that of 93.87 pF for $In_{0.53}Ga_{0.47}As$ and 38.85 pF for $In_{0.7}Ga_{0.3}As$. Due to the short-

Table 1
Comparisons of *C–V* characteristics of $In_xGa_{1-x}As$ MOS capacitors with increasing In content.

C–V characteristics	$In_{0.53}Ga_{0.47}As$	$In_{0.7}Ga_{0.3}As$	InAs
Accumulation capacitance (pF) @ 4 V & 100 kHz	177.75	172.49	160.51
Inversion capacitance (pF) @ −4 V & 100 kHz	88.16	141.03	140.50
C_{inv}/C_{acc} (%) & 100 kHz	49.59	81.76	87.53
Accumulation capacitance (pF) @ 4 V & 500 kHz	178.28	173.80	162.11
Inversion capacitance (pF) @ −4 V & 500 kHz	70.44	126.98	136.06
C_{inv}/C_{acc} (%) & 500 kHz	39.51	73.06	83.93
Accumulation capacitance (pF) @ 4 V & 1 MHz	183.36	183.81	172.01
Inversion capacitance (pF) @ −4 V & 1 MHz	71.8	122.61	139.8
C_{inv}/C_{acc} (%) & 1 MHz	39.16	66.70	81.27
$\Delta C_{inv,\ 1K-1M}$ ($C_{inv,\ 1K}$–$C_{inv,\ 1M}$) (pF)	93.87	38.85	12.41
D_{it} ($cm^{-2}eV^{-1}$) @ 1 MHz	7×10^{12}	4×10^{12}	4×10^{12}
Dielectric constant & 1 MHz	10.55	10.58	9.89

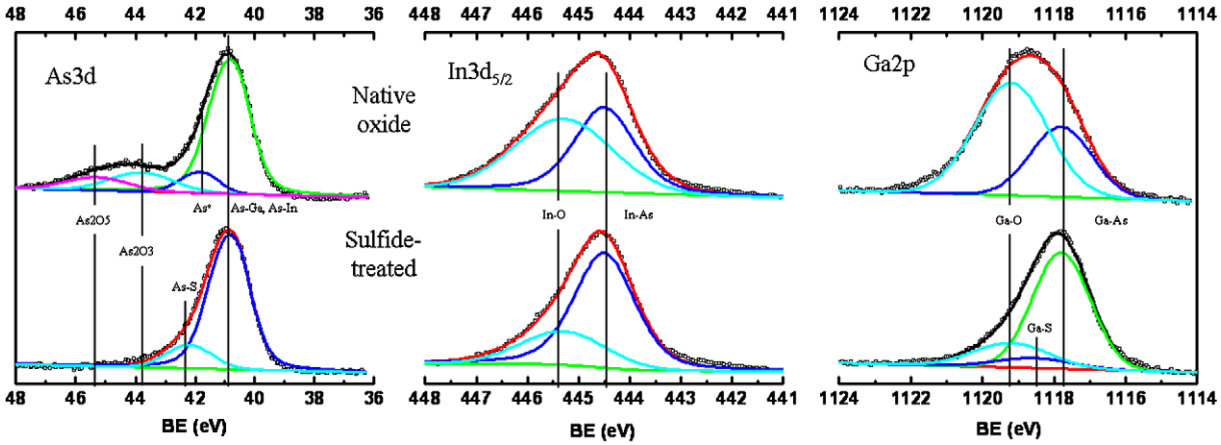

Fig. 6. XPS spectra of $In_{0.53}Ga_{0.47}As$ before and after sulfide treatment.

er minority response time of InAs, a strong inversion in InAs channel was formed and can respond to a high-frequency external ac signal at the gate.

As summarized in Table 1 and explained earlier, InAs has the highest C_{inv}/C_{acc} ratio and smallest inversion capacitance difference $\Delta C_{inv,\ 1K-1M}$, this can be attributed to the strong inversion of InAs capacitor due to higher drift velocity and shorter minority response time of InAs. These data are in accordance with the inversion phenomena observed for the ALD 7.8-nm HfO_2/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor in [15] and the ALD 30-nm Al_2O_3/p-InAs MOS capacitor in [12].

The midgap interface trap densities (D_{it}) of these $In_xGa_{1-x}As$ capacitors were extracted from the combination of single-frequency C–V and G–V characteristics using Hill's method [18,19]. The interface trap density D_{it} is expressed as the equation below:

$$D_{it} = \frac{(2/qA)(G_{max}/\omega)}{[(G_{max}/\omega C_{ox})^2 + (1 - C_m/C_{ox})^2]}$$

where G_{max} is the maximum conductance in the G–V plot with its corresponding capacitance (C_m), C_{ox} is the oxide capacitance, ω is the angular frequency, and A is the gate area of the capacitor. The interface trap density of these $In_xGa_{1-x}As$ capacitors was calculated

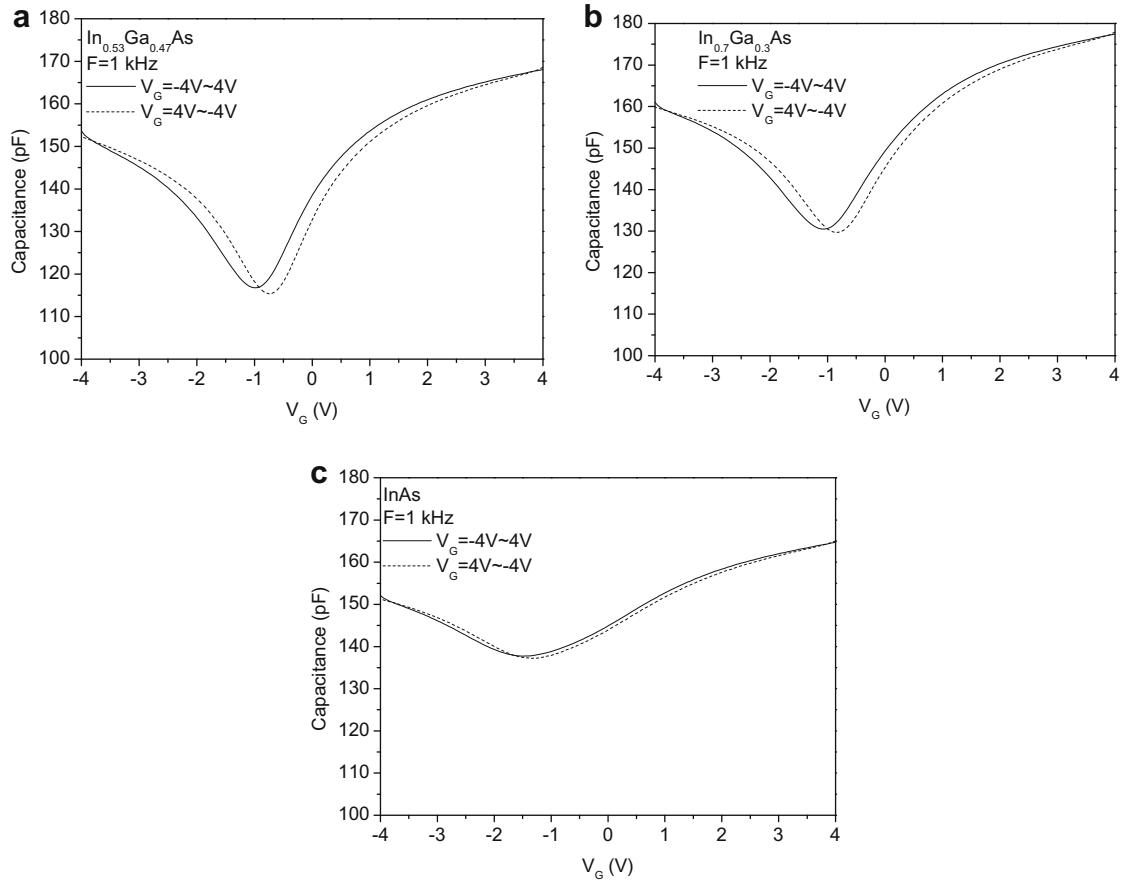

Fig. 7. (a) Bidirectional C–V sweeps of $In_{0.53}Ga_{0.47}As$ capacitor. (b) Bidirectional C–V sweeps of $In_{0.7}Ga_{0.3}$ As capacitor. (c) Bidirectional C–V sweeps of InAs capacitor.

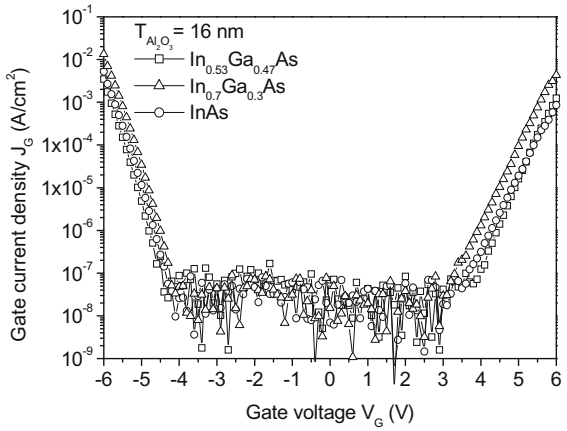

Fig. 8. J_G–V_G characteristics of $In_xGa_{1-x}As$ MOS capacitors with different In contents of 0.53, 0.7, and 1.0.

to be in the 10^{12} cm^{-2}eV^{-1} range as summarized in Table 1. It could be caused by the thermal stable interfacial native oxides (Ga_2O_3/In_2O_3) at the Al_2O_3/$In_xGa_{1-x}As$ interface. From the thermodynamic consideration, the Gibbs free energy of Ga_2O_3 and In_2O_3 are −238.6 kcal/mol and −198.6 kcal/mol respectively, which are lower than the Gibbs free energy of As_2O_3 which is −137.7 kcal/mol [20]. It has been demonstrated that there was no arsenic oxides on the interface, meanwhile residual In_2O_3 and Ga_2O_3 were detected at the ALD Al_2O_3/$In_{0.15}Ga_{0.85}As$ interface [21]. Thus, In_2O_3 and Ga_2O_3 were difficult to remove due to their higher thermal stability. Fig. 6 shows the XPS spectra of $In_{0.53}Ga_{0.47}As$ before and after sulfide treatment. It apparently indicates that arsenic oxides were mostly removed, but In_2O_3 and Ga_2O_3 remained even the $In_{0.53}Ga_{0.47}As$ surface was sulfide-treated.

Furthermore, the Al_2O_3 quality after the postdeposition annealing was investigated by using the bidirectional C–V sweeps for the $In_xGa_{1-x}As$ capacitors as shown in Fig. 7. Hysteresis occurrence depends on the quality and the densification effect of the high-κ dielectric [19]. It can be seen that hysteresis voltage in the C–V curves for the $In_xGa_{1-x}As$ materials were very small, which implies very good Al_2O_3 film quality.

One of the key parameters for the MOS devices is the leakage current through the high-κ dielectric for low power logic application. The high tunneling gate leakage current would increase the power consumption of the devices. As can be seen from Fig. 8, the gate current density (J_G) of $In_{0.53}Ga_{0.47}As$, $In_{0.7}Ga_{0.3}As$, and InAs MOS capacitors are in 10^{-8} A/cm^2 range at gate voltage (V_G) of 3 V. In addition, the tunneling current at biases above 5 V has a good consistency with the Fowler–Nordheim tunneling mechanism, indicating a low trap density inside Al_2O_3 dielectric. Overall, very low leakage current density around 10^{-8} A/cm^2 for $In_xGa_{1-x}As$ MOS capacitors can be achieved using Al_2O_3 as the gate dielectric which is important for high-performance low power logic applications.

4. Conclusion

We have studied the C–V and J_G–V_G characteristics of ALD Al_2O_3/$In_xGa_{1-x}As$/n^+-InP heterostructure with different In contents of 0.53, 0.7, and 1.0. From C–V measurement results, the inversion efficiency of the MOS capacitor increases with In content. A strong inversion for Al_2O_3/InAs capacitor was observed even at 1 MHz ac signal due to the higher drift velocity and the shorter minority response time of InAs compared to $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$. The ALD Al_2O_3/$In_xGa_{1-x}As$ capacitors also showed very low gate leakage current density in the 10^{-8} A/cm^2 range which demonstrates a low trap density inside ALD Al_2O_3 dielectric. Overall, these results indicate that Al_2O_3/InAs capacitor which has high inversion charge density with low leakage current is an attractive candidate for high-performance low power logic device applications.

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