The influences of surface treatment and gas annealing conditions on the inversion behaviors of the atomic-layer-deposition Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor

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The inversion behaviors of atomic-layer-deposition Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors are studied by various surface treatments and postdeposition annealing using different gases. By using the combination of wet sulfide and dry trimethyl aluminum surface treatment along with pure hydrogen annealing, a strong inversion capacitance-voltage (C-V) response is observed, indicating a remarkable reduction in interface trap state density (D_{it}) at lower half-part of $In_{0.53}Ga_{0.47}As$ band gap. This low D_{it} was confirmed by the temperature independent C-V stretch-out and horizontal C-V curves. The x-ray photoelectron spectroscopy spectra further confirm the effectiveness of hydrogen annealing on the reduction of native oxides. © *2010 American Institute of Physics*. [doi:10.1063/1.3467813]

High carrier mobility III-V compound semiconductors are regarded as one of the best channel materials for the high performance low power complementary metal-oxide-semiconductor transistor application.[1] Among III-V compounds, the ternary alloy $In_{0.53}Ga_{0.47}As$ lattice matched to InP is one of the most attractive materials to be used due to its high low-field electron mobility and high saturation velocity.[2] Although many significant results were achieved on the fabrication of devices incorporation high dielectric constant (high k) materials on III-V channel,[3,4] the high trap state density (D_{it}) at high k/III-V compounds interface remains a main challenge. It is still too high to be implemented into upcoming technology nodes below 22 nm causing threshold voltage shifts and instabilities as well as a reduction in the effective channel mobility.[5] Recently, Lin *et al.* reported the true inversion behavior in Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitor (MOSCAPs) by using sulfide treatment and postdeposition annealing (PDA) in forming gas.[6] This implies low interface states at upper-half band gap of p-$In_{0.53}Ga_{0.47}As$. For n-type InGaAs material, a similar result has not yet been achieved. There are many reports studying on atomic layer deposited different kind of high k materials such as ZrO_2,[2,7] Al_2O_3,[6,8] HfO_2,[9–12] $AlLaO_3$ (Ref. 13) on n-$In_{0.53}Ga_{0.47}As$ with various surface treatments. However, the results always exhibited the "bump" on capacitance-voltage (C-V) curves in inversion region, implying high interface trap states at lower-half part of band gap. In this paper, we examine the inversion behavior of C-V curves on atomic layer deposition (ALD) Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs by using the combination of *ex situ* sulfide solution surface treatment and *in situ* trimethyl aluminum (TMA) pretreatment. Strong inversion layer was achieved after using this treatment and H_2 gas PDA.

The wafers used in this study were solid source molecular beam epitaxy grown 100 nm n-$In_{0.53}Ga_{0.47}As$ layer ($5\times10^{17}/cm^3$ doping) on n^+-InP substrates. After degreasing in acetone and isopropanol, the native-oxide-covered sample without surface treatment (sample S1) and the sample after wet sulfide treatment were loaded into the ALD chamber. The wet sulfide treatment was performed using 1 min HCl: $H_2O=1:10$ solution followed by 20 min $(NH_4)_2S$ (20%): $H_2O=1:3$ solution at room temperature. In the ALD chamber, *in situ* TMA pretreatments had been employed by using ten cycles of TMA/N_2 (half ALD cycles) followed by the growth of 180 cycles (~18 nm) of Al_2O_3 films. High purity N_2 was used as purging gas and wafers were kept at 300 °C during both pretreatment and deposition processes. After oxide deposition, sample S1 and sulfide-treated sample (sample S2) were both annealed at 500 °C in N_2 gas for 10 min. Another sulfide-treated sample (sample S3) was postdeposition annealed at 500 °C in H_2 gas for 10 min. Ti/Pt/Au gate metal was subsequently deposited and formed by lift-off process. Finally, Au/Ge/Ni/Au back side Ohmic contact was deposited and postdeposition annealed at 400 °C in N_2 gas for 30 s.

The multifrequency capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics were measured using an HP4284A LCR meter. The x-ray photoelectron spectroscopy (XPS) measurement was also performed to probe chemistry at the oxide/n-InGaAs interfaces. The measurement used a commercial Microlab 350 XPS system equipped with an Al $K\alpha$ source.

For the samples with PDA in N_2 (samples S1 and S2), the C-V multifrequency responses (1 kH–1 MHz) are shown in Fig. 1, the inset in Fig. 1(b) is the corresponding conductance-voltage (G-V) curves of sample S2. At the gate voltage ranges from −4 to −1 V, sample S1 exhibits inversion bumps at high frequency and low frequency-like behavior at frequency smaller than 10 kHz as shown in Fig. 1(a). This C-V response is similar to previous reports[9–11,13,14] and

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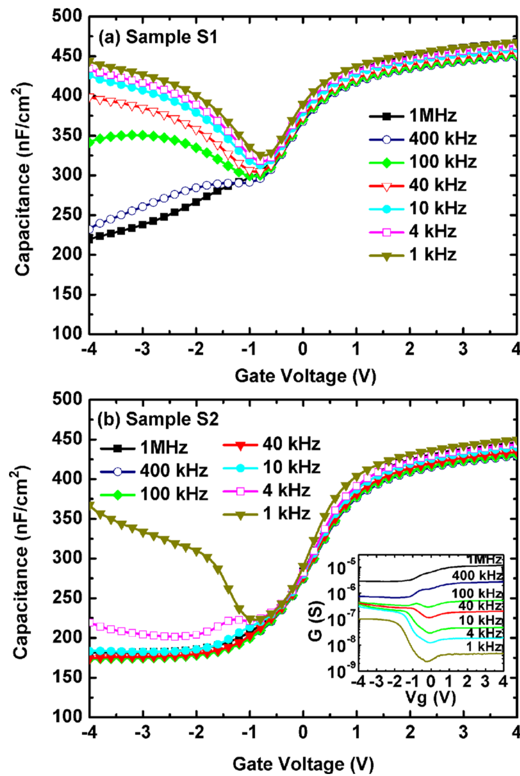

FIG. 1. (Color online) Multifrequency C-V responses in (a) TMA treated and (b) sulfide+TMA treated $Al_2O_3/n-In_{0.53}Ga_{0.47}As$ MOSCAPs, with PDA in N_2 gas. The inset in Fig. 1(b) shows the conductance-voltage (G-V) characteristics of the sample S2.

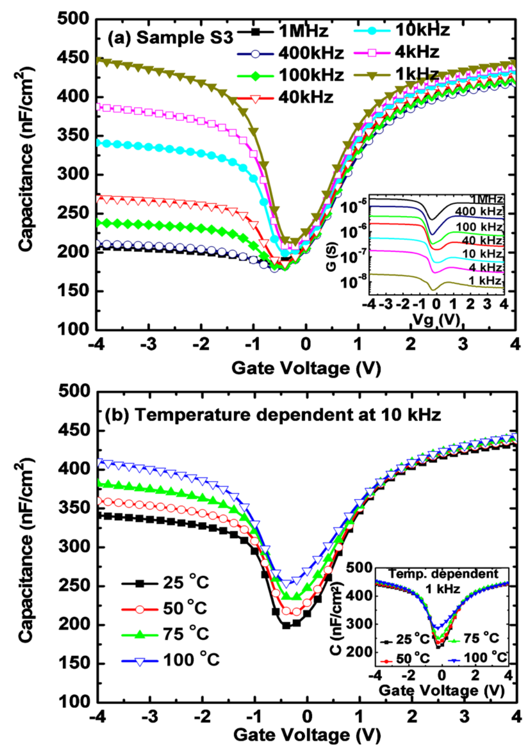

FIG. 2. (Color online) (a) Multifrequency C-V responses in sulfide+TMA treated $Al_2O_3/n-In_{0.53}Ga_{0.47}As$ MOSCAPs, with PDA in H_2 gas. (b) The temperature dependent C-V responses at 10 kHz of the same sample. The inset in Fig. 2(a) shows the conductance-voltage (G-V) characteristics; the inset in Fig. 2(b) shows the temperature dependent C-V responses at 1 kHz.

it is believed this behavior dominated by the high interface trapping states.[9,10,14] The C-V curves of sample S2 shows low frequency behavior with inversion carrier layer occurred at a frequency around 4 kHz. The observed inversion layer originates from (i) the abrupt change in C-V curves from depletion region to inversion region and (ii) the absence of the G-V peaks at frequency smaller than 10 kHz [see the inset in Fig. 1(b)]. The absence of G-V peaks indicates that the contribution of interface trap loss to the conductance is virtually masked by the contribution of inversion carrier loss.[15] The appearance of the inversion layer implies the reduction in trapping states at lower half-part of the band gap.

Figure 2(a) shows the multifrequency C-V responses of sample S3, the inset in this figure shows the corresponding G-V curves. "Low-frequency" C-V behavior with "flat," no bump inversion response at frequency as high as 1 MHz indicates that the minority carriers (holes) could be generated and freely moving to form an inversion layer. This is confirmed by the absence of G-V peaks due to the inversion carrier loss as shown in the inset in Fig. 2(a). The "free" inversion generation implies large decrease in interface trapping effect, i.e., a significant reduction in interface traps density at lower half-part of InGaAs band gap. High inversion capacitance equal to oxide capacitance (C_{ox}) was obtained at frequency around 1 kHz [Fig. 2(a)], implying that at this value of frequency, minority carriers response freely to signal and forms a fully inverted layer. This result is consistent with previous report,[11] which estimated the response time, τ_R of minority carrier in $n-In_{0.53}Ga_{0.47}As$ is about 10^{-3} s.

Figure 2(b) shows the C-V characteristics measured at 10 kHz at different temperatures for sample S3. The increase in minority carrier response time, τ_R versus temperature is clearly seen as evidenced by the increase in inversion capacitance. At frequency of 1 kHz, a fully inversion layer is formed, thus, the inversion capacitance becomes independent of temperature [the inset in Fig. 2(b)]. As show in Fig. 2(b), the accumulation capacitance is almost unchanged and the C-V curves do not shift horizontally with the temperature. The inset in Fig. 2(b) shows clearly the identical C-V stretch-out at different temperatures. These characteristics further confirm the reduction in interface charge trap density.

The As $2p_{3/2}$, In $3d_{5/2}$, and Ga $2p_{3/2}$ XPS spectra of the native oxide-covered InGaAs surface, the $Al_2O_3/InGaAs$ interface as deposited and after PDA in N_2 and H_2 gases are shown in Figs. 3(a) and 3(f), respectively. Although TMA treatment is effective in the reduction in As–O and Ga–O bonds as shown in Fig. 3(b), the amount of native oxides is still significant. A strong surface cleaning effect was made by using sulfide treatment followed by TMA pretreatment as indicated by the decrease in the native oxides signals in Fig. 3(c). By using TMA pretreatment, further removal of the native oxides is expected after sulfide treatment.[16] From Figs. 3(d) and 3(e), it is clearly seen that the decrease in As_2O_3 oxide results in the increase relative signal of the Ga-related oxides after annealing in N_2. For the sample with TMA treatment only, significant amount of As_2O_3 oxide is still remaining [Fig. 3(d)]. In contrast, as shown in Fig. 3(f), by using H_2 annealing, the As_2O_3 was almost completed removed while the reduction of Ga-related oxides also occurred but with a slightly increase of Ga–O/S bonds. The In-related oxides seem to be stable after both N_2 and H_2 annealing as indicated by the very similar In $3d_{5/2}$ spectrum of the samples before and after annealing.

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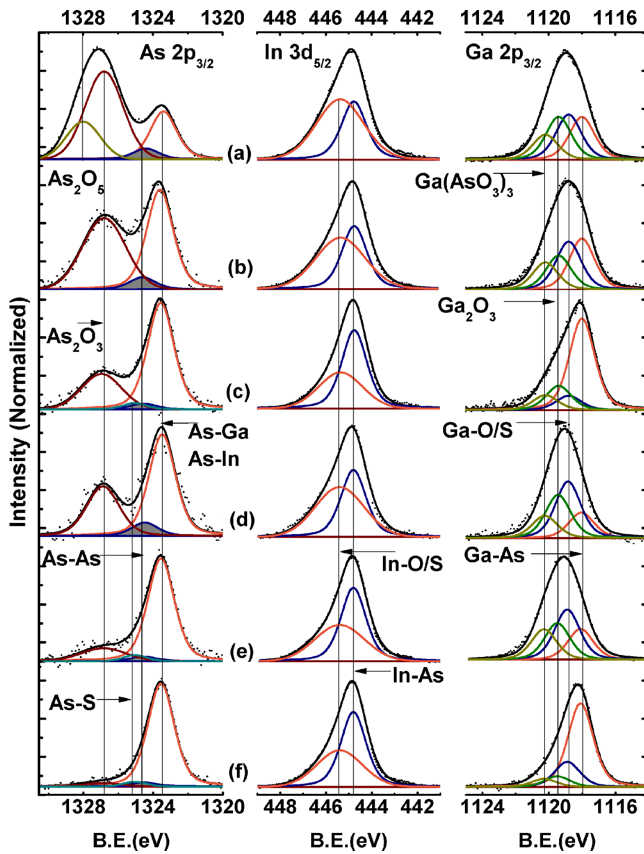

FIG. 3. (Color online) The As $2p_{3/2}$, In $3d_{5/2}$, Ga $2p_{3/2}$ XPS spectra of (a) native oxide-covered InGaAs surface; (b) TMA treated sample, with ALD Al_2O_3, as deposited; (c) sulfide+TMA treated sample, with ALD Al_2O_3, as deposited; (d) TMA treated sample, with ALD Al_2O_3, after PDA in N_2; (e) sulfide+TMA treated sample, with ALD Al_2O_3, after PDA in N_2; (f) sulfide+TMA treated sample, with ALD Al_2O_3, after PDA in H_2.

Figure 4(a) shows the C-V responses of samples at frequency of 1 kHz. The simulation results of oxide/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs shows that the C-V curve of ideal device without any interface state density has an asymmetrical sharp with higher slope at negative voltage side and low minimum capacitance value, C_{min}.[17] According to this result, in our case, the C-V characteristic of sample S3 indicates that this curve approach closest to the ideal curve as compared to either S1 or S2 (Fig. 4). By comparison, the evidence of high interface state density in sample S1 exhibited by the observation of highest value of C_{min} as well as accumulation capacitance, C_{acc}.[17] The conductance method

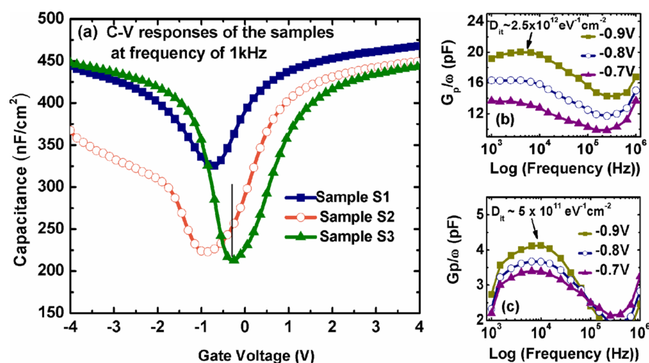

FIG. 4. (Color online) (a) The comparison of C-V responses of sample S1, sample S2, and sample S3 at frequency of 1 KHz; (b) and (c) the G_p/ω-f curves of sample S1 and sample S2, where G_p is the parallel conductance and ω is the measured angular frequency.

with the application limited to the depletion region is used to estimate the interface trap density near midgap of sample S1 and sample S2.[18] From the Gp/ω versus frequency curves shown in Figs. 4(b) and 4(c), the values obtained are about 2.5×10^{12} eV^{-1} cm^{-2} and 5×10^{11} eV^{-1} cm^{-2}, respectively, for sample S1 and S2. For sample S3, the inversion layer occurred at frequency as high as 1 MHz and the use of conductance method will overestimate. The D_{it} value of this sample, however, is smaller than that of sample S2, i.e., $<5\times10^{11}$ eV^{-1} cm^{-2}.

In conclusion, the effects of various surface treatments and different gas annealing conditions on the electrical characteristics of ALD Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors were studied. We report the true inversion channel in Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor structure by using the combination of *ex situ* sulfide treatment and *in situ* TMA pretreatment passivated surface and PDA in pure H_2 gas. Both C-V and XPS data show a strong effect of H_2 annealing on the reduction in interface trapping states. A true inversion behavior supports an evidence of the free movement of Fermi level at lower half-part band gap. However, further work is needed verify if it is a truly unpinned Fermi level.

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