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Investigation of scalability of $In_{0.7}Ga_{0.3}As$ quantum well field effect transistor (QWFET) architecture for logic applications

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ABSTRACT

In this paper, the scalability of $In_{0.7}Ga_{0.3}As$ QWFET is investigated using two-dimensional numerical drift–diffusion simulation. Numerical drift–diffusion simulations were calibrated using experimental results on short-channel $In_{0.7}Ga_{0.3}As$ QWFETs [7] to include the effects of velocity overshoot. Logic figures of merit (sub-threshold slope, saturated threshold voltage, drain induced barrier lowering, I_{ON}/I_{OFF} ratio over a specified gate swing, effective injection velocity and intrinsic switching delay) extracted from the numerical simulations are in excellent agreement with the experimental data. Three alternate QWFET device architectures are proposed and thoroughly investigated for 15 nm node and beyond logic applications. Amongst them, double-gate $In_{0.7}Ga_{0.3}As$ QWFET shows the best scalability in terms of logic figures of merit, thus making it an ideal candidate for the design and demonstration of the ultimate scaled transistor.

1. Introduction

In today's multi-core CPU era, as the dimension of silicon CMOS continues to scale to meet the ever increasing demand for higher transistor count, the rising power dissipation (both static and dynamic) has been identified as the critical brick wall to transistor scaling [1]. Aggressive supply voltage scaling to 0.5 V and below while maintaining transistor performance is a direct path toward reducing power consumption. In this regard, III-V compound semiconductor based quantum well field effect transistors (QWFETs) have recently attracted attention for low-power logic applications [2–4]. High indium content indium gallium arsenide ($In_{0.7}Ga_{0.3}As$), indium arsenide (InAs) and indium antimonide (InSb) QWFETs exhibit excellent electron transport property at both low and high electric fields arising from a combination of: (i) low Γ-valley electron mass, (ii) reduced impurity scattering due to modulation doping, (iii) reduced interface roughness scattering because of epitaxially grown smooth interfaces and (iv) large energetic separation between Γ and L-valleys. The low electron transport mass coupled with minimal back scattering from the channel back into the source gives rise to higher source side effective injection carrier velocity (v_{eff}). The expected enhancement in injection velocity is sufficient to compensate for lower carrier density in the channel of III–V QWFETs due to the reduced density of states from lower band mass compared to Si MOSFETs, and, hence, expected to deliver higher ON-current particularly at reduced supply voltages compared to Si MOSFETs, thus enabling supply voltage scaling [5,6]. However, a key question persists on the scalability of the QWFET and its ability to compete with Si MOSFETs at lower supply voltage for the 15 nm technology node and below.

Recently, higher indium concentration $In_{0.7}Ga_{0.3}As$ and InAs channel QWFETs have been experimentally demonstrated with gate length (L_G) down to 50 nm with excellent short channel performance and high speed response operating at 0.5 V supply voltage [7–9], albeit with large separation between the source and drain metal electrodes (L_{SD} = 2 μm). In order to implement III–V QWFETs in future high-performance logic applications, its scalability both in terms of physical gate length as well as the overall footprint of the transistor should be thoroughly investigated.

In this paper, we provide a systematic study of the scalability of $In_{0.7}Ga_{0.3}As$ QWFETs via two-dimensional numerical drift–diffusion (DD) simulation [10]. The paper is organized as follows. In Section 2, we perform calibration of the numerical simulator to the experimental 50 nm L_G $In_{0.7}Ga_{0.3}As$ QWFETs [7,8], to match both the ON-current in linear and saturation regime as well as the sub-threshold response. In Section 3, we investigate the effect of both lateral and vertical scaling on the $In_{0.7}Ga_{0.3}As$ QWFET device

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performance down to physical gate length of 15 nm. In Section 4, we extract the effective carrier mobility in short-channel QWFETs and conclude that, with aggressive L_G scaling, the ballistic mobility limits the short channel mobility due to near ballistic transport in the channel, and conclude that the effective carrier injection velocity, v_{eff}, near the source side is a quantitative and more pertinent indicator of transport in short-channel QWFETs than effective mobility. Finally, in Section 5, we provide a quantitative estimate of the degradation of short-channel performance of conventional $In_{0.7}Ga_{0.3}As$ QWFETs with $L_G = 15$ nm. Therefore, we introduce three different QWFET architectures in this section, provide a quantitative assessment of the logic figure of merit of three QWFETs, and propose the design for the ultimate scaled $In_{0.7}Ga_{0.3}As$ QWFET architecture suitable for 15 nm technology node and beyond logic applications. The proposed architecture is generic and could be applied to next generation antimonide-based QWFETs such as $InAs_xSb_{1-x}$ and $In_yGa_{1-y}Sb$, currently under investigation [11].

2. Device simulation

Fig. 1 presents the schematic of the simulated and experimental $In_{0.7}Ga_{0.3}As$ QWFET. The dimensions of the device are identical to those reported in [7]. The composite channel consists of 3/8/4 nm thick $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ and features both regular and buried-Pt gate stack with $L_G = 50$ nm in direct contact with the upper $In_{0.52}Al_{0.48}As$ barrier forming a Schottky junction. The $In_{0.52}Al_{0.48}As$ barrier is doped with Si delta-doping of 5.5×10^{12} cm^{-2} which is placed 3 nm above the composite channel to provide electron carriers into the channel. The 20 nm thick $In_{0.53}Ga_{0.47}As$ cap layer is n-type, heavily-doped one with 1×10^{19} cm^{-3}. The devices have total channel thickness of $T_{CH} = 15$ nm, the lateral spacer thickness (distance between the $n+$ doped layer and the gate electrode) of $L_{SIDE} = 80$ nm and a source to drain electrode spacing of $L_{SD} = 2$ μm. While the regular Pt Schottky gate device has an effective insulator thickness of $T_{INS} = 11$ nm, the buried-Pt gate device has $T_{INS} = 7$ nm. By modelling the same device structure as the real device, we attempt to simulate the associated access resistance including the contact ones ($R_{CONTACT} = 50\ \Omega\ \mu m$).

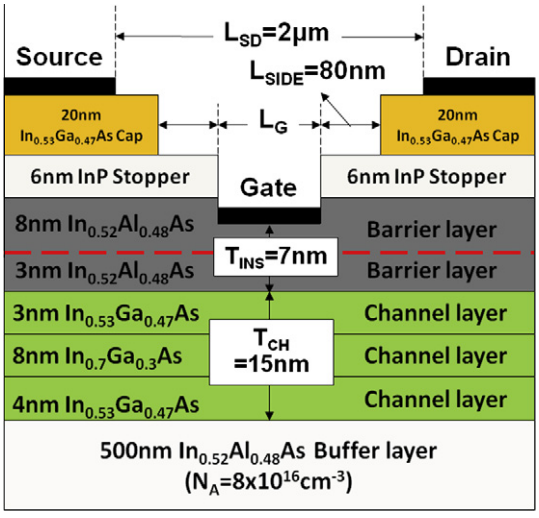

Fig. 1. Schematic of $In_{0.7}Ga_{0.3}As$ QWFET device structure. The insulator thickness (T_{INS}), the channel thickness (T_{CH}), the distance between source and drain (L_{SD}), and the distance between the gate and cap layer (L_{SIDE}) are specified. While the regular Pt Schottky gate device has an effective insulator thickness of $T_{INS} = 11$ nm, the buried-Pt gate device has $T_{INS} = 7$ nm. For the calibration, the gate length (L_G) is equal to 50 nm.

The two dimensional numerical simulation self-consistently solves the Poisson's equation with carrier continuity equation using a drift–diffusion model. To accurately capture the non-equilibrium carrier transport (such as velocity overshoot effect), we employ the Canali mobility model (1) [12] with appropriate modifications.

$$\mu(E) = \frac{(\alpha+1)\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{low}E}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \quad (1)$$

The model parameters are determined by matching the simulation results to the experimental results. The parameters used in the calibration exercise are $\mu_{low}(In_{0.7}Ga_{0.3}As) = 12{,}000$ cm^2/V s, $\mu_{low}(In_{0.53}Ga_{0.47}As) = 10{,}000$ cm^2/V s, $v_{sat} = 9.5 \times 10^7$ cm/s, $\alpha = 0$ and $\beta = 0.6$. Here, v_{sat} is the saturation velocity and β is a constant reflecting the steepness of the carrier velocity profile in the channel. They are defined as $v_{sat} = 0.93 \times 10^7$ cm/s and $\beta = 2$ for electrons by default. However, in order to take into account the velocity overshoot effect at high fields and maintain the accurate velocity at low fields, a high saturation velocity value and a lower than unity beta value are used within the drift–diffusion simulation framework, which is similar to the approach outlined by Bude [13]. Therefore, it leads to accomplish simulation time efficiency and accuracy simultaneously [14].

In order to calibrate the simulation results with the experimental results in [7], two 50 nm gate-length $In_{0.7}Ga_{0.3}As$ QWFET designs with regular and buried-Pt gate electrodes are simulated with $T_{INS} = 7$ nm and $T_{INS} = 11$ nm, respectively. Fig. 2 shows excellent agreement between the simulated and the experimental results in both sub-threshold as well as in upper-threshold regime, thereby validating the approximation of the carrier transport model and the model parameters defined in this paper. The gate leakage portion of the device transfer characteristics was not modelled in our simulation results, and will not affect the conclusions obtained in the succeeding sections.

3. Effect of lateral and vertical scaling

In this section, we first assess the impact of physical gate length scaling on the performance of conventional $In_{0.7}Ga_{0.3}As$ QWFETs for 15 nm logic applications and beyond. We simulate $In_{0.7}Ga_{0.3}As$ QWFETs with buried-Pt gate ($T_{INS} = 7$ nm, $T_{CH} = 15$ nm) for different gate-lengths ranging from 15 to 200 nm and evaluate the various

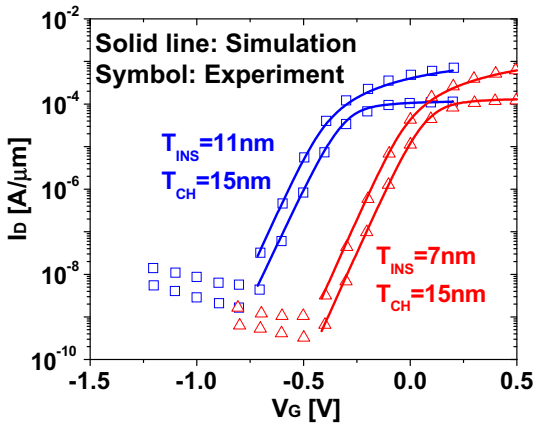

Fig. 2. Transfer characteristics of 50 nm L_G $In_{0.7}Ga_{0.3}As$ QWFETs featuring both the regular Pt Schottky gate and the buried-Pt gate. The simulation results are calibrated when $T_{INS} = 11$ nm (blue, solid) and $T_{INS} = 7$ nm (red, solid). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

figures of merit such as sub-threshold slope (SS), drain-induced barrier lowering (DIBL), threshold voltage (V_t) roll-off, and I_{ON}/I_{OFF} ratio. The figures of merit are compared with the experimental results [7] as illustrated in Fig. 3. As a result of the L_G scaling, it results in large DIBL, causing the degradation of SS. This is accompanied by significant V_t roll-off trend and the consequent decrease in I_{ON}/I_{OFF} ratio. To extract the I_{ON} and I_{OFF}, we have applied the methodology outlined by Chau et al. [1]. First, V_t is defined as a value of gate voltage where the drain current (I_D) corresponds to 1 μA/μm. Then, I_{ON} is determined from the value of I_D at which V_{GS} corresponds to approximately two-third of V_{CC} above V_t. In a similar manner, I_{OFF} is chosen as I_D where V_{GS} is one-third of V_{CC} below V_t.

Intrinsic gate delay (CV/I), as shown in Fig. 4, is another important figure of merit for high-speed logic applications. In extracting the CV/I, C is the gate capacitance (C_{GG}) defined at the same gate bias condition as I_{ON}, I is I_{ON} and V is the supply voltage of operation. The gate capacitance takes into account the barrier capacitance as well as the quantum capacitance in the channel arising from the limited density of states (DOS) as well as the parasitic capacitance from the gate to source/drain fringing electric field. The total gate capacitance is reduced with reducing L_G due to geometric effect, thereby, leading to the decrease in gate delay. However, at L_G = 15 nm, the inherent parasitic capacitances arising from gate to source/drain fringing electric field form a significant portion of the total gate capacitance, and, therefore, C_{GG} is hardly reduced further [15,16]. In addition, I_{ON} is greatly decreased due to poor electrostatics, thus adversely affecting the total gate delay.

In addition to L_G scaling, L_{SIDE} needs to be scaled in order to achieve a small device footprint needed for 15 nm or below. Initially, L_{SIDE} is kept at 80 nm and subsequently decreased to 15 nm. Table 1 summarizes the loss in electrostatic integrity of the QWFET as a direct consequence of L_{SIDE} scaling at the 15 nm L_G. To sustain a scaling path for QWFET with 15 nm physical gate length, we first normalize the physical gate length to the electrostatic scaling length of the device. As Yan et al. indicate in [17], the scaling rule is dictated by both electrostatic scaling length (λ) in (2) and aspect ratio ($\gamma = L_G/\lambda$).

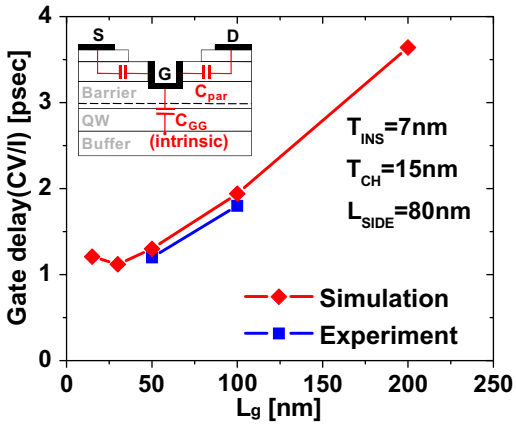

Fig. 4. Intrinsic gate delay (CV/I) versus L_G for $In_{0.7}Ga_{0.3}As$ QWFETs.

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{Si} t_{ox}} \tag{2}$$

Here, the electrostatic model originally developed for fully-depleted SOI MOSFETs (FD-MOSFETs) is applicable for conventional $In_{0.7}Ga_{0.3}As$ QWFETs and λ is calculated to be 10 nm by taking the relative contribution of $In_{0.52}Al_{0.48}As$ and composite channel InGaAs layer and their effective permittivity values into account [17,18]. To maintain the appropriate sub-threshold behaviour, γ should be maintained at least at 5 and higher. Therefore, one of the promising options is the vertical scaling of the conventional $In_{0.7}Ga_{0.3}As$ QWFETs leading to reduction of both T_{INS} and T_{CH}. Table 1 summarizes the improvement in the device performance with the vertical scaling. The insulator thickness and the channel thickness are reduced from 7 to 4 nm and from 15 to 7 nm, respectively. The simulation results indicate that vertical scaling indeed contributes to a better electrostatic integrity and, thereby improves the SS, DIBL, V_t-roll off and I_{ON}/I_{OFF} ratio. To further improve the electrostatic integrity of the $In_{0.7}Ga_{0.3}As$ QWFETs, we also investigate the effect of compensation doping (N_A) of the bot-

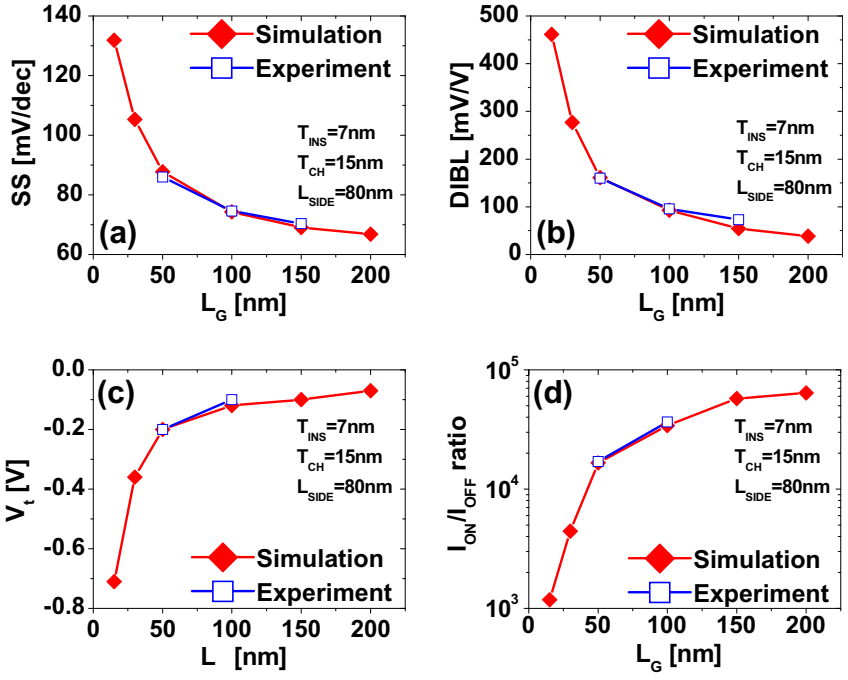

Fig. 3. Logic figures of merit for $In_{0.7}Ga_{0.3}As$ QWFETs with different L_G. $In_{0.7}Ga_{0.3}As$ QWFETs with buried-Pt gate (T_{INS} = 7 nm, T_{CH} = 15 nm) for different gate-lengths ranging from 15 to 200 nm are designed and the logic figures of merit (SS, DIBL, V_t, I_{ON}/I_{OFF} ratio) are extracted.

Table 1
Device performance comparison. At L_G = 15 nm, L_{SIDE} is reduced from 80 nm to 15 nm (in column 2). To further improve the device performance, T_{INS} and T_{CH} are reduced from 7 nm to 4 nm and from 15 nm to 7 nm, respectively (in column 3). To increase the buffer layer doping (N_A) to 1×10^{18} cm^{-3} leads to improvement in the electrostatic integrity, but the increase in access resistance suppresses the ON-current (in column 4). Bold values indicate the change in the current simulation from the previous simulation.

L_G = 15 nm (V_{CC} = 0.5)	T_{INS} = 7 nm T_{CH} = 15 nm L_{SIDE} = 80 nm $N_A = 8 \times 10^{16}$ cm^{-3}	T_{INS} = 7 nm T_{CH} = 15 nm **L_{SIDE} = 15 nm** $N_A = 8 \times 10^{16}$ cm^{-3}	**T_{INS} = 4 nm** **T_{CH} = 7 nm** L_{SIDE} = 15 nm $N_A = 8 \times 10^{16}$ cm^{-3}	T_{INS} = 4 nm T_{CH} = 7 nm L_{SIDE} = 15 nm **$N_a = 1 \times 10^{18}$ cm^{-3}**
DIBL (mV/V)	461.3	595	298	135.7
SS (mV/dec)	131.9	152.6	109.9	101.8
$V_{t,sat}$ (V)	−0.71	−0.85	−0.24	0.26
I_{ON}/I_{OFF}	1.18×10^3	5.71×10^2	3.59×10^3	4.67×10^3
I_{ON} (A/μm)	6.890×10^{-5}	4.963×10^{-5}	1.184×10^{-4}	1.115×10^{-4}

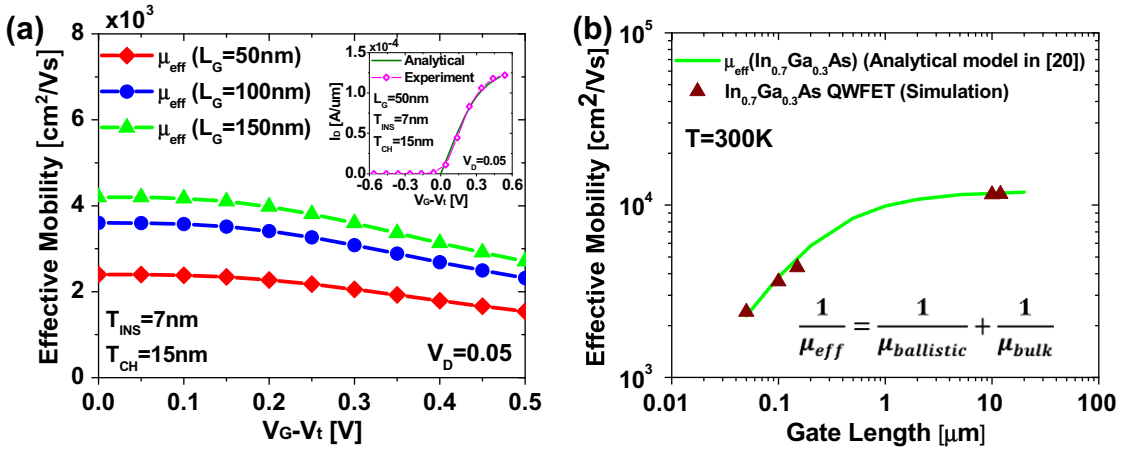

Fig. 5. (a) The effective mobility as a function of gate bias for $In_{0.7}Ga_{0.3}As$ QWFETs with 50 nm, 100 nm and 150 nm L_G. (b) The effective mobility as a function of L_G for $In_{0.7}Ga_{0.3}As$ QWFETs. The effective mobility values of QWFETs (brown, triangle) from simulations are in close agreement with the one obtained from Mathiessen's rule $\left(1/\mu_{eff} = 1/\mu_{ballistic} + 1/\mu_{bulk}\right)$ in [20] (green, solid). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

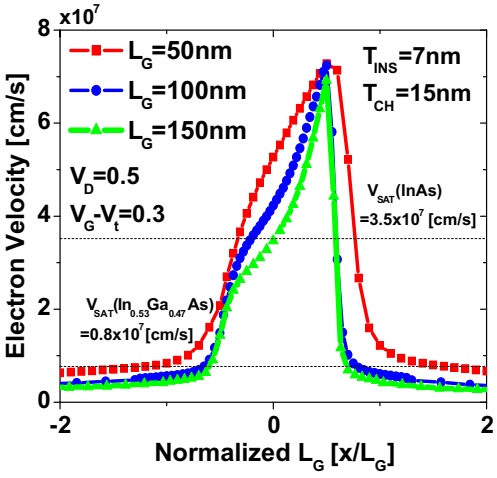

Fig. 6. The effective carrier injection velocity profile in the channel with the channel normalized. v_{eff} for 50, 100 and 150 nm L_G $In_{0.7}Ga_{0.3}As$ QWFETs is directly extracted from the simulation at the conduction band peak near the source end at V_D = 0.5 V and $V_G - V_t$ = 0.3 V. v_{sat} for InAs and $In_{0.53}Ga_{0.47}As$ are obtained from [23].

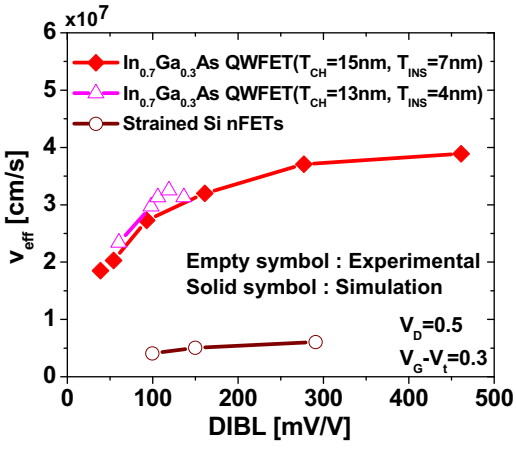

Fig. 7. The effective carrier injection velocity (v_{eff}) versus DIBL for various L_G $In_{0.7}Ga_{0.3}As$ QWFETs from simulations (solid) with the experimental data for-$In_{0.7}Ga_{0.3}As$ QWFET and strained Si nFETs (symbols) at V_D = 0.5 V and $V_G - V_t$ = 0.3 V. $In_{0.7}Ga_{0.3}As$ QWFETs from simulations have T_{INS} = 7 nm and T_{CH} = 15 nm, while the experimental $In_{0.7}Ga_{0.3}As$ QWFETs from [24,25] have T_{INS} = 4 nm and T_{CH} = 13 nm. Also, v_{eff} for strained Si nFETs is plotted together at the same bias conditions.

tom barrier layer on the device performance. As N_A is increased from 8×10^{16} cm^{-3} to 1×10^{18} cm^{-3}, both DIBL and SS improve and V_t increases. However, increasing the buffer layer doping results in higher access resistance, as the increased p-type doping in the bottom barrier layer pinches off the access regions leading to high R_{EXT}, which reduces the ON-current, as shown in Table 1.

4. Ballistic effect and short channel transport

As the device dimension is scaled down, there is a transition in device transport behavior from the diffusive toward the ballistic limit. Unlike silicon MOSFETs with moderate mobility values,

QWFETs with III–V compound semiconductors possess high electron mobility up to 15,000 $cm^2/V\,s$ or even higher. For example, $In_{0.7}Ga_{0.3}As$ QWFET has a low-field electron mobility of 12,000 $cm^2/V\,s$ with carrier density of $2 \times 10^{12}\ cm^{-2}$ in the channel and thus, its mean-free-path is calculated to be approximately 150 nm. Therefore, QWFETs with gate-length approaching 15 nm are expected to operate close to the ballistic limit [19] across a range of operating bias conditions. In order to quantify the significance of ballistic transport, we have investigated the short-channel mobility of QWFETs in detail in this section.

As mentioned earlier, the high carrier mobility in long channel III–V based QWFET arises from a combination of its low electron mass, reduced Columbic scattering and lower interface roughness scattering. However, in the short-channel QWFETs, electrons are launched with thermal velocity (V_{th}) from source into the channel and traverse the channel encountering few collisions. In such a scenario, the actual channel resistance is weakly dependent on the physical gate length of the device, and any attempt to estimate the short-channel mobility as a function of L_G results in values lower than their long channel values. In this respect, the effective carrier mobility for short-channel devices operating close to the ballistic limit is primarily limited by the so-called "ballistic mobility", whereas the one for long-channel devices is primarily governed by the bulk mobility. The ballistic mobility is given by Eq. (3) in [20].

$$\mu_{ballistic} = \frac{2qL}{\pi m V_{th}} \tag{3}$$

In order to extract the effective mobility for short-channel $In_{0.7}Ga_{0.3}As$ QWFETs, the experimental transfer characteristics of $In_{0.7}Ga_{0.3}As$ QWFETs (50 nm, 100 nm and 150 nm L_G) are obtained [7,8].

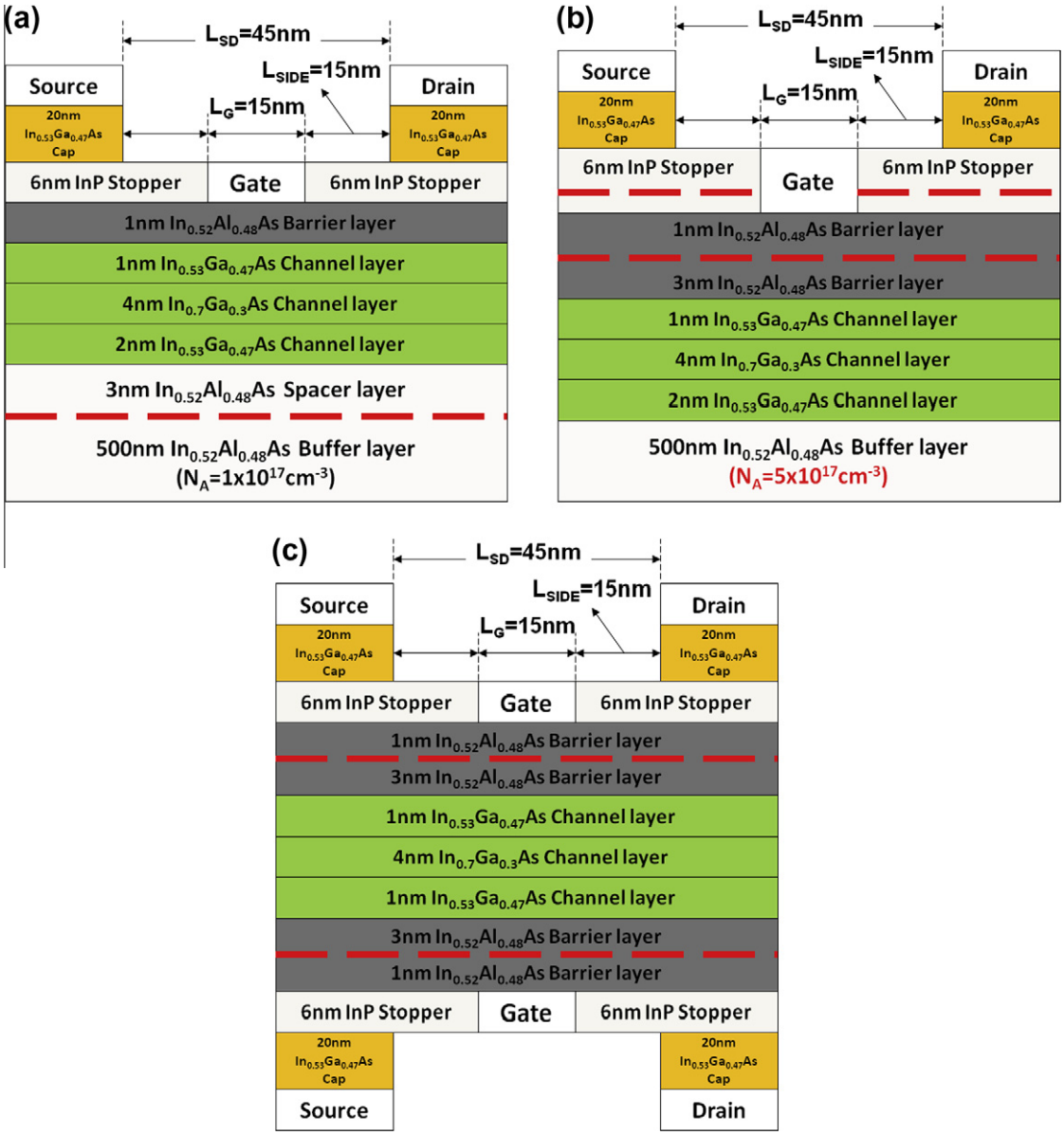

Fig. 8. (a) Schematic of 15 nm L_G inverted-$In_{0.7}Ga_{0.3}As$ QWFET with T_{INS} = 1 nm and T_{CH} = 7 nm. (b) Schematic of 15 nm L_G $In_{0.7}Ga_{0.3}As$ QWFET with high bottom-barrier doping ($N_A = 5 \times 10^{17}\ cm^{-3}$), T_{INS} = 4 nm and T_{CH} = 7 nm. To mitigate the higher access resistance problem, the second delta doping layer is incorporated 1 nm above $In_{0.52}Al_{0.48}As$ barrier layer in the InP etch stopper layer. (c) Schematic of 15 nm L_G double-gate $In_{0.7}Ga_{0.3}As$ QWFET with T_{INS} = 4 nm and T_{CH} = 6 nm. To make suitable for 60 nm gate-pitch footprint, L_{SIDE} is aggressively reduced down to 15 nm.

$$I_D = C_{GG}\frac{w}{L_{eff}}(V_G - V_t)\frac{\mu_{low}}{(1+(\theta(V_G-V_t))^{\beta})^{\frac{1}{\beta}}}V_D \quad (4)$$

Effective electron mobility values in the linear operation regime are calculated using Eq. (4) in [21], where C_{GG} is a combination of the barrier capacitance and the centroid capacitance. Also, both θ and β are adjustable parameters to reflect the dependence of the gate electric field on the channel transport. As seen in the inset of Fig. 5 (L_G = 50 nm), the deviation of the transfer characteristic from linear *Vg* dependence at high gate bias regime is captured by introducing θ = 2.8 and β = 3 (analytical model with β = 1 and higher values of θ results in the underestimation of I_D). The adjusted θ and β match well with the experiments for 50 nm, 100 nm and 150 nm L_G $In_{0.7}Ga_{0.3}As$ QWFETs. Physically, the higher value of β used in the analytical mobility model reflects the non-stationary effect related to the velocity overshoot near the drain end.

Fig. 5a shows the effective mobility as a function of gate bias for $In_{0.7}Ga_{0.3}As$ QWFETs with 50 nm, 100 nm and 150 nm gate-length. It is clear that the effective mobility reduces as L_G is scaled down. In Fig. 5b, the effective channel mobility of short-channel QWFETs is in close agreement with the one obtained from Mathiessen's rule $(1/\mu_{eff} = 1/\mu_{ballistic} + 1/\mu_{bulk})$ in [20] which directly arises from the transmission factor being the ratio of the mean-free-path to the physical L_G. However, this apparent degradation in short channel mobility is not an actual concern for scaled $In_{0.7}Ga_{0.3}As$ QWFET performance. Rather, the effective carrier injection velocity (v_{eff}) at the conduction band peak near the source end (injection velocity) becomes more significant. The ON-current is primarily limited, not by the effective carrier mobility, but by the effective carrier injection velocity as short-channel devices enter the ballistic regime [22].

$$I_D = C_{OX}W v_T\left(\frac{t_c}{1+r_c}\right)(V_{GS} - V_t) \quad (5)$$

$$v_{inj} = v_T\left(\frac{t_C}{1+r_C}\right) \quad (6)$$

Eq. (5) shows the dependence of drain current on the transmission ($t_c = \lambda/(L+\lambda)$) and reflection coefficients ($r_c = L/(L+\lambda)$) as predicted from scattering theory [22] and Eq. (6) shows the dependence of injection velocity on the transmission coefficient. Consequently, due to the low electron mass in $In_{0.7}Ga_{0.3}As$ QWFET and very little back scattering from the channel into the source, a high injection velocity can be achieved. Further, the increase in the effective injection velocity with L_G scaling improves the drive current.

From a careful calibration of the saturation ON-current for 50 nm, 100 nm and 150 nm $In_{0.7}Ga_{0.3}As$ QWFETs [8] by adjusting v_{sat} and β [12], the effective electron velocity is directly extracted from the plot of carrier velocity profile in Fig. 6 at the conduction band peak near the source end at V_D = 0.5 V and $V_G - V_t$ = 0.3 V. InAs and $In_{0.53}Ga_{0.47}As$ v_{sat} values are obtained from [23]. Fig. 7 plots v_{eff} versus DIBL for $In_{0.7}Ga_{0.3}As$ QWFETs from 15 to 200 nm L_G. Since the effective carrier injection velocity for $In_{0.7}Ga_{0.3}As$ QWFETs in [7] is not available, it is extracted from experimental data in [24] and compared with the simulation results. The $In_{0.7}Ga_{0.3}As$ QWFETs in [24,25] possess T_{CH} = 13 nm, T_{INS} = 4 nm and L_{SI-DE} = 80 nm with the gate-length ranging from 30 to 130 nm. Their effective carrier injection velocity values were also extracted under the same bias conditions. In Fig. 7, it is clearly shown that the effective carrier injection velocity increases as the electrostatic integrity aggravates. However, at a fixed DIBL value (100 mV/V), the simulation result shows about 6.9 times higher v_{eff} for $In_{0.7}Ga_{0.3}As$ QWFETs than the one for strained Si nMOSFETs in [5] which is about 4.06×10^6 cm/s at V_D = 0.5 V and $V_G - V_t$ = 0.3 V. This increase in injection velocity for III–V compound semiconductors is a necessity in order to compensate for lower carrier density in the channel of III–V QWFETs due to the reduced density of states in $In_{0.7}Ga_{0.3}As$ QWFETs compared to Si MOSFETs.

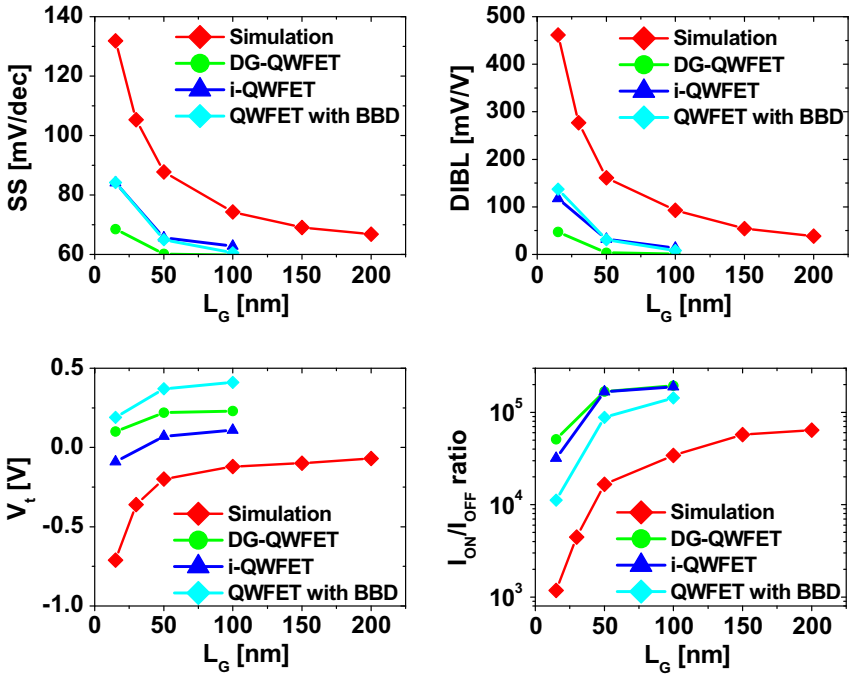

Fig. 9. Logic figures of merit for different $In_{0.7}Ga_{0.3}As$ QWFET device architectures. Compared to conventional $In_{0.7}Ga_{0.3}As$ QWFETs (red line), the scalability of all three QWFETs is improved due to better device architecture schemes. Among them, double-gate $In_{0.7}Ga_{0.3}As$ QWFET shows the best scalability and electrostatic integrity. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

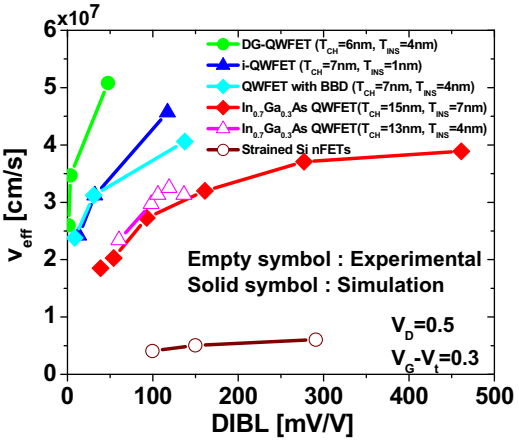

Fig. 10. The effective carrier injection velocity (v_{eff}) versus DIBL for different $In_{0.7}Ga_{0.3}As$ QWFET device architectures. It indicates that the extracted v_{eff} values for three QWFET architectures exceed that of the conventional QWFETs (red line). Consequently, amongst them, double-gate $In_{0.7}Ga_{0.3}As$ QWFETs represent the highest v_{eff} at a fixed DIBL value. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

5. Scalable QWFET architectures

Using the calibrated numerical simulation from Sections 3 and 4, three different $In_{0.7}Ga_{0.3}As$ QWFET device architectures are studied; inverted QWFET (i-QWFET), QWFET with higher bottom-barrier doping (QWFET with BBD) and double-gate QWFET (DG-QWFET). For 15 nm node and beyond logic applications, L_G and L_{SIDE} are aggressively scaled down to 15 nm, thus making them suitable for a 60 nm contacted gate-pitch.

In an inverted-$In_{0.7}Ga_{0.3}As$ QWFET design shown in Fig. 8a, T_{CH} is kept at 7 nm and T_{INS} is reduced down to 1 nm, thereby, resulting in a better gate control. The gate leakage is ignored in this study since in future devices a high-k dielectric will be integrated with the QWFET architecture [26]. Next, we have investigated the $In_{0.7}Ga_{0.3}As$ QWFETs with higher bottom-barrier doping shown in Fig. 8b, where the overall electrostatic integrity is significantly improved compared to the conventional $In_{0.7}Ga_{0.3}As$ QWFETs. This QWFET with higher bottom-barrier doping has T_{INS} = 4 nm and T_{CH} = 7 nm. Additionally, to mitigate the high access resistance associated with the carrier depletion effects arising from higher bottom barrier p-type doping, a second delta doping layer is incorporated 1 nm above the $In_{0.52}Al_{0.48}As$ barrier layer in the InP etch stopper layer. Finally, a double-gate $In_{0.7}Ga_{0.3}As$ QWFET structure is shown in Fig. 8c with T_{INS} = 4 nm and T_{CH} = 6 nm. Fig. 9 compares the logic figures of merit for the three different QWFET architectures. Compared to conventional $In_{0.7}Ga_{0.3}As$ QWFETs (red line), the scalability of all three QWFETs is improved due to better device architecture schemes. The effective carrier injection velocity versus DIBL is also plotted for three QWFET device architectures in Fig. 10. It indicates that the extracted v_{eff} values for three QWFET architectures exceed that of the conventional QWFETs (red line). However, the reason for the different peak values of v_{eff} at L_G = 15 nm originates from the relationship between the mean-free-path (λ) and the effective mobility (μ_{eff}) [19]. From $D_n = V_{th}\lambda/2$ and Einstein relation, the mean-free-path is dependent on the mobility values for the three different QWFET architectures which are different due to the gate-field dependence as captured quantitatively by the Canali transport model. Consequently, double-gate $In_{0.7}Ga_{0.3}As$ QWFETs exhibit the highest effective carrier injection velocity at a fixed DIBL value and deliver the best logic performance (SS, DIBL, V_t-roll off and I_{ON}/I_{OFF} ratio) due to its electrostatic robustness, thus making it a strong candidate for the design of the ultimate scaled transistor.

6. Conclusions

The scalability of conventional $In_{0.7}Ga_{0.3}As$ QWFETs is thoroughly investigated using a calibrated two-dimensional numerical drift–diffusion simulation. The non-equilibrium transport effect due to velocity overshoot in short channel $In_{0.7}Ga_{0.3}As$ QWFET is accurately captured in the modified drift–diffusion model. The conventional $In_{0.7}Ga_{0.3}As$ QWEFTs show a poor scaling behaviour down to L_G = 15 nm. In addition to L_G scaling, L_{SIDE} is also scaled down to achieve a small device footprint, which degrades the overall device performance further and highlights the necessity of aggressive vertical scaling of the device. The importance of ballistic effect in short-channel QWFETs is emphasized and the limitations on the extracted effective short channel mobility due to ballistic effect are examined in detail. The significance of source side injection velocity is also pointed out for III-V QWFETs, thus making v_{eff} versus DIBL an important figure of merit to benchmark various QWFET device architectures operating in the quasi or near ballistic regime. Finally, three alternate QWFET device architectures are proposed and thoroughly investigated for the 15 nm node and beyond logic applications. Amongst them, double-gate $In_{0.7}Ga_{0.3}As$ QWFET has the best logic figures of merit and the highest effective carrier injection velocity, thus making it an ideal candidate for the design and demonstration of the ultimate scaled transistor.

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