Applied Physics Express **5** (2012) 021104
DOI: 10.1143/APEX.5.021104

Effect of Postdeposition Annealing Temperatures on Electrical Characteristics of Molecular-Beam-Deposited HfO_2 on n-InAs/InGaAs Metal–Oxide–Semiconductor Capacitors

Hai-Dang Trinh, Yueh-Chin Lin, Huan-Chung Wang, Chia-Hua Chang, Kuniyuki Kakushima[1], Hiroshi Iwai[1], Takamasa Kawanago[1], Yan-Gu Lin, Chi-Ming Chen, Yuen-Yee Wong, Guan-Ning Huang, Mantu Hudait[2], and Edward Yi Chang*

Department of Materials Science and Engineering, National Chiao-Tung University, Hsinchu 30010, Taiwan, R.O.C.
[1]*Interdisciplinary Graduate School of Science and Technology, Tokyo Institute of Technology, Yokohama 226-8502, Japan*
[2]*Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, U.S.A.*

Received December 5, 2011; accepted January 7, 2012; published online January 31, 2012

The electrical characteristics of molecular-beam-deposited HfO_2/n-InAs/InGaAs metal–oxide–semiconductor capacitors with different postdeposition annealing (PDA) temperatures (400–550 °C) are investigated. Results show that the sample with the PDA temperature of 500 °C exhibits the best capacitance–voltage (C–V) behavior with small frequency dispersion and small hysteresis. The X-ray photoelectron spectroscopy (XPS) spectra show the reduction of the amount of As-related oxides to below the XPS detection level when the PDA temperature is up to 500 °C. As the PDA temperature was increased to above 500 °C, As and In atoms seem to diffuse significantly into HfO_2, resulting in the degradation of C–V behavior. © 2012 The Japan Society of Applied Physics

The integration of high-k materials on III–V compounds has been widely investigated for future high-performance low-power logic applications. Some high-k materials such as Al_2O_3, Ga_2O_3 (Gd_2O_3), ZrO_2, and HfO_2 have been studied as gate oxides.[1–6] Due to high electron mobility and bandgap in the range of 0.36–1.42 eV, $In_xGa_{1-x}As$-based metal–oxide–semiconductor (MOS) devices are potentially suitable for application at low supply voltages.[7] However, the lack of high-k/InGaAs interfacial quality has emerged as the main challenge. Many studies have been focused on various passivation methods such as using chemical solution treatments, and using interfacial passivation layers (Ge, Si, Ge/Si) to improve the quality of high-k/InGaAs interfaces.[8–11] Among the $In_xGa_{1-x}As$ materials, InAs has the highest electron mobility and thus, the InAs-based devices have potential to achieve high performance at a very low turn-on voltage ($\leq$0.5 V).[12,13] However, as compared with the numerous studies on high-k/GaAs or high-k/InGaAs structures, studies on high-k/InAs MOS capacitor (MOSCAP) structures are still limited.[2,14–17] To improve the electrical properties of high-k/InAs structures, some factors such as surface passivation methods, oxide growth conditions, and annealing conditions need to be further investigated. In this work, the electrical characteristics of HfO_2/n-InAs/InGaAs MOSCAP devices are investigated with several postdeposition annealing (PDA) temperatures. A hafnium (HfO_2)-based gate dielectric is deposited using molecular beam deposition (MBD) methods. After oxide deposition, the HfO_2/n-InAs/InGaAs structures were annealed at different PDA temperatures of 400, 450, 500, and 550 °C. The capacitance–voltage (C–V) measurements and X-ray photoelectron spectroscopy (XPS) were performed to study the influence of different post-annealing temperatures on the improvement of interface quality of the HfO_2/n-InAs/InGaAs MOS structures.

The wafers used in this work were molecular-beam-epitaxy-grown 5×10^{17} cm^{-3} Si-doped n-type 5 nm InAs/3 nm $In_{0.7}Ga_{0.3}As$/10 nm $In_{0.53}Ga_{0.47}As$ epilayers on 3-in. n^+ InP substrates. The MOS capacitor process steps include surface treatments, oxide deposition, postdeposition annealing, gate metal deposition, and formation of ohmic contact on the backside of n^+ InP substrate. After degreasing in acetone and isopropanol, the wafers were cleaned in a HF solution (49%) for 3 min, and then followed by sulfur treatment in an $(NH_4)_2S$ solution (7%) for 30 min at room temperature. The surface-treated wafers were loaded into the MBD system for the deposition of 15 nm HfO_2 at 300 °C at chamber pressure of 10^{-8} Torr. The HfO_2 target was used as oxide source, and the growth rate was control in 0.05 Å/s. After that, PDA process was performed with temperatures ranging from 400 to 550 °C in forming gas for 5 min. Finally, Ni metal (contact size: 50 μm in diameter) was deposited on the front side of the wafer as a gate contact metal and Au metal was deposited by sputtering on the backside of n+ InP substrates to complete the fabrication.

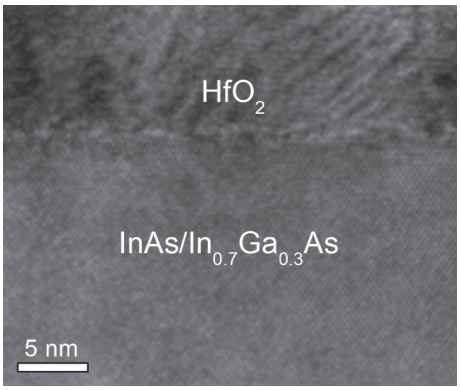

Fig. 1. Cross-sectional TEM image of the as deposited HfO_2/n-InAs/InGaAs stacks.

Figure 1 shows the cross-sectional high-resolution transmission electron microscopy (HRTEM) image of an as-deposited HfO_2/n-InAs/InGaAs sample. The TEM image shows good HfO_2/InAs stack with an indistinguishable interfacial layer. On the HfO_2/$In_{0.53}Ga_{0.47}As$ structure, which underwent a very similar process condition, the TEM image showed a thin native oxides layer between HfO_2 and $In_{0.53}Ga_{0.47}As$ (data not shown). This indicates that the

*E-mail address: edc@mail.nctu.edu.tw

 © 2012 The Japan Society of Applied Physics

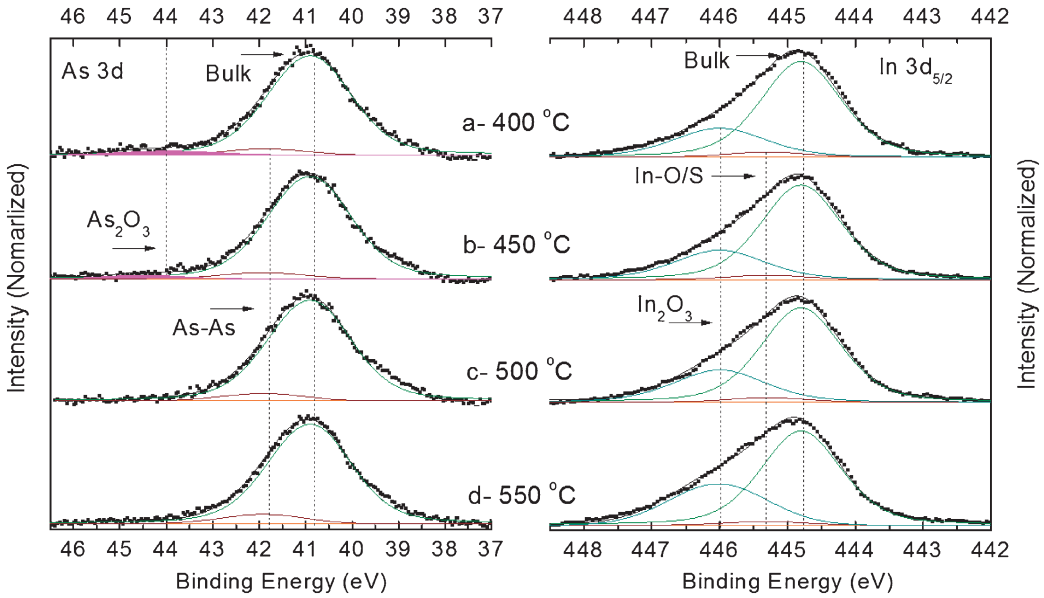

Fig. 2. As 3d and In $3d_{5/2}$ XPS spectra of samples with postdeposition annealing temperature of (a) 400, (b) 450, (c) 500, and (d) 550 °C in forming gas for 5 min.

HfO_2/InAs structure seems to have a better interfacial quality than the HfO_2/InGaAs structure. The studies of high-k/InGaAs with various In content were discussed[18,19] and it was believed that the less Ga-related oxide formation with increasing In content would result in the improvement of high-k/InGaAs interfacial quality.[7,18,19]

The As 3d and In $3d_{5/2}$ XPS spectra of samples with different PDA temperatures were obtained and analyzed as shown in Fig. 2. For XPS measurement, 2 nm MBD HfO_2 was deposited on InAs/InGaAs substrates. As shown in the As 3d spectra, the amount of As-related oxides were reduced to below the XPS detection level at the PDA temperature of 500 °C and above. Meanwhile, the In $3d_{5/2}$ spectra exhibit a slight increase of the amount of In-related oxides when the PDA temperature was up to 500 °C. Since the Gibb's free energies of As_2O_3 and In_2O_3 are −137.7 and −198.6 kcal/mol respectively,[7] the slight increase of the amount of In-related oxides could be explained by the conversion of As–O bonding to In–O bonding during thermal process. When the PDA temperature was increased to 550 °C, the As–As bonding and In-related oxides increased significantly, as shown in Fig. 2(d) by the As 3d and In $3d_{5/2}$ spectra. This indicates that at a PDA temperature of above 500 °C, the As and In atoms diffused significantly into HfO_2. A drastic increase of As–As bonding and In-related oxides was observed when the PDA temperature was up to 600 °C (data not shown).

Multifrequency C–V responses of the samples are shown in Fig. 3. The accumulation capacitance decreased as the PDA temperatures increased. It was reported that at the PDA temperature of above 500 °C, the HfO_2/semiconductor interfacial layer would increase with increasing annealing temperature, resulted in the decrease of the accumulation capacitance.[20–22] The C–V behaviors show improvement when the PDA temperature is increased from 400 to 500 °C. The sample annealed at 500 °C shows good C–V responses with a small frequency dispersion [see the inset of Fig. 3(c)] and clear accumulation/depletion/inversion regions. This is consistent with the decrease of As oxides at the HfO_2/InAs interface as indicated in the XPS spectra. At the PDA temperature of 550 °C, the C–V behavior degraded as indicated by the increase of frequency dispersion and depleted capacitance [Fig. 3(d)]. This degradation might be related to the significant increase of As–As bonding and In-related oxides.

Figure 4 shows the bidirectional C–V curves of samples at a frequency of 100 kHz. The values of C–V hysteresis near the flatband of samples are shown in the Table I. As can be seen from the figure and table, there is remarkable improvement of the C–V hysteresis, from 810 to 40 mV when the temperatures increased from 400 to 500 °C. The inset of Fig. 4 and Table I show the negative shift of flat-band voltage with the increase of PDA temperatures from 400 to 500 °C. The HfO_2 oxide was found to contain a large concentration of defects, especially oxygen vacancies.[23] These oxygen vacancies would become negative charges when the gate voltage biased from negative to positive, resulting in high positive flat-band voltage. The negative shift of flat-band voltage indicates the noticeable reduction of oxygen vacancies during annealing process at 500 °C. The C–V hysteresis was significant increased and the flat-band voltage showed positive shift again when the PDA temperature was up to 550 °C due to the significant increase of In-related oxides. The interface trap densities D_{it} of samples with different PDA temperatures were estimated by the conductance method[24] and the results are listed in Table I. It shows that the MOS capacitor with the PDA temperature of 500 °C has the lowest D_{it} of 2.7×10^{12} cm^{-2}·eV^{-1} among all the temperatures studied.

In conclusion, HfO_2/n-InAs/InGaAs metal–oxide–semiconductor capacitors with different postannealing temperatures from 400 to 550 °C were investigated. Much improvement in the C–V characteristics was observed for the sample annealed at 500 °C. When the PDA temperature increased to

© 2012 The Japan Society of Applied Physics

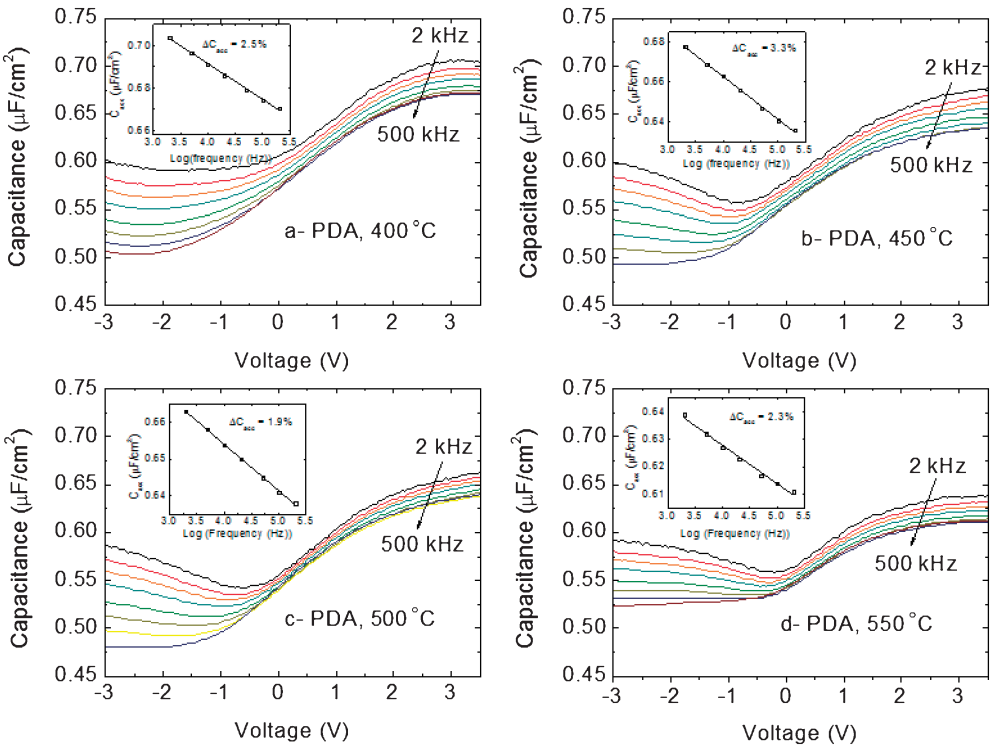

Fig. 3. Multifrequency C–V characteristics of HfO_2/n-InAs MOS capacitors with different PDA temperatures: (a) 400, (b) 450, (c) 500, and (d) 550 °C. The insets present the accumulation capacitance, C_{acc} vs measured frequency at a gate bias of 3.5 V.

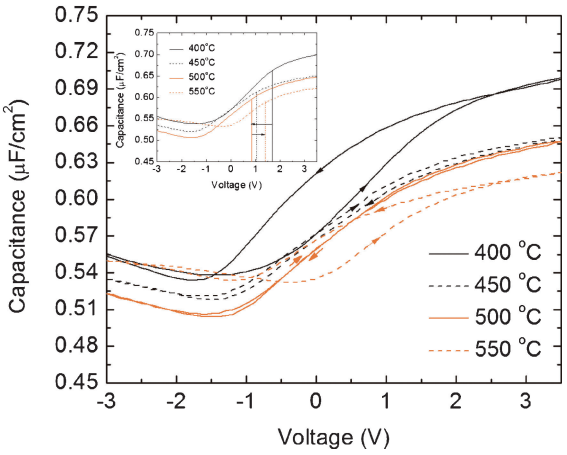

Fig. 4. Bidirectional C–V characteristics of samples measured at a frequency of 100 kHz. The inset of the figure shows the shift of the flat-band voltage with the PDA temperature.

Table I. Comparison of C–V characteristics of the HfO_2/n-InAs capacitors after annealing at different temperatures.

	PDA temperature (°C)			
	400	450	500	550
Flatband voltage (V) at 100 kHz	1.65	1.09	0.85	1.45
Hysteresis (V)	0.81	0.18	0.04	0.65
D_{it} (cm^{-2}·eV^{-1})	1.02×10^{13}	4.37×10^{12}	2.71×10^{12}	5.33×10^{12}

550 °C, there is a degradation of the C–V characteristic of the sample. XPS indicates the reduction of the amount of As_2O_3 to below the XPS detection level as the PDA temperature reaches 500 °C. The As–As bonding and In oxide amounts were significantly increased at the PDA temperature of 550 °C and above. The lowest interfacial trap density of 2.7×10^{12} eV^{-1} cm^{-2} was obtained for the sample annealed at 500 °C. More studies will be carried out to further improve the MBD HfO_2/n-InAs/InGaAs interfacial quality.

Acknowledgment The authors would like to thank the Ministry of Education and the National Science Council of the Republic of China for supporting this research under contract Nos. 98-2923-E-009-002-MY3 and 100-2120-M-009-010.

1) H. D. Trinh *et al.*: Appl. Phys. Lett. **97** (2010) 042903.
2) H. D. Trinh *et al.*: IEEE Electron Device Lett. **32** (2011) 752.
3) T. D. Lin *et al.*: Appl. Phys. Lett. **93** (2008) 033516.
4) M. M. Frank *et al.*: Appl. Phys. Lett. **86** (2005) 152904.
5) S. Koveshnikov *et al.*: Appl. Phys. Lett. **92** (2008) 222904.
6) Y. Xuan *et al.*: Appl. Phys. Lett. **88** (2006) 263518.
7) C. L. Hinkle *et al.*: Curr. Opin. Solid State Mater. Sci. **15** (2011) 188.
8) S. Oktyabrsky *et al.*: Mater. Sci. Eng. B **135** (2006) 272.
9) I. Ok *et al.*: IEEE Electron Device Lett. **27** (2006) 145.
10) H. Kim *et al.*: Appl. Phys. Lett. **93** (2008) 102906.
11) F. Zhu *et al.*: Appl. Phys. Lett. **94** (2009) 013511.
12) D.-H. Kim and J. A. Alamo: IEEE Electron Device Lett. **29** (2008) 830.
13) C.-I. Kuo *et al.*: Electrochem. Solid-State Lett. **11** (2008) H193.
14) H.-D. Trinh *et al.*: Jpn. J. Appl. Phys. **49** (2010) 111201.
15) D. Wheeler *et al.*: Microelectron. Eng. **86** (2009) 1561.
16) N. Li *et al.*: Appl. Phys. Lett. **92** (2008) 143507.
17) H.-Y. Lin *et al.*: Appl. Phys. Lett. **98** (2011) 123509.
18) E. O'Connor *et al.*: Appl. Phys. Lett. **94** (2009) 102902.
19) H. D. Trinh *et al.*: submitted to IEEE Trans. Electron Devices.
20) H. Kim *et al.*: Appl. Phys. Lett. **82** (2003) 106.
21) S. Mudanai *et al.*: IEEE Electron Device Lett. **23** (2002) 728.
22) T.-H. Moon *et al.*: Microelectron. Eng. **83** (2006) 2452.
23) K. Xiong *et al.*: Appl. Phys. Lett. **87** (2005) 183505.
24) D. K. Schroder: *Semiconductor Material and Device Characterization* (Wiley, New York, 2006).

© 2012 The Japan Society of Applied Physics