Microelectronic Engineering 97 (2012) 16–19

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

C–V characteristics of epitaxial germanium metal–oxide–semiconductor capacitor on GaAs substrate with ALD Al_2O_3 dielectric

Shih Hsuan Tang [a], Chien I. Kuo [a], Hai Dang Trinh [a], Mantu Hudait [b], Edward Yi Chang [a,c,*], Ching Yi Hsu [c], Yung Hsuan Su [a], Guang-Li Luo [d], Hong Quan Nguyen [a]

[a] Department of Materials Science and Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsin-chu 300, Taiwan, ROC

[b] Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, USA

[c] Department of Electronics Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsin-chu 300, Taiwan, ROC

[d] National Nano Device Laboratories, Hsin-chu 300, Taiwan, ROC

ARTICLE INFO

Article history:
Received 17 October 2011
Received in revised form 29 February 2012
Accepted 22 March 2012
Available online 30 March 2012

Keywords:
Ge MOSCAP
CMOS integration
RTO
ALD Al2O3
Ge epitaxial film

ABSTRACT

Epitaxial germanium metal–oxide–semiconductor capacitors (MOSCAP) were fabricated on GaAs substrate using atomic layer deposited Al_2O_3 gate dielectric with surface treatments including pure HF and HF plus rapid thermal oxidation (RTO). The electrical characteristics of 10 nm Al_2O_3/Ge MOSCAP showed p-type behavior with excellent *C–V* responses and low leakage current. Interface state density in the order of 10^{11} eV^{-1} cm^{-2} was determined from the conductance method and the HF plus RTO treatment exhibits better Al_2O_3/Ge interface quality than that of pure HF treatment.

© 2012 Elsevier B.V. All rights reserved.

1. Introduction

Device scaling is a major effort to enhance device performance for silicon industry in recent years. With continued transistor scaling, new materials and device architectures are being introduced at a rapid pace to sustain an aggressive operating voltage scaling roadmap in a persistent effort towards enhancing the energy efficiency of the transistors. Metal–oxide–semiconductor field-effect transistor (MOSFET) based on III–V material has attracted a lot of attention due to their higher carrier mobility compared to that of Si devices, for example, InAs has an electron mobility of more than 20,000 cm^2 V^{-1} s^{-1} [1,2]. However, III–V materials still suffer from lower hole mobility, it is very critical to explore a novel channel material with higher hole mobility that would provide an energy-efficient nanoscale FET for future complementary structures [3]. In general, Ge is a good candidate for p-channel material because of its high hole mobility (1900 cm^2 V^{-1} s^{-1}). Typically, the Ge p-channel devices are usually fabricated on bulk Ge substrate [4,5], however, for post CMOS applications, the growth of Ge on GaAs is a possible solution for materials integration since GaAs material has high resistivity, thus reduce the parasitic effect of the Ge device.

The Ge epitaxial film grown on GaAs is of immense interest due to very low lattice mismatch (~0.08%) which ensures larger critical thickness and lower dislocation density [6]. Furthermore, the Ge film grown on GaAs is anti-phase boundary (APB) free, unlike the growth of GaAs film on Ge where APB is usually detected [7]. Only a few groups have been investigated the growth of Ge film on GaAs by molecular beam epitaxy [8–10]. Due to the advantages of Ge epitaxial film on GaAs substrate as indicated above, recently Ge/GaAs material system has become gained lot of interest for p-channel option [11,12]. The high quality Ge film grown on GaAs substrate with low defect density and smooth surface morphology can be used for the fabrication of the p-channel MOSFET, and thus the p-channel MOSFET can be integrated with n-channel III–V material devices on the same GaAs template for complimentary architecture for beyond-the-CMOS-roadmap logic applications. In this letter, high quality epitaxial Ge film was grown on (100) GaAs wafer using ultrahigh vacuum chemical vapor deposition (UHVCVD). The MOS capacitors were fabricated on Ge film grown on GaAs using atomic layer deposited (ALD) Al_2O_3 as gate dielectric and the capacitance–voltage, conductance measurements were performed to investigate the quality of the gate dielectric on Ge film. The measurement results in this letter clearly evidenced excellent capacitance–voltage characteristics and lower interface

* Corresponding author at: Department of Materials Science and Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsin-chu 300, Taiwan, ROC.
E-mail address: edc@mail.nctu.edu.tw (E.Y. Chang).

0167-9317/$ - see front matter © 2012 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.mee.2012.03.014

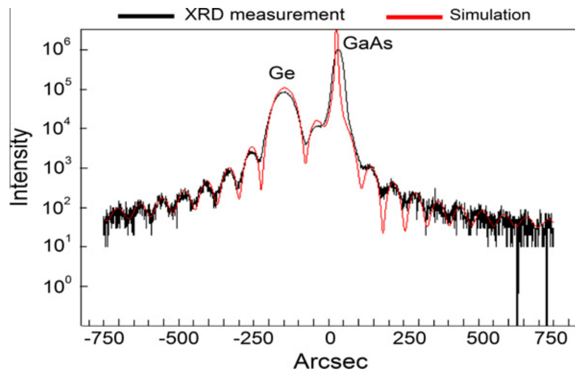

Fig. 1. XRD measurement of 250 nm Ge film on GaAs substrate. The fringes on both sides indicates a sharp Ge/GaAs heterointerface.

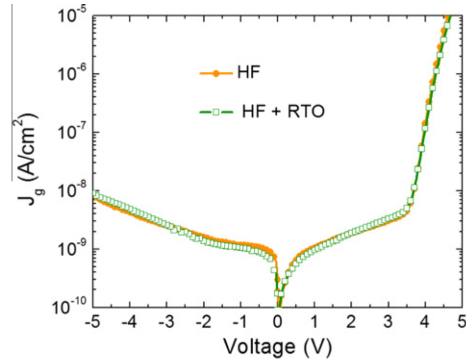

Fig. 3. The current–voltage characteristics of Al_2O_3/Ge/GaAs MOSCAPs.

induced defects achieved from Al_2O_3/epitaxial Ge MOS capacitor structures. This demonstrates the great potential of Ge for p-type transistor applications and thus future integration of beyond-CMOS logic applications.

2. Experimental

In this study, 250 nm high quality Ge epitaxial film was grown on (100) GaAs substrate by UHVCVD system. The metal–oxide–semiconductor capacitor (MOSCAP) was fabricated on the Ge film grown on GaAs using ALD Al_2O_3, and the quality of the interface properties were determined by the interface trapping density (D_{it}) using conductance measurement. Prior to the deposition of Al_2O_3, Ge epitaxial films were surface treated, (i) including HF etching and (ii) HF etching plus rapid thermal oxidation (RTO), to reduce the D_{it} value. Several reports have been demonstrated reduction of interface D_{it} value by introducing GeO_2 interlayer between the high-k and Ge substrate by RTO method [13–15]. In this paper, the material properties and detailed electrical characteristics of the Ge MOSCAP devices are investigated.

Epi-ready (100) GaAs substrates were used for the growth of Ge epitaxial film. The as-received GaAs wafer was loaded into the UHVCVD without any pre-clean. The GaAs substrate was baked for 90 s at ~600 °C. The purpose of the bake is to remove the native oxide (As_2O_3 and Ga_2O_3) on the GaAs surface without arsenic overpressure. The baking time was carefully controlled to prevent the decomposition of GaAs surface [6] followed by GeH_4 flow at a rate of 10 sccm at a fixed pressure of 20 mTorr. The 250 nm Ge epitaxial film was deposited on GaAs substrate at the growth temperature of 600 °C. Prior to fabrication of MOSCAP, the Ge/GaAs wafer was degreased in acetone and isopropanol followed by removal of native oxide using HF (49%): H_2O = 1:100 solution and finally rise with deionized (DI) water. After the HF treatment, one sample went through RTO to grow a thin GeO_2 film prior to the deposition of Al_2O_3. The RTO was performed at 400 °C for 3 min in oxygen atmosphere and 10 nm ALD Al_2O_3 was deposited at 250 °C as the MOSCAP dielectric. Post deposition annealing (PDA) was carried out at 450 °C for 5 min in forming gas [16] followed by e-beam evaporated Pt/Au (500 Å/1000 Å) gate metal and Ti/Au (500 Å/1000 Å) ohmic contact, respectively. Finally, post metal annealing was performed at 250 °C for 30 s in forming gas.

3. Results and discussion

The quality of 250 nm Ge epitaxial film deposited on GaAs at 600 °C was determined by high-resolution X-ray diffraction (HRXRD), as shown in Fig. 1. Fig. 1 shows the experimental (black) and the simulated curve (red line), respectively. The HRXRD result and the simulated curve are in agreement with each other, indicates the closely lattice match Ge epitaxial film grown on GaAs substrate. Moreover, the appearance of the fringes on both sides of Ge and GaAs peaks indicates a very sharp Ge/GaAs heterointerface [11].

The surface morphologies of the samples without and with the deposited Al_2O_3 were measured by tapping mode atomic force microscopy (AFM), as shown in Fig. 2. The root mean square roughness (rms) and the mean surface roughness (Ra) of a bare Ge film were 0.19 and 0.15 nm, and that of Al_2O_3/Ge were 0.21 and 0.16 nm, respectively. It indicates that the surface of these samples were quite smooth even with 10 nm Al_2O_3 film deposited on the

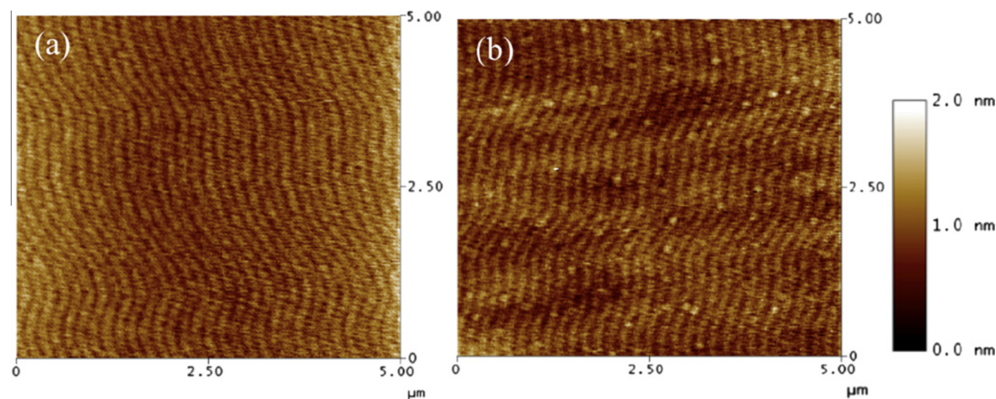

Fig. 2. The AFM measurement of Ge epitaxial film on GaAs substrate: (a) blank Ge epitaxial film and (b) with Al_2O_3 on top of Ge epitaxial layer.

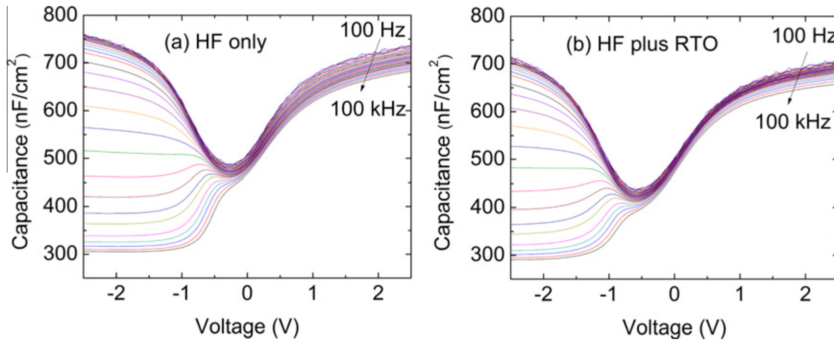

Fig. 4. The capacitance–voltage measurement of Al_2O_3 Ge/GaAs MOSCAPs (a) with HF treatment and (b) with HF plus RTO treatment.

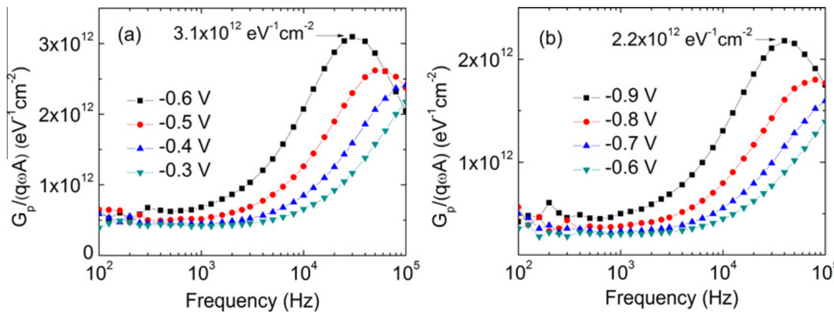

Fig. 5. The $G_p/q\omega A$ versus frequency measurement for Al_2O_3/Ge/GaAs samples (a) with HF treatment (b) with HF plus RTO treatment.

surface of Ge epitaxial film. Additionally, a smooth surface is essential for deeply scaled p-channel devices.

Fig. 3 shows the *I–V* characteristics of MOSCAP samples treated by HF and HF plus RTO process. In the gate bias range of −5 to 3.5 V, leakage current smaller than 10^{-8} A/cm^2 was obtained. The *I–V* characteristics for both samples were very similar; it implied that the Al_2O_3 deposited by ALD had a very good quality and RTO process does not create any surface damage prior to deposition of gate dielectric.

Fig. 4 shows the capacitance–voltage curves of Al_2O_3/Ge/GaAs MOSCAP without and with RTO treatment measured at the frequencies from 100 Hz to 100 kHz. The *C–V* responses show p-type behavior, it represents that the Ge epitaxial layer exhibits n-type doping which is in agreement with the previous study and is related from the arsenic auto-doping effect during the growth of Ge epitaxial film on GaAs [6]. Excellent *C–V* curves with good inversion behaviors were observed for both the samples, and the sample with HF plus RTO treatment shows smaller frequency dispersion in accumulation region and depletion region as compared with the samples with HF treatment.

For high performance MOSFET, the interface quality of the MOS capacitor is very important, and the lower D_{it} is needed. The higher D_{it} value has a significant effect on the transistor performance by increasing the transistor sub-threshold slope, drain-induced barrier lowering, etc. The values of D_{it} of these samples were extracted by conductance method [17]. The relationship between the parallel conductance G_p and D_{it} can be expressed through Eq. (1):

$$D_{it} = 2.5\left(\frac{G_p}{q\omega A}\right)_{max} \quad (1)$$

From Eq. (1) and the $G_p/q\omega A$–f curves at different gate voltages in the depletion region Fig. 5(a) and (b), the D_{it} values estimated at near Ge midgap by conductance method are 7.75×10^{12} and 5.5×10^{12} eV^{-1} cm^{-2} for samples with HF treatment and HF plus RTO treatment samples, respectively. According to the paper reported by Martens et al. [18] with the weak inversion response taken into consideration, the D_{it} estimation by conductance method is usually overestimated. For more accurate estimation of D_{it}, full conductance method needs to be applied and the true values should be one order lower than the above values, i.e. about in the mid 10^{11} eV^{-1} cm^{-2} range for the case of the HF plus RTO sample [18].

4. Summary

In conclusion, high quality, smooth Ge epitaxial film was successfully grown on GaAs substrate. The film exhibits very low *rms* even after 10 nm dielectric oxide Al_2O_3 was deposited on the 250 nm Ge epitaxial layer. The Al_2O_3/Ge/GaAs MOSCAP treated with HF plus RTO showed good inversion behavior with lower D_{it} value. The frequency dispersions in the accumulation and depletion regions were effectively improved and the interface D_{it} was reduced to the order of mid 10^{11} eV^{-1} cm^{-2} range at near the Ge midgap. Thus, Ge epitaxial film with Al_2O_3 gate dielectric shows a great promise for p-channel MOSFET which can be integrated with III–V n-channel MOSFET on the same GaAs template for beyond Si-CMOS logic applications.

Acknowledgment

The authors would like to acknowledge the assistance and support from the National Science Council, Taiwan, ROC, under the contracts: NSC 99-2120-M-009-005.

References

[1] C.I. Kuo, H.T. Hsu, E.Y. Chang, Electrochem. Solid-State Lett. 11 (2008) H193.
[2] Y.C. Lin, H. Yamaguchi, E.Y. Chang, Y.C. Hsieh, M. Ueki, Y. Hirayama, C.Y. Chang, Appl. Phys. Lett. 90 (2007) 023509.
[3] T. Akatsu, C. Deguet, L. Sanchez, F. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Boussagol, V. Loup, F. Mazen, J.M. Hartmann, Y. Campidelli, L.

Clavelier, F. Letertre, N. Kernevez, C. Mazure, Mater. Sci. Semicond. Process. 9 (2006) 444.
[4] Yosuke Nakakita, Ryosho Nakane, Takashi Sasada, Hiroshi Matsubara, Mitsuru Takenaka, Shinichi Takagi, in: IEEE International Electron Devices Meeting, 2008, pp. 1–4.
[5] Keisuke Yamamoto, Ryuji Ueno, Takeshi Yamanaka, Kana Hirayama, Haigui Yang, Dong Wang, Hiroshi Nakashima, Appl. Phys. Exp. 4 (2011) 051301.
[6] S.H. Tang, Edward Y. Chang, M. Hudait, J.S. Maa, C.W. Liu, G.L. Luo, H.D. Trinh, Y.H. Su, Appl. Phys. Lett. 98 (2011) 161905.
[7] G.L. Luo, Y.C. Hsieh, E.Y. Chang, M.H. Pilkuhn, C.H. Chien, T.H. Yang, J. Appl. Phys. 101 (2007) 084501.
[8] X.S. Wang, K.W. Self, W.H. Weinberg, J. Vac. Sci. Technol., A 12 (1994) 1920.
[9] J. Falta, M.C. Reuter, R.M. Tromp, Appl. Phys. Lett. 65 (1994) 1680.
[10] C.B. Ebert, L.A. Eyres, M.M. Fejer, J.S. Harris, J. Cryst. Growth 201 (1999) 187.
[11] M. Zhu, H.C. Chin, G.S. Samudra, Y.C. Yeo, J. Electrochem. Soc. 155 (2008) H76.
[12] Y. Bai, K.E. Lee, C.W. Cheng, M.L. Lee, E.A. Fitzgerald, J. Appl. Phys. 104 (2008) 084518.
[13] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, S. Takagi, Appl. Phys. Lett. 98 (2011) 112902.
[14] A. Delabie, F. Bellenger, M. Houssa, T. Conard, S.V. Elshocht, M. Caymax, M. Heyns, M. Meuris, Appl. Phys. Lett. 91 (2007) 082904.
[15] F. Bellenger, M. Houssa, A. Delabie, V. Afanasiev, T. Conard, M. Caymax, M. Meuris, K. De Meyer, M.M. Heyns, J. Electrochem. Soc. 155 (2008) G33.
[16] H.D. Trinh, E.Y. Chang, P.W. Wu, Y.Y. Wong, C.T. Chang, Y.F. Hsieh, C.C. Yu, H.Q. Nguyen, Y.C. Lin, K.L. Lin, M.K. Hudait, Appl. Phys. Lett. 97 (2010) 042903.
[17] D.K. Schroder, IEEE Trans. Electron Dev. 55 (2008) 547.
[18] K. Martens, C.O. Chui, G. Brammertz, B.D. Jaeger, D. Kuzum, M. Meuris, M.M. Heyns, T. Krishnamohan, K. Saraswat, H.E. Maes, G. Groeseneken, IEEE Trans. Electron Dev. 55 (2008) 547.