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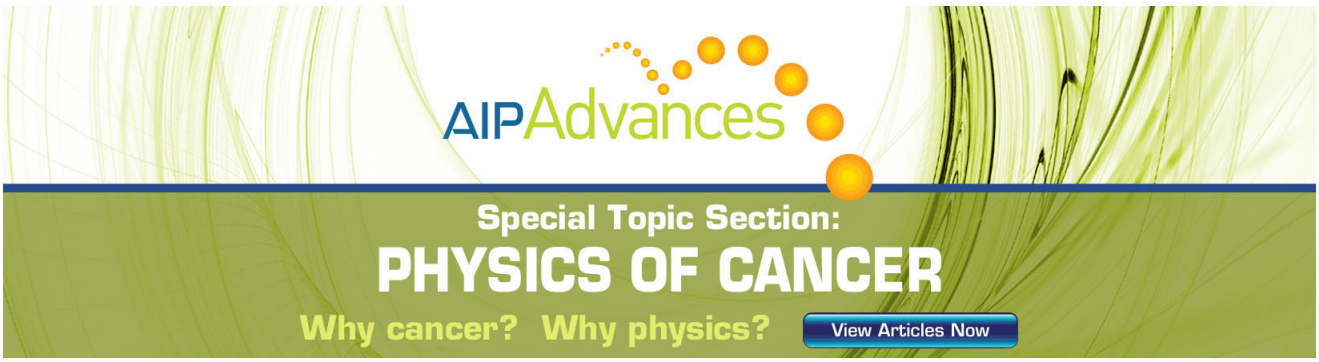

Role of InAs and GaAs terminated heterointerfaces at source/channel on the mixed As-Sb staggered gap tunnel field effect transistor structures grown by molecular beam epitaxy

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The structural, morphological, defect properties, and OFF state leakage current mechanism of mixed As-Sb type-II staggered gap GaAs-like and InAs-like interface heterostructure tunnel field effect transistors (TFETs) grown on InP substrates using linearly graded $In_xAl_{1-x}As$ buffer by molecular beam epitaxy are investigated and compared. Symmetric relaxation of >90% and >75% in the two orthogonal ⟨110⟩ directions with minimal lattice tilt was observed for the terminal $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ active layers of GaAs-like and InAs-like interface TFET structures, respectively, indicating that nearly equal numbers of α and β dislocations were formed during the relaxation process. Atomic force microscopy reveals extremely ordered crosshatch morphology and low root mean square roughness of ~3.17 nm for the InAs-like interface TFET structure compared to the GaAs-like interface TFET structure of ~4.46 nm at the same degree of lattice mismatch with respect to the InP substrates. The GaAs-like interface exhibited higher dislocation density, as observed by cross-sectional transmission electron microscopy, resulting in the elongation of reciprocal lattice point of $In_{0.7}Ga_{0.3}As$ channel and drain layers in the reciprocal space maps, while the InAs-like interface creates a defect-free interface for the pseudomorphic growth of the $In_{0.7}Ga_{0.3}As$ channel and drain layers with minimal elongation along the $\Delta\omega$ direction. The impact of the structural differences between the two interface types on metamorphic TFET devices was demonstrated by comparing p^+-i-n^+ leakage current of identical TFET devices that were fabricated using GaAs-like and InAs-like interface TFET structures. Higher OFF state leakage current dominated by band-to-band tunneling process due to higher degree of defects and dislocations was observed in GaAs-like interface compared to InAs-like interface where type-II staggered band alignment was well maintained. Significantly lower OFF state leakage current dominated by the field enhanced Shockley-Read-Hall generation-recombination process at different temperatures was observed in InAs-like TFET structure. The fixed positive charge at the source/channel heterointerface influences the band lineup substantially with charge density greater than $1 \times 10^{12}/cm^2$ and the band alignment is converted from staggered gap to broken gap at $\sim 6 \times 10^{12}/cm^2$. Clearly, InAs-like interface TFET structure exhibited 4× lower OFF state leakage current, which is attributed primarily to the impact of the layer roughness, defect properties on the carrier recombination rate, suggesting great promise for metamorphic TFET devices for high-performance, and ultra-low power applications. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4737462]

I. INTRODUCTION

Further downscaling of conventional silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) faces critical issues, which result in increased power consumption in integrated circuits. Governed by the transport mechanism relying on thermionic emission of charge carriers over source-channel barrier, the subthreshold swing (SS) is limited to 60 mV/dec at 300 K for these MOSFETs. Reduction of supply voltage (V_{dd}) becomes more challenging due to the exponentially increased in sub-threshold leakage. Together with these effects, higher OFF state leakage (I_{OFF}) and reduced I_{ON}/I_{OFF} ratio are thus expected for sub-65 nm conventional Si MOSFETs. Recently, interband tunneling field-effect-transistors (TFETs)[1–10] based on band-to-band-tunneling (BTBT) injection mechanism different from diffusion over a potential barrier have been proposed and studied in order to reduce SS below the diffusion limit of 60 mV/dec and reduce I_{OFF}. Numerical simulation model of TFET devices using carbon nanotube,[1–3] Ge,[4] Si,[5–7] and III-V[8–10] materials exhibited remarkable higher transistor I_{ON} current and steeper SS. Among these material systems, III-V materials

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are very attractive as they can provide a smaller tunneling mass and allow different band-edge alignment[11,12] for enhancement of transistor ON current[9] and lower OFF state leakage.[13]

III-V heterostructures can reduce the effective bandgap overlap in type-II staggered gap TFETs for further enhancement of ON current. These TFETs have already been predicted to have significant performance enhancement compared with homojunctions by theoretical studies[14,15] as well as recent experimental demonstration.[8,9,16,17] Mixed As-Sb based staggered gap heterojunction enables a wide range of staggered band lineups depending on the material compositions in the source and channel materials.[14] The OFF state leakage current of TFETs is determined by the leakage current of the reverse biased p^+-i-n^+ diode.[18,19] Moreover, defects at the source/channel heterointerface will not only enhance the Shockley-Read-Hall (SRH) generation-recombination (G-R) effect but also increase trap-assisted tunneling or interband tunneling process at OFF state, all of which will lead to increased I_{OFF} and decreased I_{ON}/I_{OFF} ratio. As a result, the quality of the heterointerface at the source/channel region plays a significant role on determining the higher I_{ON} current, lower I_{OFF}, and higher I_{ON}/I_{OFF} ratio of TFET devices. Nevertheless, engineering an abrupt change from Sb rich to As rich heterointerface (As rich to Sb rich) is needed for type-II staggered gap band alignment; otherwise, it can leads to higher defect density and large fixed interface charge density, resulting in higher OFF state leakage current[9,17] and band alignment from staggered to broken gap lineup. The change of group-V fluxes from Sb to As in the mixed anion GaAsSb to mixed cation InGaAs layers introduces an interface intermixing that leads to uncontrolled layer composition at the interface. Moreover, switching from Sb to As, different surface termination will lead to the formation of either GaAs or InAs layer at the GaAsSb/InGaAs interface. Therefore, exploring a proper growth switching sequences at the GaAsSb/InGaAs source/channel heterointerface to reduce defects and investigating the influence of different atomic termination at the source/channel interface on the mixed As-Sb staggered gap tunnel FET structures will provide an important guidance on further boosting performance of TEFT devices, namely, I_{ON}, I_{OFF}, SS, and I_{ON}/I_{OFF} ratio.

In this paper, a comprehensive study was carried out with the role of GaAs and InAs terminated heterointerface (so called GaAs-like and InAs-like interface) at the source and channel region on the structural and electrical transport properties of type-II staggered gap mixed As-Sb based heterostructure TFETs grown by solid source molecular beam epitaxy (MBE). The detailed numerical simulation was performed to explain the OFF state leakage current mechanism of these two TFET devices. Two heterostructure TFETs as shown in Figures 1(a) and 1(b) were grown on semi-insulating (100) InP substrates where the 1-2 monolayers (ML) of gallium (Ga) or indium (In) were added at the source and channel heterointerface, respectively. To accommodate the lattice mismatch between active layers and the InP substrate, 1 μm linearly graded $In_xAl_{1-x}As$ buffer layer was grown with In composition increased from 52% to 70%

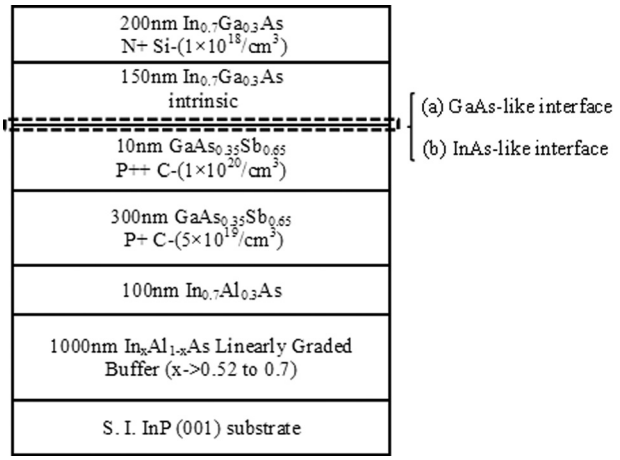

FIG. 1. MBE grown epitaxial n-channel tunnel FET device structures. The dashed box shows two different types of interfaces: (a) GaAs-like interface and (b) InAs-like interface.

and aluminum (Al) composition decreased from 48% to 30% so that the top of the buffer layer composition (i.e., $In_{0.7}Al_{0.3}As$) and the source region $GaAs_{0.35}Sb_{0.65}$ are internally lattice matched. After the deposition of 100 nm $In_{0.7}Al_{0.3}As$ top buffer layer, 300 nm carbon (C) doped p^+ $GaAs_{0.35}Sb_{0.65}$ source layer (C doping of $\sim 5 \times 10^{19}/cm^3$) was deposited. In order to reduce the tunneling width and increase the tunneling electric field and thereby improve the ON current,[20,21] 10 nm p^{++} $GaAs_{0.35}Sb_{0.65}$ layer with C doping of $1 \times 10^{20}/cm^3$ was grown. Two different surface terminations, i.e., (a) GaAs-like and (b) InAs-like were realized when switching from Sb rich GaAsSb to As rich InGaAs layer. For the latter case, 1-2 ML of In was added prior to the growth of $In_{0.7}Ga_{0.3}As$ layer when the As flux was ramping up from 35% to 100%. Finally, 150 nm intrinsic $In_{0.7}Ga_{0.3}As$ channel layer and 200 nm n^+ $In_{0.7}Ga_{0.3}As$ (Si doping of $\sim 1 \times 10^{18}/cm^3$) drain layer were grown to complete the entire TFET device structure. The TFET devices were fabricated from these two structures to validate the role of the two interface termination on the OFF state leakage current. The experimental results were explained using detailed theoretical modeling and observed that InAs-like interface exhibited superior structural and electrical transport properties.

II. EXPERIMENTAL DETAILS

A. Structural characterization and strain relaxation properties

The strain relaxation, surface morphology, and defect properties of TFET structures were characterized using double axis x-ray diffraction (XRD), atomic force microscopy (AFM), and cross-sectional transmission electron microscopy (TEM). TEM samples were prepared using conventional mechanical thinning procedure followed by Ar^+ ion milling. Reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu Kα1 line x-ray source.

For diamond and zinc-blende semiconductors, formation of 60° a/2⟨110⟩ {111} misfit dislocations (MDs) at the

film/substrate interfaces is the primary mechanism to relax misfit strain[22] and the lattice mismatch between the substrate and the mismatch epilayer can be accommodated by dislocation glide. Asymmetric dislocation distribution would result in different in-plane lattice constants along the two orthogonal [110] and [1$\bar{1}$0] dislocation directions. As a result, the projection of the incident x-ray beam was aligned with each of the in-plane ⟨110⟩ directions to measure the anisotropy in strain relaxation of these two TFET structures. Both symmetric (004) and asymmetric (115) RSMs were recorded to determine the alloy composition, the lattice mismatch, and the strain relaxation properties. In-plane lattice constant, a, and out-of-plane lattice constant, c, can be determined using Bragg's law from asymmetric and symmetric RSMs, respectively. The relaxed layer lattice constant, a_r, and the strain, ε, of each layer with respect to the substrate can be calculated using[23,24]

$$a_r = \frac{2v}{1+v}a + \frac{1-v}{1+v}c, \tag{1}$$

$$\varepsilon = \frac{a_r - a_s}{a_s}, \tag{2}$$

where a_s is the lattice constant of the substrate and υ is the Poisson's ratio of each ternary layer calculated from the elastic constants of InAs, AlAs, GaAs, and GaSb using Vegard's law. From RSMs with different incident x-ray beam directions, a_r and ε along [110] and [1$\bar{1}$0] directions can be determined. Relaxation of each layer with respect to the substrate in each ⟨110⟩ direction can also be expressed as

$$R_{[110]} = \frac{a_{[110]} - a_s}{c_{[110]} - a_s} \text{ and } R_{[1\bar{1}0]} = \frac{a_{[1\bar{1}0]} - a_s}{c_{[1\bar{1}0]} - a_s}. \tag{3}$$

For isotropic relaxation, $R_{[110]} = R_{[1\bar{1}0]}$ and the average relaxation is $\bar{R} = (R_{[110]} + R_{[1\bar{1}0]})/2$. The perpendicular lattice mismatch of epilayer with respect to the "virtual" substrate is[25]

$$f_\perp = \frac{c - a_0}{a_0}, \tag{4}$$

where a_0 is the relaxed lattice constant of "virtual" substrate. Similarly, the parallel lattice mismatch measured along the [110] and [1 $\bar{1}$ 0] directions are

$$f_{\parallel[110]} = \frac{a[110] - a_0}{a_0}; \quad f_{\parallel[1\bar{1}0]} = \frac{a[1\bar{1}0] - a_0}{a_0}, \tag{5}$$

where $a_{[110]}$ and $a_{[1\bar{1}0]}$ are in-plane lattice constants of epilayer along [110] and [1$\bar{1}$0] directions, receptively. For the fully relaxed case, the lattice mismatch f_r for fully relaxed layer is described as[22]

$$f_r = \frac{1-v}{1+v}f_\perp + \frac{v}{1+v}(f_{\parallel[110]} + f_{\parallel[1\bar{1}0]}). \tag{6}$$

The critical thickness, h_c, for the formation of misfit dislocations due to the strain relaxation can be estimated using the theoretical expression proposed by Matthews and Blakeslee:[26]

$$h_c = \frac{b}{2\pi f_r}\frac{(1 - v\cos^2\alpha)}{(1+v)\cos\lambda}\left(\ln\frac{h_c}{b} + 1\right), \tag{7}$$

where $b = |\boldsymbol{b}|$ is the magnitude of the dislocation Burgers vector **b**, α is the angle between the dislocation line and its Burgers vector, and β is the angle between the slip direction and the direction in the film plane which is perpendicular to the line of intersection of the slip plane and the interface. Here, Burgers vectors of the dislocations were $\frac{1}{2}$a⟨110⟩ type and were inclined at 45° to (001) such that $b = |\boldsymbol{b}| = \frac{a_r}{\sqrt{2}}$.[27] For 60°a/2 ⟨110⟩ {111} slip system, $\cos\alpha = \cos\beta = 1/2$.[26]

The strain relaxation properties of epitaxial layers can be represented from RSMs relating to **q** vectors. In RSMs, the vector **q** represents the deviation between the reciprocal lattice points (RLPs) of the substrate and epilayers. There are two components involve in **q** vector, q_x and q_z, which corresponds to the angular splitting ω and 2θ, respectively, in real space. Reciprocal lattice points in RSMs might have different q_x and q_z positions depending on different relaxation degree and misorientation, corresponding to a fully strained (pseudomorphic) and a partially relaxed layer, or a fully relaxed (metamorphic) layer.[28] For a (115) asymmetric RSM of an ideal, fully relaxed epitaxial layer without tilt, the diffracted intensity from this layer is expected to fall on the fully relaxed line joining the (115) RLP of the substrate and having a 15.8° angle between the (001) and (115) directions. In contrary, a fully strained layer is expected to follow the fully strained line that joins the (115) RLP of the substrate and along the (001) direction.

B. Processing of self-aligned gate staggered heterojunction TFETs

In order to determine the influence of InAs-like and GaAs-like heterointerfaces at the source/channel region to the leakage current of TFETs, self-aligned metal gate TFET devices were fabricated using two different structures as shown in Figure 1. The detailed TFET process flow can be found elsewhere.[9,29] The 250 nm thick molybdenum (Mo) was deposited on the n^+ $In_{0.7}Ga_{0.3}As$ layer and Cr/Ti dry etch masks were created on the top of Mo. A nano-pillar was formed after the dry etch of Mo and $In_{0.7}Ga_{0.3}As$ layer. Wet etch process was performed to remove sidewall damage and create undercut. An undercut of about 50 nm was obtained and it was ready for the formation of self-aligned gate. Here, the "self-aligned" referred to the isolation of the top contact and the side wall gate as a result of wet etch undercut of the nano-pillar.[9] For the high-k gate dielectric, 1 nm Al_2O_3/3.5 nm HfO_2 was deposited using atomic layer deposition at 250 °C. After the deposition of gate, source and drain metals, the entire structure was planarized with benzocyclobutene (BCB) for device isolation. A 3D schematic diagram of such fabricated nano-pillar device is shown in Figure 2(a) and the corresponding tilted view scanning electron microscopy (SEM) micrograph (without drain pad) is shown in Figure 2(b).

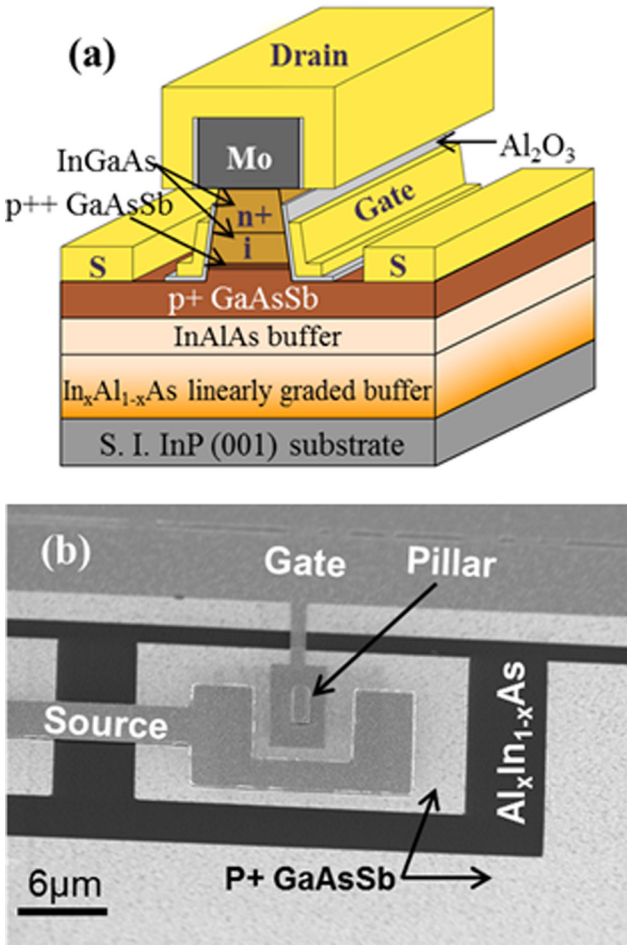

FIG. 2. (a) Schematic of self-aligned gate nano-pillar staggered heterojunction TFET and (b) tilted view SEM micrograph of the TFET device. The drain pad is not shown in this figure.

III. RESULTS AND DISCUSSION

A. Structural properties

1. Certification of layers corresponding to different x-ray peaks

According to the epilayer structures as shown in Figures 1(a) and 1(b), the $In_{0.7}Al_{0.3}As$ uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer, the $GaAs_{0.35}Sb_{0.65}$ source layer, and the $In_{0.7}Ga_{0.3}As$ channel and drain layers were designed to be internally lattice matched. As a result, the RLPs of each layer would appear at the same peak position in the RSM of these TFET structures. However, due to residual strain[30] present in these layers, heavily C doping caused lattice contraction[31] and compositional fluctuation during MBE growth,[28] two distinct RLPs along with InP substrate were found in the RSMs of GaAs-like interface structure (as shown in Figures 5 and 6) and three RLPs in the RSMs of InAs-like interface structure (as shown in Figures 8 and 9), respectively. In order to certificate each layer RLP, wet chemical etching was performed to selectively remove epilayer one from other epilayers of these structures. Symmetric (004) RSMs were recorded to assign the RLP of each layer in these TFET structures. Citric acid/hydrogen peroxide ($C_6H_8O_7$:H_2O_2) at volume ratios of 20:1 and 5:1 were used to selectively etch $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, respectively. All wet etch experiments were carried out at room temperature. Anhydrous citric acid crystals were dissolved in deionized water (DI H_2O) at the ratio of 1 g $C_6H_8O_7$:1 ml H_2O. The solution was kept more than 12 h prior to wet etch process of TFET structures to ensure complete dissolution and room temperature stability. About 15 min before the wet etch experiment, the above mixed liquid solution (considered as one part of $C_6H_8O_7$) was mixed with 30% hydrogen peroxide (H_2O_2) at the desired volume ratio (x parts $C_6H_8O_7$ to 1 part H_2O_2 by volume).[32] From our measurements, the etch rate for $In_{0.7}Ga_{0.3}As$ using $C_6H_8O_7$:H_2O_2 at volume ratio of 20:1 was ~48 nm/min and the selectivity between $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers was found to be ~50.[32,33] The InAs-like interface TFET structure was etched for 10 min to ensure that the $In_{0.7}Ga_{0.3}As$ top layer was completely removed. After symmetric (004) RSM measurement of this etched TFET sample, the same structure was further etched using $C_6H_8O_7$:H_2O_2 at volume ratio of 5:1 for 2 h to remove most of the $GaAs_{0.35}Sb_{0.65}$ layer. The symmetric (004) RSM was performed once again to determine the change of diffraction patterns and assignment of layer peaks. With these measurement results, each layer RLP was precisely assigned. Figure 3 shows (004) RSMs of InAs-like interface TFET structure (a) before wet etching, (b) etched with $C_6H_8O_7$:H_2O_2 at volume ratio of 20:1 for 10 min, and (c) etched with $C_6H_8O_7$:H_2O_2 at volume ratio of 5:1 for another 2 h. All the peak positions and materials composition were labeled in this figure. Similarly, wet etch process was performed on the GaAs-like TFET structure and Figure 4 shows the symmetric (004) RSMs of this structure. Unlike InAs-like interface structure, $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers were merged together due to higher degree of strain relaxation of the $In_{0.7}Ga_{0.3}As$ layer. As a result of removing the top $In_{0.7}Ga_{0.3}As$ cap layer, the RLP position of the remaining $GaAs_{0.35}Sb_{0.65}$ layer was shifted compared with the combined contour of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ prior to wet etching. The detailed strain relaxation analysis of these two layers can be found in Sec. III A 3 of this paper.

2. Lattice contraction due to heavy C doping in $GaAs_{0.35}Sb_{0.65}$

In order to understand the impact of the heavy C doping in the $GaAs_{0.35}Sb_{0.65}$ source layer on the lattice constant, the

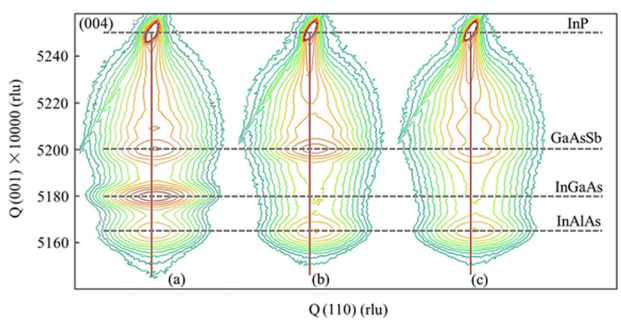

FIG. 3. Symmetric (004) RSMs of InAs-like interface TFET structure: (a) before etching, (b) $In_{0.7}Ga_{0.3}As$ channel and drain layers were etched with $C_6H_8O_7$:H_2O_2 at volume ratio of 20:1 for 10 min, and (c) $GaAs_{0.35}Sb_{0.65}$ was etched with $C_6H_8O_7$:H_2O_2 at volume ratio of 5:1 for another 2 h. Selective wet etch process clearly distinguished each epilayer peak corresponding to reciprocal lattice point of each layer as indicated in this figure.

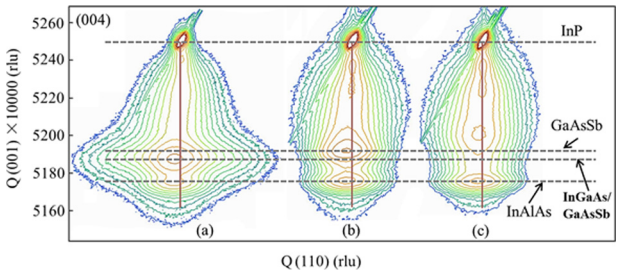

FIG. 4. Symmetric (004) RSMs of GaAs-like interface TFET structure: (a) before etching, (b) $In_{0.7}Ga_{0.3}As$ channel and drain layers were etched with $C_6H_8O_7$:H_2O_2 at volume ratio of 20:1 for 10 min, and (c) $GaAs_{0.35}Sb_{0.65}$ was etched with $C_6H_8O_7$:H_2O_2 at volume ratio of 5:1 for another 2 h. Selective wet etch process clearly distinguished each epilayer peak corresponding to reciprocal lattice point of each layer as indicated in this figure.

estimation of the lattice constant change due to doping and hence the lattice mismatched to the $In_{0.7}Ga_{0.3}As$ layer was performed. If the C atoms change the lattice constant in the material, measures must be taken in the active region design

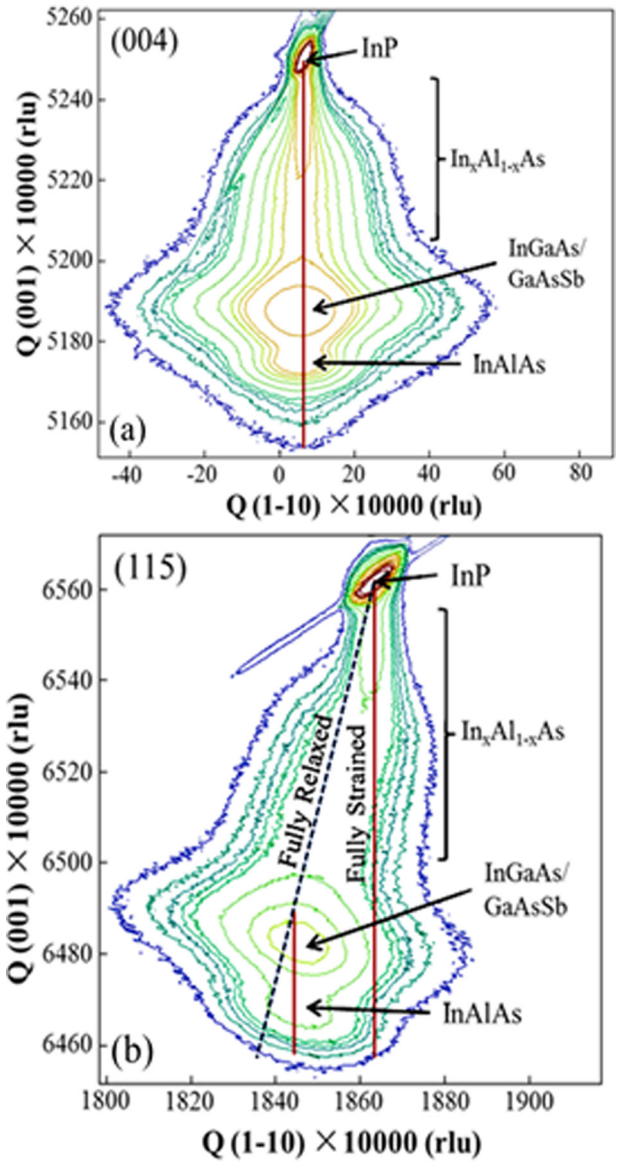

FIG. 5. (a) Symmetric (004) and (b) asymmetric (115) RSMs of GaAs-like interface TFET structure using an incident beam along [1$\bar{1}$0] direction.

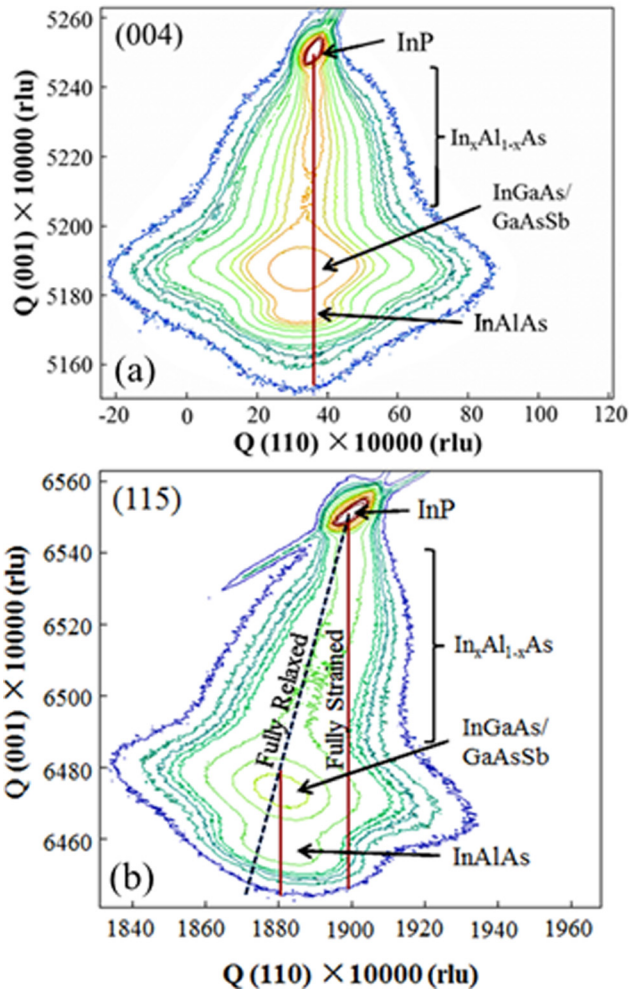

FIG. 6. (a) Symmetric (004) and (b) asymmetric (115) RSMs of GaAs-like interface TFET structure using an incident beam along [110] direction.

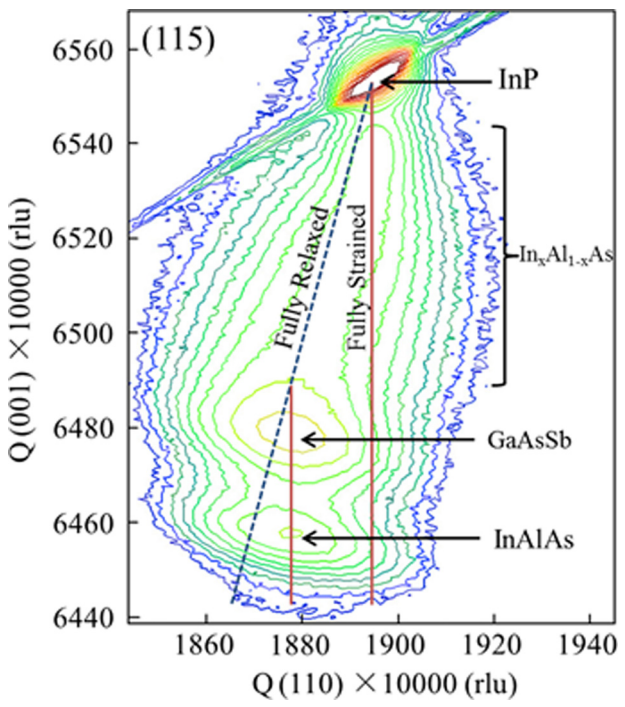

FIG. 7. Asymmetric (115) RSM of GaAs-like interface TFET structure after wet etching with $C_6H_8O_7$:H_2O_2 at volume ratio of 20:1 for 10 min.

such that the active layer should always be internally lattice matched in these mixed As and Sb based TFET structures. It has been well established that for C doped III-V materials beyond the doping level of $1 \times 10^{19}/\text{cm}^3$, substitutional carbon causes the III-V host lattice to contract due to its small tetrahedral covalent radius (0.77 Å). Lattice mismatch due to lattice contraction by heavily doped C atom has already been reported and calculated in GaAs,[34,35] GaSb,[36] InGaAs,[37] and AlGaAs[35] material systems. In our case, similar lattice contraction in $GaAs_{0.35}Sb_{0.65}$ was also observed at the doping level of $5 \times 10^{19}/\text{cm}^3$. As no evidence shows that carbon behaves as a donor at this doping level,[35] the resulting mismatch due to lattice contraction can be estimated by[37]

$$|f_\perp| = \left|\frac{c - a_0}{a_0}\right| = \frac{1+v}{1-v}\,\frac{4}{\sqrt{3}a_i}\left\{\frac{[(r_c - r_{As})N_c]y}{N_{0(As)}} + \frac{[(r_c - r_{Sb})N_c](1-y)}{N_{0(Sb)}}\right\}, \tag{8}$$

where c is the perpendicular lattice constant of heavily C doped $GaAs_ySb_{1-y}$ layer, a_0 is the undoped lattice constant of

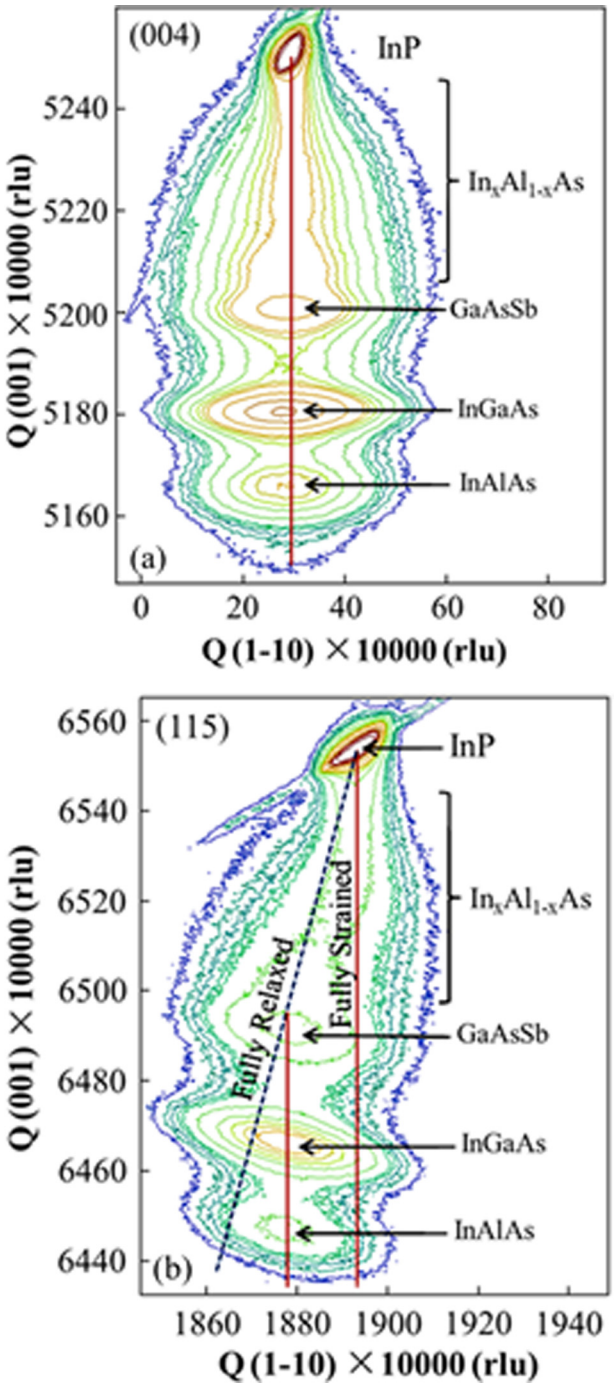

FIG. 8. (a) Symmetric (004) and (b) asymmetric (115) RSMs of InAs-like interface TFET structure using an incident beam along [1$\bar{1}$0] direction.

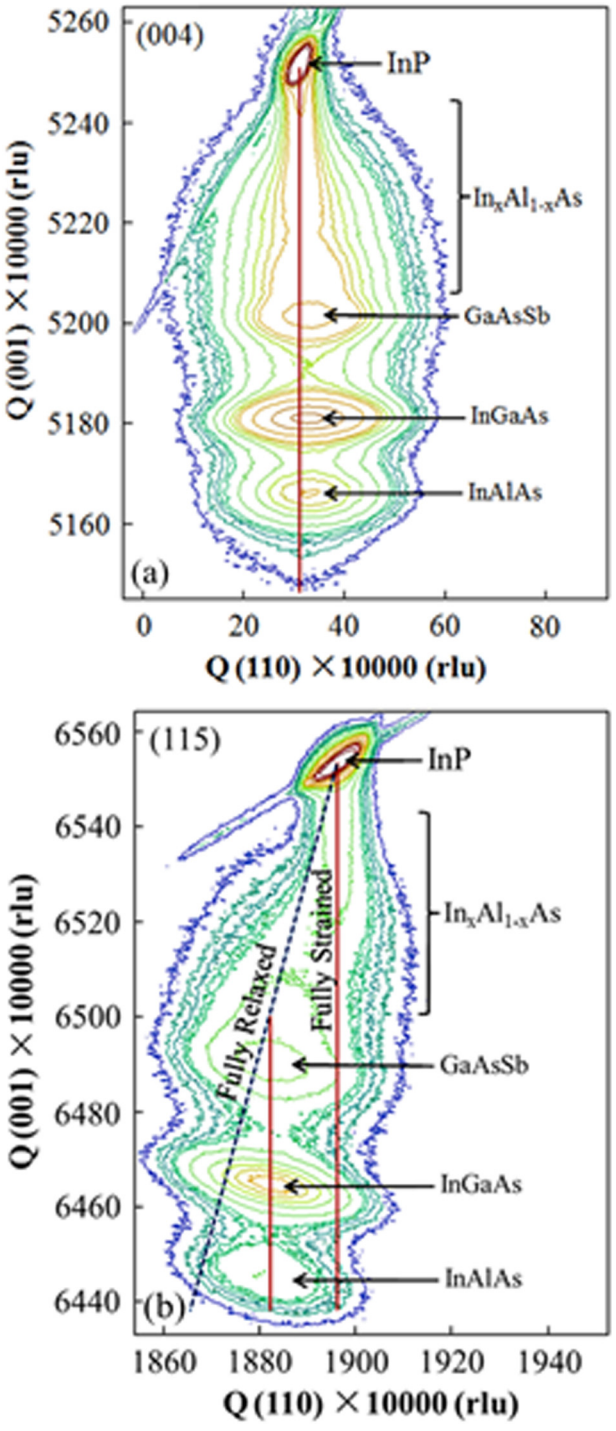

FIG. 9. (a) Symmetric (004) and (b) asymmetric (115) RSMs of InAs-like interface TFET structure using an incident beam along [110] direction.

the same material (here the relaxed lattice constant of lattice matched InGaAs was used for a_o), and r_c (0.77 Å), r_{As} (1.19 Å), and r_{Sb} (1.38 Å) are the covalent radius of C, As, and Sb, respectively. $N_c \approx 5 \times 10^{19}/\text{cm}^3$ is the concentration of substitutional C atoms, $v = 0.31$ is the Poisson ratio of GaAs and GaSb, $N_{0(As)} = 2.21 \times 10^{22}/\text{cm}^3$ is the number of As atoms per cm^3 in GaAs at 300 K, $N_{0(Sb)} = 1.77 \times 10^{22}/\text{cm}^3$ is the number of Sb atoms per cm^3 in GaSb at 300 K, and y = 0.35 is the composition of As in $GaAs_ySb_{1-y}$. From Eq. (8) and using the above listed materials parameter, the calculated lattice mismatch was found to be 1.11×10^{-3}.

In order to quantify the lattice mismatch of this $GaAs_{0.35}Sb_{0.65}$ layer from the measured RSMs, as shown in Figures 8 and 9, the perpendicular lattice constant of $GaAs_{0.35}Sb_{0.65}$ and the relaxed lattice constant of $In_{0.7}Ga_{0.3}As$ were measured. Using these lattice constant parameters and Eq. (4), the lattice mismatch was determined. As the $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ peaks merged together in GaAs-like interface TFET structure, the InAs-like interface TFET structure was used to evaluate the lattice mismatch due to C doping in $GaAs_{0.35}Sb_{0.65}$. Using Eq. (4), the lattice mismatch of heavily C doped $GaAs_{0.35}Sb_{0.65}$ layer respect to its lattice matched $In_{0.7}Ga_{0.3}As$ layer of InAs-like interface TFET structure along $[1\bar{1}0]$ and [110] directions was found to be $\sim 1.16 \times 10^{-3}$ and 1.28×10^{-3}, respectively. Thus, the measured values of lattice mismatch due to heavily C doped $GaAs_{0.35}Sb_{0.65}$ layer were symmetric along the two orthogonal $\langle 110 \rangle$ directions and were in excellently agreement with the estimated lattice mismatch determined from the Eq. (8). The lattice parameter, mismatch, composition, and relaxation were summarized in Table I. Therefore, the Sb composition in the $GaAs_{0.35}Sb_{0.65}$ layer and the C-doping should be well controlled such that the upper $In_{0.7}Ga_{0.3}As$ layer is lattice matched during the MBE growth of mixed As and Sb based type-II staggered gap tunnel FET structures.

3. Strain relaxation properties

a. GaAs-like interface TFET structure. Once the peak positions were assigned as described in Sec. III A 1, the relaxation state and residual strain of epilayers were obtained from symmetric (004) and asymmetric (115) reflections of RSMs. RSMs of the GaAs-like interface TFET structure with incident beam along $[1\bar{1}0]$ and [110] directions are shown in Figures 5 and 6, respectively. From RSMs, the lattice constant in the growth plane, a (from the asymmetric reflection), and the lattice constant in the out-of-plane (growth direction), c (from the symmetric reflection), can be determined in both orthogonal $\langle 110 \rangle$ directions. The relaxed lattice constant can be calculated from these measured parameters using Eq. (1). One can find from these figures that there are three distinct RLP maxima corresponds to (i) the InP substrate, (ii) 350 nm $GaAs_{0.35}Sb_{0.65}$ and 450 nm $In_{0.7}Ga_{0.3}As$ layers, and (iii) 100 nm $In_{0.7}Al_{0.3}As$ uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer. The composition of each ternary $GaAs_ySb_{1-y}$, $In_xGa_{1-x}As$, and $In_xAl_{1-x}As$ alloy was calculated by Vegard's Law using the calculated relaxed layer lattice constant and the lattice constant of each binary alloy. The in-plane and out-of-plane lattice constants, relaxed lattice constants, strain relaxation, residual strain, and alloy composition of each epilayer with the projection of x-ray beam along both $[1\bar{1}0]$ and [110] directions were also summarized in Table I. The relaxation state of the upper part of the linearly graded $In_xAl_{1-x}As$ buffer has a significant role for the internally lattice mismatched active layer in As and Sb based TFET structures. From both (004) and (115) RSMs, the strain relaxation value of the uppermost $In_{0.7}Al_{0.3}As$ layer of the linearly graded buffer with respect to InP substrate was found to be 70% along the $[1\bar{1}0]$ direction and 69% along the [110] direction, which corresponds to a misfit strain of 1.14% and 1.15%, respectively. The strain relaxation value obtained from our measurement of the uppermost $In_{0.7}Al_{0.3}As$ layer is consistent with the results obtained by other researchers on the uppermost layer of linear graded $In_xAl_{1-x}As$ buffer.[30,38]

There are two types of dislocations exist in III-V compound semiconductors during strain relaxation process. Those related to group-III atoms at their core and belonging to the shuffle set are known as α dislocation, while those shuffle set dislocations with group-V atoms at their core are known as β type. In compressively strained III-V layer, an α type dislocation lies in the $[1\bar{1}0]$ direction.[39] Similarly, a β type dislocation lies in the [110] direction to relieve compressive strain in the epilayer.[39] As a result, for strain

TABLE I. Summary of InAs-like and GaAs-like interfaces TEFT structures with incident x-ray beam along $[1\bar{1}0]$ and [110] directions.

Sample	Incident beam direction	Layers	Lattice constant (Å) c	a	a_r	Composition	Relaxation (%)	Tilt (arc sec)	Strain (%)
(a) GaAs-like interface	$[1\bar{1}0]$	InGaAs/GaAsSb	5.9401	5.9322	5.9361	In: 70% Sb: 65%	94	−37	1.15
		InAlAs	5.9538	5.9180	5.9359	In: 70%	73	−43	1.14
	[110]	InGaAs/GaAsSb	5.9400	5.9284	5.9342	In: 69% Sb: 64%	91	−145	1.11
		InAlAs	5.9537	5.9182	5.9360	In: 69%	74	−164	1.15
(b) InAs-like interface	$[1\bar{1}0]$	GaAsSb	5.9249	5.9064	5.9157	Sb: 64%	80	−19	0.80
		InGaAs	5.9481	5.9159	5.9318	In: 69%	75	−43	1.08
		InAlAs	5.9651	5.9235	5.9443	In: 71%	72	−44	1.29
	[110]	GaAsSb	5.9247	5.9065	5.9156	Sb: 64%	81	95	0.80
		InGaAs	5.9481	5.9168	5.9323	In: 69%	76	78	1.08
		InAlAs	5.9655	5.9235	5.9445	In: 71%	72	95	1.29

relaxation by misfit component of 60° dislocations, relaxation along the [1$\bar{1}$0] direction is controlled by the nucleation and glide of β dislocations and relaxation along the [110] direction is controlled by the nucleation and glide of α dislocations, respectively. It is well established that the formation kinetics of these two types of dislocations are different, which leads to observed asymmetric strain relaxation along both ⟨110⟩ directions.[39] However, from our study on these TFET structures, the strain relaxation value extracted along [1$\bar{1}$0] direction of $In_{0.7}Al_{0.3}As$, $GaAs_{0.35}Sb_{0.65}$, or $In_{0.7}Ga_{0.3}As$ layers is similar to that extracted from [110] direction. The symmetric strain relaxation of each layer along [110] and [1$\bar{1}$0] directions is in agreement with the results from mixed anion step graded InAsP buffer[23] and mixed cation linearly graded InAlAs[38] buffer materials. The symmetric relaxation in these layers indicates that the total length of misfit dislocation in each ⟨110⟩ direction is approximately the same. Moreover, the lattice tilt amplitude of less than 200 arc sec was observed from the symmetric (004) RSMs indicates nearly equal amounts of α and β dislocations participated during the relaxation process, supporting the observed symmetric strain relaxation of the linearly graded $In_xAl_{1-x}As$ buffer layer, $GaAs_{0.35}Sb_{0.65}$, and $In_{0.7}Ga_{0.3}$ As layers.

As shown in Figures 5 and 6, the contour of $In_{0.7}Ga_{0.3}As$ channel/drain layer was merged with the heavily C doped $GaAs_{0.35}Sb_{0.65}$ source layer, with the incident beam along both [110] and [1$\bar{1}$0] directions. In Figures 5(a) and 5(b), the measured lattice constants along the out-of-plane and in-plane directions of these two layers were found to be 5.9401 Å and 5.9322 Å, respectively, with the projection of the beam oriented along [1$\bar{1}$0] direction, corresponding to the relaxed lattice constant of 5.9361 Å. Similarly, the lattice parameters along the out-of-plane and in-plane directions of these two layers were 5.9400 Å and 5.9284 Å, respectively, with the projection of the beam oriented along the [110] direction using Figures 6(a) and 6(b), corresponding to the relaxed lattice constant of 5.9342 Å. From the asymmetric (115) RSMs of the GaAs-like interface TFET structure as shown in Figures 5(b) and 6(b), the RLP of $GaAs_{0.35}Sb_{0.65}$/$In_{0.7}Ga_{0.3}As$ layers followed the fully relaxed line (the blue dashed line), indicated nearly full relaxation of these two layers with respect to InP substrate. The percentage of strain relaxation of these two layers was found to be 94% and 91%, respectively, in [1$\bar{1}$0] and [110] directions, within the relative experimental error, indicating symmetric relaxation.

There are two reasons that can lead the two contours of $GaAs_{0.35}Sb_{0.65}$ layer and $In_{0.7}Ga_{0.3}As$ layer in GaAs-like TFET structure to merge together: (1) they have internally lattice matched to each other, or (2) high dislocation density at the heterointerface of $GaAs_{0.35}Sb_{0.65}$/$In_{0.7}Ga_{0.3}As$ caused large strain relaxation. It has been observed from RSMs that the high dislocation density contributes to the combination of these two peaks, supported by the elongation of contours along the x-axis of RSMs in Figures 5 and 6. It is well-known that misfit dislocations can cause variation in the orientation of the lattice planes, which is known as mosaic structures, resulting in diffuse scattering of x rays in the ⟨110⟩ directions. Misfit dislocations in the [1$\bar{1}$0] direction lead to the elongation of the constant intensity contours when the incident beam is aligned in the [110] direction, denoted by $\Delta q_{[110]}$ and similarly, misfit dislocations with [110] direction cause the elongation of constant intensity contours in the [1$\bar{1}$0] direction, denoted by $\Delta q_{[1\bar{1}0]}$. As a result, the elongation of contour in RSMs in a given ⟨110⟩ direction is a measure of the mosaicity caused by misfit dislocations in its orthogonal ⟨110⟩ direction.[39] From Figures 5 and 6, the elongation of the combined $GaAs_{0.35}Sb_{0.65}$/$In_{0.7}Ga_{0.3}As$ contour was found from both [1$\bar{1}$0] and [110] directions, which indicates high misfit dislocation density in the two orthogonal ⟨110⟩ directions in this GaAs-like TFET structure. The symmetric elongation in these two ⟨110⟩ directions also indicates that almost equal numbers of α and β dislocations were formed during the relaxation process. In fact, the symmetric relaxation can also be supported by the smaller tilt amplitude of <200 arc sec. In order to distinguish whether the large strain relaxation caused by higher misfit dislocation density formed at the $GaAs_{0.35}Sb_{0.65}$/$In_{0.7}Ga_{0.3}As$ heterointerface or one of the layer is impacted by severe dislocations due to lattice mismatched, the top $In_{0.7}Ga_{0.3}As$ layer was etched and both symmetric (004) and asymmetric (115) RSM measurements were performed on the etched GaAs-like TFET structure. The measured (004) and (115) RSMs with the incident x-ray beam along [110] directions are shown in Figures 3(b) and 7, respectively. By comparing Figure 3(b) with Figure 3(a), it was found that the elongation of contour is highly enfeebled after removing the top $In_{0.7}Ga_{0.3}As$ layer, which indicates that the $GaAs_{0.35}Sb_{0.65}$ layer is not as defective as the $In_{0.7}Ga_{0.3}As$ layer and the higher dislocation density is only confined within top $In_{0.7}Ga_{0.3}As$ layer. In fact, the RLP of $GaAs_{0.35}Sb_{0.65}$ layer is masked by the $In_{0.7}Ga_{0.3}As$ layer. Furthermore, by comparing Figure 3(a) with Figure 3(b) and Figure 6(b) with Figure 7, it was found that the position of RLP from $GaAs_{0.35}Sb_{0.65}$ layer shifted in both (004) symmetric and (115) asymmetric RSMs in contrast with the combined RLP positions prior to etching the top $In_{0.7}Ga_{0.3}As$ layer. It indicates that the strain relaxation of $GaAs_{0.35}Sb_{0.65}$ layer is different from $In_{0.7}Ga_{0.3}As$ layer in the GaAs-like interface TFET structure. Using Figures 3(b) and 7, the amount of strain relaxation of $GaAs_{0.35}Sb_{0.65}$ layer was analyzed along the [110] direction. The lattice parameters along the out-of-plane and in-plane directions of the $GaAs_{0.35}Sb_{0.65}$ layer were found to be 5.9373 Å and 5.9141 Å, respectively. The degree of relaxation of this layer was 80% with respect to the InP substrate, which is lower than the combined RLP of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers (i.e., 94% along [1$\bar{1}$0] direction and 91% along [110] direction).

The higher degree of strain relaxation of the top $In_{0.7}Ga_{0.3}As$ layer can be formed in two ways: (1) misfit dislocations were generated when a critical thickness was reached, and (2) threading dislocations started at the interface of $GaAs_{0.35}Sb_{0.65}$/$In_{0.7}Ga_{0.3}As$ to relieve strain. However, from Eq. (7) and using the lattice mismatch calculated from Sec. III A 2, the critical layer thickness for the formation of misfit dislocations in $In_{0.7}Ga_{0.3}As$ layer is several micrometers, which is more than the thickness of the $In_{0.7}Ga_{0.3}As$ channel/drain layer. Therefore, it is reasonable

to assume that the GaAs-terminated interface contributes high dislocation density in the $In_{0.7}Ga_{0.3}As$ layer due to the formation of unwanted GaAs layer at the $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ heterointerfaces and this higher dislocation density leads to the higher degree of strain relaxation of the $In_{0.7}Ga_{0.3}As$ layer.

b. InAs-like interface TFET structure. A similar analysis was performed on the InAs-like interface TFET structure. Figures 8 and 9 show RSMs for (004) and (115) reflections obtained from the structure, with the projection of incident beam along $[1\bar{1}0]$ and [110] directions, respectively. One can find from these figures that in each RSM, four RLPs are well resolved. From the analysis of Sec. III A 1, the peak assignments corresponding to those RLP maxima are from (1) the InP substrate, (2) $GaAs_{0.35}Sb_{0.65}$ source layer, (3) $In_{0.7}Ga_{0.3}As$ channel/drain layer, and (4) the $In_{0.7}Al_{0.3}As$ uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer. The uppermost $In_{0.7}Al_{0.3}As$ layer of the linearly graded buffer showed similar amount of relaxation as the one in GaAs-like interface TFET structure. Using the lattice parameters extracted from the RSMs shown in Figures 8 and 9 with the alignment of incident beam along $[1\bar{1}0]$ and [110] directions, the relaxation of the final $In_{0.7}Al_{0.3}As$ uppermost buffer layer was calculated to be 72% in both directions. The corresponding measured lattice constants along out-of-plane and in-plane directions of the $In_{0.7}Al_{0.3}As$ upper most buffer layer were summarized in Table I. Symmetric relaxation along two orthogonal $\langle 110 \rangle$ directions indicates similar total misfit dislocation length in both directions, suggesting that the relaxation is near equilibrium. Besides, as the epilayer tilt is primarily caused by nonzero net out-of-plane Burgers vectors due to imbalance between dislocation glide/multiplication in different directions, the small lattice tilt amplitude also indicates nearly equal amounts of α and β dislocation involved in the relaxation process,[23] supporting the conclusion that the InAlAs buffer relaxed symmetrically from the above analysis.

The RLP from $GaAs_{0.35}Sb_{0.65}$ layer in the InAs-like interface structure was well resolved from its lattice matched $In_{0.7}Ga_{0.3}As$ channel/drain layer due to heavily C doping induced lattice contraction, which is different from GaAs-like interface structure where the $GaAs_{0.35}Sb_{0.65}$ layer RLP is masked by $In_{0.7}Ga_{0.3}As$ layer. The measured lattice constants along the out-of-plane and in-plane directions of the $GaAs_{0.35}Sb_{0.65}$ layer were found to be 5.9249 Å and 5.9064 Å, respectively, with the projection of the x-ray beam along $[1\bar{1}0]$, showed a strain relaxation value of 80%. Similarly, the lattice constants along the out-of-plane and in-plane directions of this layer with the incident beam along [110] direction were found to be 5.9247 Å and 5.9065 Å, respectively, corresponding to the strain relaxation of 81%. This indicates the symmetric strain relaxation of the $GaAs_{0.35}Sb_{0.65}$ layer on the linearly graded $In_xAl_{1-x}As$ buffer. Thus, the strain relaxation of $GaAs_{0.35}Sb_{0.65}$ layer in the InAs-like structure is almost identical as the relaxation value of the $GaAs_{0.35}Sb_{0.65}$ layer in GaAs-like interface structure once the top $In_{0.7}Ga_{0.3}As$ layer was carefully etched from the TFET structure. It is reasonable to assume that the quality of the $GaAs_{0.35}Sb_{0.65}$ layer on the linearly graded $In_xAl_{1-x}As$ buffer in both InAs-like and GaAs-like interface TFET structures is identical in terms of strain relaxation properties and the elongation of the RLP in RSMs.

The strain relaxation property of the $In_{0.7}Ga_{0.3}As$ layer is investigated with the effect of GaAs-like and InAs-like interfaces using RSMs. Comparing Figures 8 and 9 with Figures 5 and 6, a distinct $In_{0.7}Ga_{0.3}As$ RLP was observed in RSMs in the InAs-like interface structure than combined RLPs of both $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ layers in the GaAs-like interface TFET structure. In the latter case, the $GaAs_{0.35}Sb_{0.65}$ layer is masked by the defective $In_{0.7}Ga_{0.3}As$ layer, as discussed in Sec. III A 3 a. The measured out-of-plane and in-plane lattice constants of the $In_{0.7}Ga_{0.3}As$ layer with incident beam along $[1\bar{1}0]$ direction were 5.9481 Å and 5.9157 Å, respectively, showing a strain relaxation value of 75%. Similarly, the out-of-plane and in-plane lattice constants with the incident beam along [110] direction were 5.9481 Å and 5.9168 Å, respectively, corresponding to the strain relaxation value of 76%. The strain relaxations in both directions are symmetric. However, the strain relaxation values are less than that of $In_{0.7}Ga_{0.3}As$ layer in the GaAs-like interface structure. The lower value of strain relaxation indicates reduced dislocation density in the $In_{0.7}Ga_{0.3}As$ layer, which could be further supported from the shorter elongation of $In_{0.7}Ga_{0.3}As$ RLP, $\Delta q_{[1\bar{1}0]}$, from Figure 8 and $\Delta q_{[110]}$ from Figure 9, along $\Delta\omega$ direction. Smaller dislocation density in [110] (or $[1\bar{1}0]$) direction leads to less diffuse scattering of x-rays in its orthogonal $[1\bar{1}0]$ (or [110]) direction, resulting in the shorter elongation of contours along $\Delta\omega$ direction in $[1\bar{1}0]$ (or [110]) direction.

One can find from the asymmetric (115) RSMs in the two orthogonal $\langle 110 \rangle$ directions that the $In_{0.7}Ga_{0.3}As$ layer is fully relaxed in the GaAs-like interface TFET structure as shown in the fully relaxed line in Figures 5(b) and 6(b) (blue dashed line). On the other hand, the RLP maxima from $In_{0.7}Ga_{0.3}As$ layer in the InAs-like interface TFET structure appears in between the fully strain line (red solid line) and the fully relaxed line (blue dashed line) in both Figures 8(b) and 9(b). This indicates that the $In_{0.7}Ga_{0.3}As$ layer is pseudomorphic in nature compared to the $In_{0.7}Ga_{0.3}As$ layer in the GaAs-like interface layer. Besides, the pseudomorphic nature of the $In_{0.7}Ga_{0.3}As$ layer in the InAs-like interface structure can be confirmed by the RLP from the $In_{0.7}Ga_{0.3}As$ layer which appears directly under the RLP from $GaAs_{0.35}Sb_{0.65}$ in the asymmetric (115) RSMs. Although, the in-plane lattice constant of $In_{0.7}Ga_{0.3}As$ layer is higher than the lattice constant of $GaAs_{0.35}Sb_{0.65}$ layer, the small difference in lattice constant does not generate strain relaxation of the $In_{0.7}Ga_{0.3}As$ layer due to the critical layer thickness consideration. Moreover, a larger out-of-plane lattice constant difference of these two layers should be expected in the symmetric (004) RSMs. Since the out-of-plane and in-plane lattice constants of $In_{0.7}Ga_{0.3}As$ layer were different and the out-of-plane lattice is larger, there is a compressive strain exists in the $In_{0.7}Ga_{0.3}As$ layer, which leads to the in-plane lattice constant of the $In_{0.7}Ga_{0.3}As$ layer followed the in-plane lattice constant of $GaAs_{0.35}Sb_{0.65}$ layer. It should also be noted that the apparent change of RLP position of

$GaAs_{0.35}Sb_{0.65}$ with respect to the $In_{0.7}Ga_{0.3}As$ could be due to the lattice contraction due to heavy C doping inside the $GaAs_{0.35}Sb_{0.65}$ layer. In realistic situation, the lattice constant difference between $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers is lower than the apparent position of these two layers in RSMs. The calculated in-plane and out-of-plane lattice constants of these two layers are summarized in Table I. From the measured in-plane and out-of-plane lattice constants, only ~4% strain relaxation was expected in the $In_{0.7}Ga_{0.3}As$ layer with respect to the $GaAs_{0.35}Sb_{0.65}$ layer. The pseudomorphic characteristic of the $In_{0.7}Ga_{0.3}As$ layer indicates the lower dislocation density at the $In_{0.7}Ga_{0.3}As$/$In_{0.7}Ga_{0.3}As$ interface or within the $In_{0.7}Ga_{0.3}As$ layer. Therefore, the InAs-like interface TFET structure creates a "virtually" defect-free active region compared to GaAs-like interface TFET structure, which is desirable for improving the performance of TFET devices with lower OFF state p^+-i-n^+ leakage and higher I_{ON}/I_{OFF} ratio.

B. Surface morphology

It is important to characterize the surface morphology (roughness, other possible features) for metamorphic TFET structures due to the expected crosshatch resulting from ideal strain relaxation with minimum concentrations of threading dislocations, as this is an important figure of merit. Surface morphology of the two TFET structures was examined by AFM in contact mode. The $20\,\mu m \times 20\,\mu m$ AFM micrographs of these two structures and related line profiles in two orthogonal $\langle 110 \rangle$ directions are shown in Figures 10 and 11, respectively. From Figure 10, the anticipated two-dimensional crosshatch pattern is well-developed and quite uniform, as expected for an ideal graded buffer, from the InAs-like interface TFET structure. Crosshatch pattern is a common surface morphology which is observed after plastic strain relaxation in the heteroepitaxy of mismatched layers that grow in a two-dimensional mode. Crosshatch pattern shows a characteristic undulating morphology with hills and valleys parallel to the intersection of slip planes with the crystal surface.[40] In our case, the undulating surface morphology exhibits ridges and grooves parallel to the [110] and [1$\bar{1}$0] directions on the surface. The peak-to-valley height from line profiles in the two orthogonal $\langle 110 \rangle$ direction is also included in these figures. The uniform distribution of the crosshatch pattern from [110] and [1$\bar{1}$0] directions for the InAs-like interface TFET structure suggests a symmetric relaxation of the linearly graded buffer layer, which is in agreement with the XRD results. The AFM micrograph of the InAs-like interface structure shows a smooth surface morphology with surface *rms* roughness of 3.17 nm. Compared to the surface morphology of InAs-like interface, the GaAs-like interface structure does not exhibit two-dimensional crosshatch surface morphology. A grainy texture dispersed crossing the surface was observed from the AFM micrograph of the GaAs-like interface structure. From the line profiles along [110] and [1$\bar{1}$0] directions, the peak-to-valley height of GaAs-like interface sample is 3× higher than the InAs-like interface structure, indicating a significantly poor surface quality due to the large amount of dislocation embedded within the TFET structure. The surface *rms* roughness of the GaAs-like interface sample is 4.46 nm, which is much higher than that of the InAs-like interface structure. The rough surface and deterioration of the two-dimensional cross-hatch pattern on the surface of GaAs-like interface structure should be attributed to the higher dislocation density of the $In_{0.7}Ga_{0.3}As$ layer introduced by the GaAs-like interface,

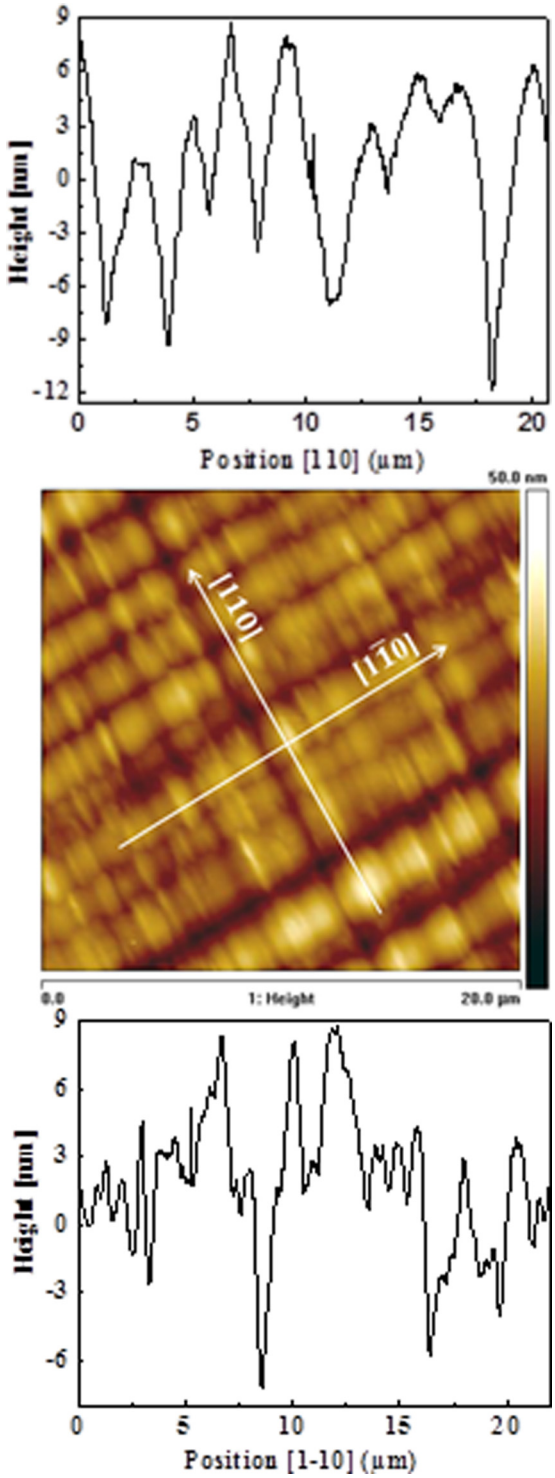

FIG. 10. 20 $\mu m \times 20\,\mu m$ AFM surface morphology and line profiles in two orthogonal $\langle 110 \rangle$ directions of the InAs-like interface TFET structure. The micrograph shows typical cross-hatch pattern with *rms* roughness of 3.17 nm.

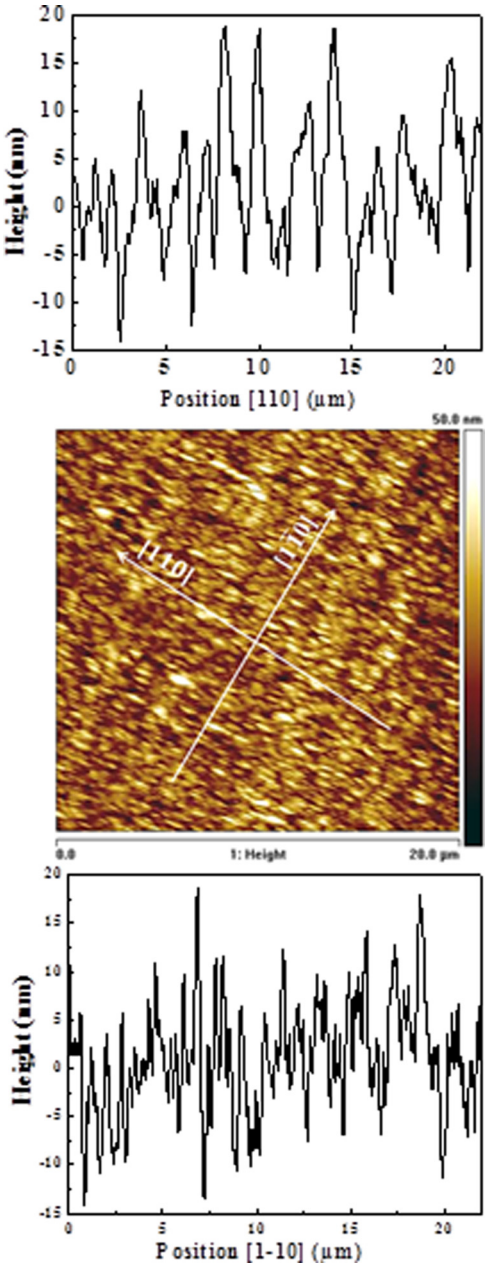

FIG. 11. 20 μm × 20 μm AFM surface morphology and line profiles in two orthogonal ⟨110⟩ directions of the GaAs-like interface TFET structure. The micrograph shows a grainy texture dispersed crossing the surface with *rms* roughness of 4.46 nm.

which was also confirmed by the broadening of the RLP during x-ray measurement as discussed earlier in this paper. From the AFM micrographs of these two structures, it can be concluded that the InAs-like surface structure shows a much better surface morphology with typical two-dimensional cross-hatch patterns and lower peak-to-valley height corresponding to a reduced *rms* roughness than those of the GaAs-like interface structure. As the two structures are identical except the interface between $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, one can indicate that the InAs-like interface can provide a better surface morphology relating to higher crystalline quality of the $In_{0.7}Ga_{0.3}As$ layer and thus one can expect a much lower defect density in the InAs-like interface TFET structure and superior electrical transport properties.

C. Dislocation and defects

Further insight into the structural properties of the GaAs-like interface and InAs-like interface TFET structures is provided by cross-sectional TEM analysis. Figures 12 and 13 show representative cross-sectional TEM micrographs of the GaAs-like interface and InAs-like interface structures, respectively. All the layers were labeled in these figures and the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface was denoted by an arrow in each micrograph. One can find from these figures that in the linearly graded $In_xAl_{1-x}As$ buffer layer, the dislocations were confined within the graded buffer layer and the uppermost region of the graded $In_xAl_{1-x}As$ buffer of thickness about 200 nm has a minimal dislocation and not observed at this scale. As evidenced in the literature that the linearly graded buffer appears to have advantages of spreading the misfit dislocations with depth throughout the layer, it is supposed to leave less residual strain on the top of the buffer layer.[41,42] Since near to the top of linear grades, where the residual strain is significantly small, no further relaxation will take place, leaving a strained and dislocation-free region at the top of the linearly graded buffer. No threading dislocations are observable in the $GaAs_{0.35}Sb_{0.65}$ layers grown on the linearly graded $In_xAl_{1-x}As$ buffers in both of the two structures, indicating that the $In_xAl_{1-x}As$ linearly graded buffer effectively accommodates the lattice mismatch between the active layer and the InP substrate and thus provides a high-quality virtual substrate for the TFET structures.

It can be seen from Figure 12 that the $In_{0.7}Ga_{0.3}As$ layer of the GaAs-like interface TFET structure is full of threading dislocations. Threading dislocations were generated from the interface of $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ and went all the way up until the end of the structure. The dislocation density in the $In_{0.7}Ga_{0.3}As$ layer was too high to be quantified. As no dislocation was observed from the bottom $GaAs_{0.35}Sb_{0.65}$ layer on which the $In_{0.7}Ga_{0.3}As$ was grown, it was reasonable to conclude that the GaAs-like interface contributed to

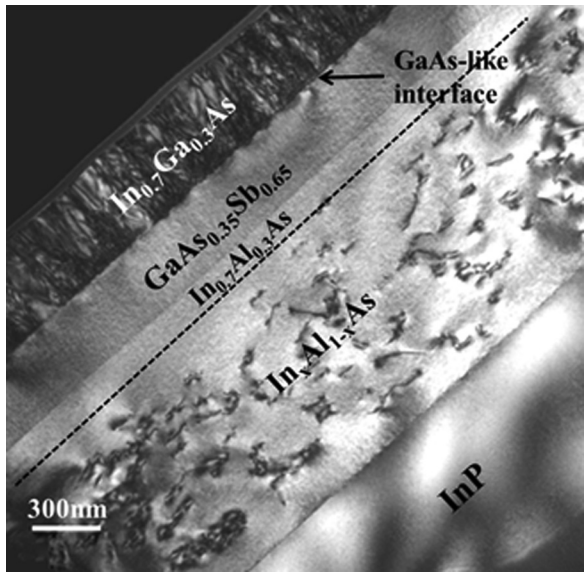

FIG. 12. Cross-sectional TEM micrograph of the GaAs-like interface TFET structure. High threading dislocation density is shown in the $In_{0.7}Ga_{0.3}As$ channel and drain layers.

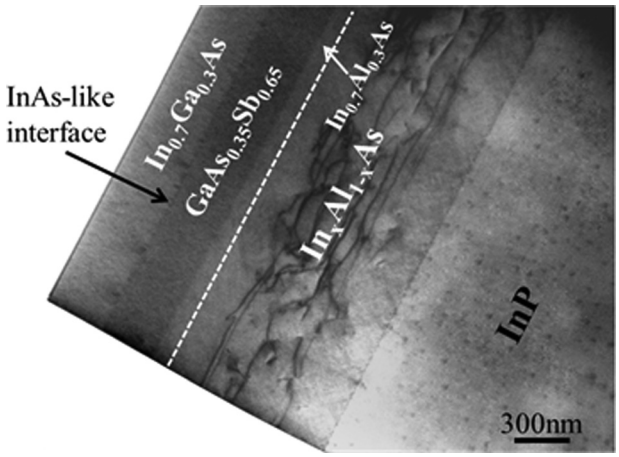

FIG. 13. Cross-sectional TEM micrograph of the InAs-like interface TFET structure. No threading dislocation is observed in the $In_{0.7}Ga_{0.3}As$ channel and drain layers with this magnification.

the high dislocation density in the $In_{0.7}Ga_{0.3}As$ layer and it is consistent with the XRD analysis discussed above. Moreover, it is also clear that the poor surface morphology of the GaAs-like interface TFET structure from AFM measurement and the elongation of the RLP in RSMs are due to a very high defect density present in the top $In_{0.7}Ga_{0.3}As$ layer, as observed by cross-sectional TEM. On the other hand, no threading dislocations were observed in the top $In_{0.7}Ga_{0.3}As$ layer of the InAs-like interface TFET structure at this magnification, indicating a threading dislocation density (TDD) in this layer on the order of or below $\sim 10^7/cm^2$. The low dislocation density of the $In_{0.7}Ga_{0.3}As$ layer in the InAs-like interface structure leads to a superior surface and well-developed two dimensional crosshatch pattern from the linearly graded buffer, both of which are confirmed with the results from AFM analysis. Moreover, the low dislocation density also contributes to the pseudomorphic characteristic of the $In_{0.7}Ga_{0.3}As$ layer and the small $\Delta\omega$ broadening of the RLP in RSMs from InAs-like interface TFET structure. The InAs-like interface provides a high-quality TFET structure compared to GaAs-like interface, where higher dislocations are seen in the channel and drain $In_{0.7}Ga_{0.3}As$ layer, as seen from x-ray, AFM, and cross-sectional TEM analysis. The higher dislocation density at the source/channel interface and within the channel/drain layer will enhance both the SRH G-R and tunneling process at the heterointerface, which will contribute to the higher OFF state leakage current and degrades the I_{ON}/I_{OFF} ratio of the TFET devices.

D. Comparison of OFF state current of TFET devices with InAs-like and GaAs-like interface at source/channel region

In order to assess what impact the difference between InAs-like and GaAs-like interface at source/channel may have on the OFF state leakage current of TFETs, two sets of TFET devices were fabricated and tested. The schematic of the fabricated device and corresponding tilted-view SEM micrograph were shown in Figures 2(a) and 2(b), respectively. As the OFF state current of TFETs is governed by the leakage current of the reverse-biased p^+-i-n^+ diode,[18] current-voltage (I-V) characteristics of these p^+-i-n^+ diodes were measured and compared.

Figure 14 shows the I-V characteristics of the un-gated GaAs-like interface and InAs-like interface p^+-i-n^+ diodes at room temperature. About four orders of higher leakage current density was observed from the GaAs-like interface structure than the InAs-like interface p^+-i-n^+ diodes at 300 K, indicating different OFF state current mechanisms are involved in these TFET structures with different interface termination at source/channel region. In order to gain insight into the OFF state current mechanism for these TFET structures, temperature dependent I-V measurements were carried out on these reverse-biased p^+-i-n^+ diodes with temperature ranging from 150 K to 300 K and simulations have been performed with Sentaurus.[43] Physical models consisting of Jain-Roulston band-gap narrowing,[44] field-enhanced SRH G-R,[45] radiative and auger generation-recombination model[43] were used to explain the observed differences of OFF-state leakage current. A list of parameters used for this simulation is provided in Table II. In both GaAs-like and InAs-like interface TFET structures, the source and drain layers were heavily doped. As a result of heavy doping, carrier-carrier and carrier-impurity interactions were increased due to high impurity concentration and smaller carrier-carrier distance. These interactions either lowered the conduction band edge or raised the valence band edge, resulting in band gap narrowing (BGN) effect. Jain-Roulston model[44] was used to calculate BGN for both TFET structures at each band edge of n- and p-sides.

Figure 15 shows the I-V characteristics of the p^+-i-n^+ diode leakage current as a function of measurement temperatures of the GaAs-like interface TFET devices. One can find from this figure that the OFF state leakage current is decreasing when the temperature is decreased from 300 K to 150 K, as expected. Moreover, the small temperature dependence and the higher leakage current confirmed that the tunneling process is the dominated OFF state transport mechanism involved in the GaAs-like interface TFET structure, which is

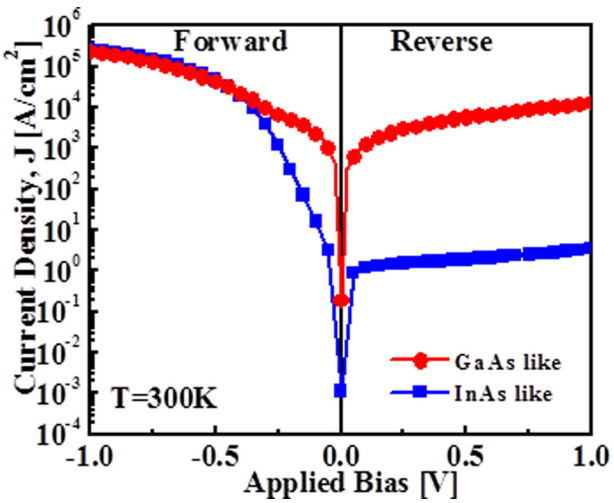

FIG. 14. Measured I-V characteristic of GaAs-like interface and InAs-like interface ungated p^+-i-n^+ diode at T = 300 K. Almost four orders higher leakage current density was observed from the GaAs-like interface p^+-i-n^+ diode than the InAs-like interface p^+-i-n^+ diode.

TABLE II. List of the material parameters used for the simulations.

Parameters	Units	$In_{0.7}Ga_{0.3}As$	$GaAs_{0.35}Sb_{0.65}$
Band gap	eV	0.58	0.703
Effective conduction band density of states	cm^{-3}	2.1×10^{17}	2.13×10^{17}
Effective valence band density of states	cm^{-3}	7.7×10^{18}	1.48×10^{19}
Electron effective mass (relative)	m_0	0.0422	0.0417
Hole effective mass (relative)	m_0	0.0523	0.0612
Electron Auger coefficient	$cm^6\ s^{-1}$	6.6×10^{28}	3.6×10^{28}
Hole Auger coefficient	$cm^6\ s^{-1}$	6.6×10^{28}	3.6×10^{28}
Electron SRH lifetime	ps	20	20
Hole SRH lifetime	ps	20	20
Radiative recombination coefficient	$cm^3\ s^{-1}$	2.93×10^{-10}	3.17×10^{-10}

indeed the case due to higher dislocation density present in the $In_{0.7}Ga_{0.3}As$ channel and drain regions (as shown in Figure 12). A direct BTBT model[19] was performed to explain the observed high OFF state current as a function of temperature, due to the higher dislocation density observed at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ source/channel heterointerface, as seen earlier from our cross-sectional TEM analysis. As shown in Figure 15, the simulated *I-V* characteristics of the reverse-biased p^+-i-n^+ diode agreed well with the measured data at all temperatures studied in this paper. To explain why the BTBT process dominates the OFF state transport of the GaAs-like interface TFET structure, positive fixed charges caused by Tamm states or point defects which are widely observed at the heterointerfaces of mixed As/Sb material systems[46,47] were introduced at the GaAs-like interface region in the simulation. The fixed positive charges cause energy band bending at the GaAs-like heterointerface region. Figure 16 shows the simulated band diagram of the GaAs-like interface TFET structure and the inset shows the position of the fixed positive charges in this energy

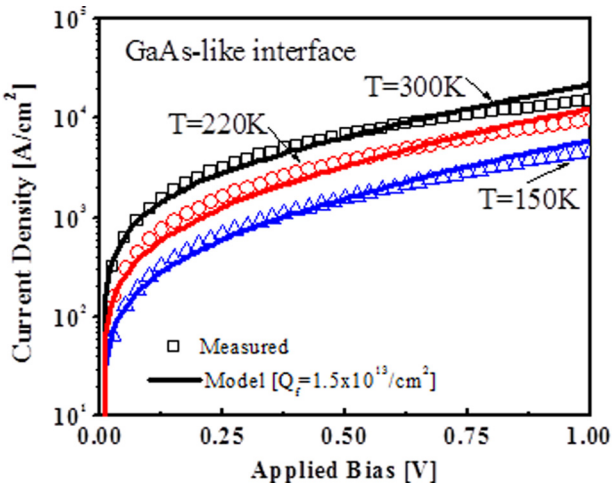

FIG. 15. Measured and simulated *I-V* characteristics of reverse-biased GaAs-like interface p^+-i-n^+ diode for temperature ranging from 150 K to 300 K. The direct BTBT model agrees well with the measured data at different temperature ranges. The small temperature dependence and the high leakage current confirm that the tunneling process is the dominating OFF state transport mechanism in this structure.

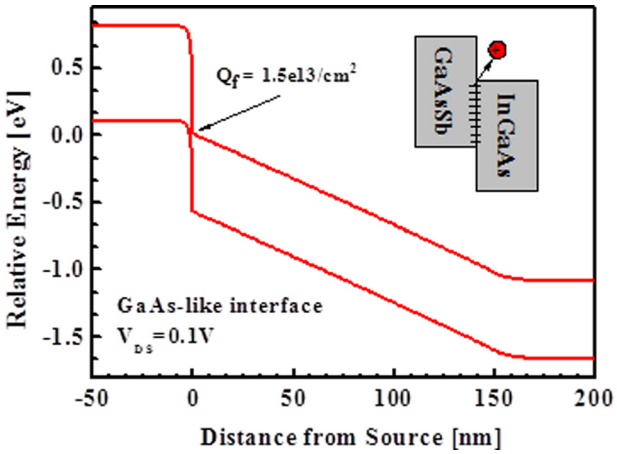

FIG. 16. Simulated band diagram of GaAs-like interface TFET structure with $V_{DS} = 0.1$ V. The inset shows the position of fixed positive charge. High fixed charge density bends energy bands, resulting in overlap of the valence band of $GaAs_{0.35}Sb_{0.65}$ source and conduction band of $In_{0.7}Ga_{0.3}As$ channel, causing the device to be normally on even at OFF state.

band diagram. A high fixed positive charge density of $1.5 \times 10^{13}/cm^2$ due to higher defect density is indeed needed to induce the large band bending in the GaAs-like interface structure to generate the OFF state current as measured in different temperature ranges. As shown in Figure 16, the fixed charge density at this level can convert the band alignment of the TFET structure from staggered gap to broken gap, resulting in overlap of the valence band of $GaAs_{0.35}Sb_{0.65}$ source and conduction band of $In_{0.7}Ga_{0.3}As$ channel, causing the device to be normally ON even at OFF state condition. As a result, the high fixed positive charge density caused by Tamm states or point defects related to the high defect density at the GaAs-like interface leads to the interband tunneling which dominates the OFF state transport of the GaAs-like interface TFET structure.

The direct BTBT is negligible in the InAs-like interface TFET structure, since the active device region (i.e., source-channel-drain) is pseudomorphic and the observed defect density was significantly lower than GaAs-like interface structure. Figure 17(a) shows the *I-V* characteristics of the p^+-i-n^+ diode leakage current as a function of measurement temperatures of the InAs-like interface TFET devices. One can find from this figure that the OFF state leakage current at 300 K is about 4 orders lower than GaAs-like interface TFET structure. Moreover, the observed difference of the OFF state leakage current decreases faster with the decreasing temperature than the GaAs-like interface TFET structure, which is signaling a different transport mechanism involved in the InAs-like interface TFET devices. A field enhanced SRH G-R model[45] was used to explain the observed differences in OFF state leakage current at different temperature. The simulated *I-V* characteristics agreed well with the measured data. In this model, band-traps-band tunneling (also called field enhanced SRH G-R)[45] and thermionic emission process[18] were used to explain the OFF state leakage current in the InAs-like interface TFET devices. A lower positive fixed change density, $Q_f = 10^{12}\ cm^{-2}$ due to lower defect density in the active region compared to GaAs-like interface ($Q_f = 1.5 \times 10^{13}\ cm^{-2}$), was incorporated in the simulation

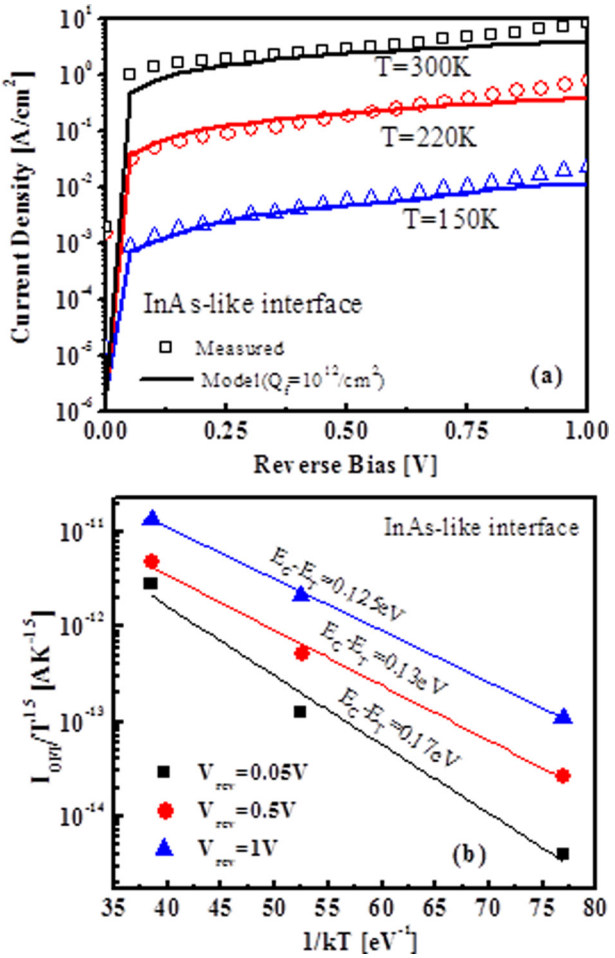

FIG. 17. (a) Measured and simulated *I-V* characteristics of reverse-biased InAs-like interface p^+-*i*-n^+ diode for temperature ranging from 150 K to 300 K and (b) an extraction of the activation energy for leakage current generation as a function of reverse bias voltage of InAs-like interface p^+-*i*-n^+ diode. The field enhanced SRH generation-recombination model with band-traps-band tunneling followed by thermionic emission agrees well with the measured data. The activation energy shows dependence of reverse bias voltage.

along with band-traps-band tunneling process to explain the lower OFF state leakage current. The simulated data agreed well with the experimental results at different temperatures suggest the validation of the model used in InAs-like interface TFET devices.

Figure 17(b) shows the Arrhenius plot of the OFF-state leakage of reverse-biased p^+-*i*-n^+ diode as a function of $1/kT$ at various reverse bias voltages. A straight line fitting to these data points at a given reverse bias yields a gradient which corresponds to the activation energy of $Ea = E_C - E_T$, which is responsible for the OFF state leakage current generation. Here, E_C stands for the conduction band minimum of channel near the source/channel interface and E_T is the energy of trap states. One can find from this figure that Ea decreases with increasing reverse bias voltage from 0.17 eV to 0.125 eV, results in an increasing leakage current trend. This is due to the fact that the electrical field intensity across the p^+-*i*-n^+ diode was enlarged as increasing the reverse bias voltage. The enlarged electrical field further increases the band-bending which leads to an enhanced band-traps-band tunneling process across the interface.

This enhanced tunneling process results in a shallower activation energy compared with deep energy states of SRH process which usually located at the half of the bandgap. This leads to a faster capture-emission process and contributes to lower lifetimes of electrons and holes ($\tau_p = \tau_n = 20$ ps) in the InAs-like interface TFET structure at the OFF state condition. Simulation was performed in order to see the $Q_f = 10^{12}\,cm^{-2}$ effect on the energy band diagram of the InAs-like interface TFET structure, as shown in Figure 18. One can find from this figure that the fixed positive charge density Q_f is lower than GaAs-like interface TFET structure due to the superior interface quality as suggested by structural analysis. Simulation also suggests that the type-II staggered nature of band alignment was well maintained in the InAs-like interface TFET structure, which leads to lower leakage current at OFF state condition.

In order to gain further insight into the band alignment of these TFET structures as a function of fixed positive change density within the source/channel interface region introduced by Tamm states and point defects, simulation was performed to generate band diagram at different Q_f. As shown in Figure 19, the band offset, defined as the energy difference between the conduction band minimum of channel and the valence band maximum of source at the interface, becomes smaller with increasing value of Q_f. One can find from this figure that by varying Q_f content, the band lineup can be adjusted from staggered to broken. Although a broken lineup yields the best ON state performance, it can also increase the OFF state leakage current and thus significantly reduces the I_{ON}/I_{OFF} ratio. Figure 19 inset shows the band offset in source and channel as a function of Q_f. It can be seen from this figure that the fixed positive charge density below $1 \times 10^{12}/cm^2$ has minimal impact on the change of band offset in the InAs-like interface TFET structure. However, the band offset changes rapidly with the positive fixed charge density greater than $1 \times 10^{12}/cm^2$. Moreover, the band alignment is converted from staggered gap to broken gap at the fixed charge density of $\sim 6 \times 10^{12}/cm^2$. In order to

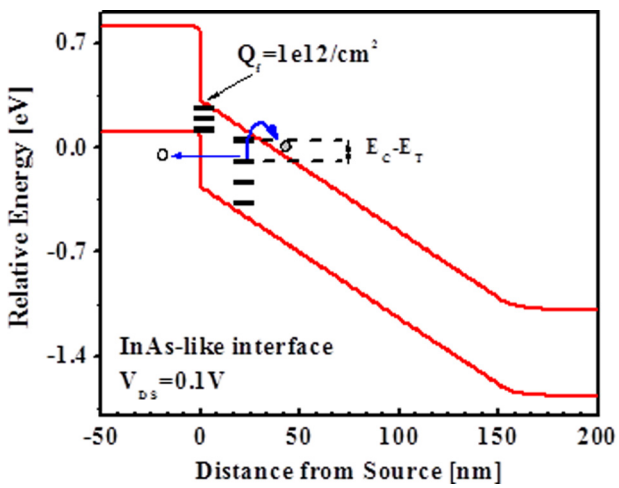

FIG. 18. Simulated band diagram of InAs-like interface TFET structure with $V_{DS} = 0.1$ V. Fixed charges and trap states are indicated in the figure. The staggered band alignment is well kept due to lower fixed charge density at the interface region of source/channel.

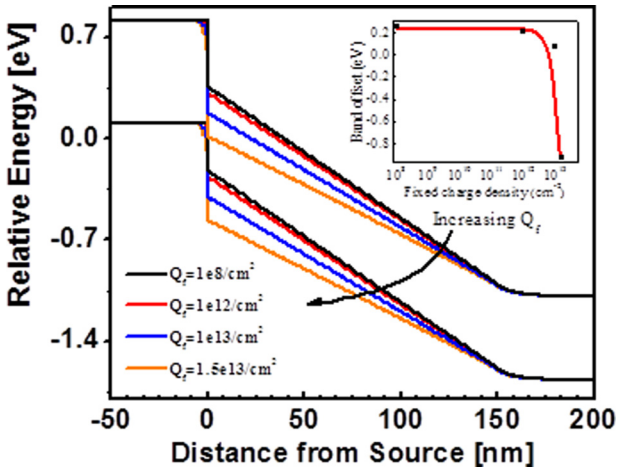

FIG. 19. Simulated band diagrams of $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ n-channel heterostructure TFET structures with different fixed charges at source/channel interface region. The inset shows the band offset ($E_{C\ channel} - E_{V\ source}$) changes as a function of fixed charge density. The band alignment is converted from staggered gap to broken gap at the fixed charge density of $\sim 6 \times 10^{12}/cm^2$.

maintain the staggered nature of band alignment, the lower Q_f is essential, which can only be achieved by minimizing the interface defect density in a TFET structure. The InAs-like interface provides lower defect density which leads to lower Q_f at the source/channel heterointerface, resulting in well maintained type-II staggered gap band alignment. It leads to lower OFF state leakage current, higher I_{ON}/I_{OFF} ratio and shows a great potential for future high-performance heterostructure TFETs for low-power logic applications.

IV. CONCLUSIONS

The strain relaxation behavior, surface morphology, and dislocation properties of MBE grown mixed As-Sb type-II staggered gap tunnel FET heterostructures with GaAs-like and InAs-like interface at the source/channel region have been investigated. The OFF state leakage current transport mechanisms of these tunnel FET devices with two different interfaces were studied. Both GaAs-like and InAs-like interface TFET structures exhibited symmetric strain relaxation. However, the GaAs-like interface introduced high dislocation density, as observed by cross-sectional TEM micrograph, resulting in the elongation of reciprocal lattice point of $In_{0.7}Ga_{0.3}As$ layer in the reciprocal space maps and poor surface morphology, while the InAs-like interface creates a defect-free interface for the pseudomorphic growth of the $In_{0.7}Ga_{0.3}As$ channel and drain layer with minimal elongation along $\Delta\omega$ direction and uniform two-dimensional cross-hatch surface morphology. High fixed positive charge density of greater than $10^{13}\,cm^{-2}$ due to Tamm states and point defects caused by defective GaAs-like interface results in overlap of the valence band of source and the conduction band of channel regions. As a result, higher OFF state leakage current dominated by band-to-band tunneling process was observed. On the other hand, the InAs-like interface exhibited lower fixed positive charge density of $10^{12}\,cm^{-2}$ and type-II staggered band alignment was well maintained. Due to this, significantly lower OFF state leakage current caused by the field enhanced Shockley-Read-Hall generation-recombination process at different temperatures was observed in this TFET structure. The fixed positive charge at the source/channel heterointerface influences the band lineup substantially with charge density greater than $1 \times 10^{12}/cm^2$ and the band alignment is converted from staggered gap to broken gap at the fixed charge density of $\sim 6 \times 10^{12}/cm^2$, leading to high OFF state leakage current. Finally, InAs-like interface at source/channel region provides superior structural and electrical properties of the mixed As-Sb type-II staggered gap tunnel field effect transistors and thus, making it a very promising device candidate for high-performance and ultra-low power applications.

ACKNOWLEDGMENTS

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