

***In situ* grown Ge in an arsenic-free environment for GaAs/Ge/GaAs heterostructures on off-oriented (100) GaAs substrates using molecular beam epitaxy**

Mantu K. Hudait,^{a)} Yan Zhu, Nikhil Jain, Siddharth Vijayaraghavan, and Avijit Saha
Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, Virginia 24061

Travis Merritt and Giti A. Khodaparast
Department of Physics, Virginia Tech, Blacksburg, Virginia 24061

(Received 26 April 2012; accepted 24 July 2012; published 10 August 2012)

High-quality epitaxial Ge layers for GaAs/Ge/GaAs heterostructures were grown *in situ* in an arsenic-free environment on (100) off-oriented GaAs substrates using two separate molecular beam epitaxy (MBE) chambers, connected via vacuum transfer chamber. The structural, morphological, and band offset properties of these heterostructures are investigated. Reflection high energy electron diffraction studies exhibited (2×2) Ge surface reconstruction after the growth at 450 °C and also revealed a smooth surface for the growth of GaAs on Ge. High-resolution triple crystal x-ray rocking curve demonstrated high-quality Ge epilayer as well as GaAs/Ge/(001)GaAs heterostructures by observing Pendellösung oscillations and that the Ge epilayer is pseudomorphic. Atomic force microscopy reveals smooth and uniform morphology with surface roughness of ~ 0.45 nm and room temperature photoluminescence spectroscopy exhibited direct bandgap emission at 1583 nm. Dynamic secondary ion mass spectrometry depth profiles of Ga, As, and Ge display a low value of Ga, As, and Ge intermixing at the Ge/GaAs interface and a transition between Ge/GaAs of less than 15 nm. The valence band offset at the upper GaAs/Ge- (2×2) and bottom Ge/(001)GaAs- (2×4) heterointerface of GaAs/Ge/GaAs double heterostructure is about 0.20 eV and 0.40 eV, respectively. Thus, the high-quality heterointerface and band offset for carrier confinement in MBE grown GaAs/Ge/GaAs heterostructures offer a promising candidate for Ge-based *p*-channel high-hole mobility quantum well field effect transistors. © 2012 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4742904>]

I. INTRODUCTION

With continued transistor scaling, new materials and device architectures are needed to continue the transistor miniaturization and enhance performance.¹ High performance *n*-channel III-V quantum well (QW) transistors have been demonstrated on Si substrate operating at 0.5 V (Refs. 2–5); however, the demonstration of an equally high-performance *p*-channel QW within the same material system with similar performance remains elusive to date due to low hole mobility in III-V materials without which energy efficient complementary logic circuits will not be realized. Although, strained III-Sb materials, namely InSb,⁶ InGaSb,^{7–10} and GaSb^{11,12} materials are potential *p*-channel candidates, Ge has much higher bulk hole mobility (~ 1900 cm² V⁻¹ s⁻¹) even without strain compared to III-Sb materials (800–850 cm² V⁻¹ s⁻¹). The theoretical investigations of hole transport in 1.5–2% biaxially strained III–V semiconductors show an increase in the hole mobilities up to a factor of 2 over unstrained value^{3–15}; however, the hole mobility in 2% bi-axially strained bulk Ge can be increased up to 4000 cm² V⁻¹ s⁻¹,¹⁶ which is significantly higher than any III–V materials. Considering several material choices and strain engineering in the channel, Ge epitaxial film grown on a large bandgap GaAs material is of immense interest due to lattice match (mismatch $\sim 0.07\%$) which ensures larger critical thickness, lower dislocation

density, and strain-free Ge epitaxial film. As a result, high-hole mobility of Ge and its narrow bandgap ($E_g = 0.67$ eV) make the GaAs/Ge heterojunction suitable for the fabrication of *p*-channel QW field effect transistors,¹⁷ solar cells,¹⁸ metal-oxide semiconductor field effect transistors,^{19,20} millimeter-wave mixer diodes,²¹ temperature sensors,²² photodetectors,^{23,24} and quantum confinement devices.²⁵

In order to realize a high-performance Ge QW transistor structure, higher bandgap III–V barrier layers are essential in order (i) to eliminate parallel conduction,^{2,3} (ii) to provide large valence band offset ($\Delta E_v \geq 0.4$ eV)^{26–29} for hole confinement inside the Ge QW, (iii) to achieve high-quality high-*k*/III–V barrier interface with lower Dit,³⁰ (iv) to control lattice mismatch,^{3,31} (v) to provide strain to the active Ge channel,¹⁷ (vi) to have better interface properties,²⁷ (vii) to provide modulation doping^{3,5} in the Ge quantum well field effect transistor (QWFET) structure, (viii) to control the off state leakage, and (ix) to improve ohmic contact.³² Therefore, selective combination of the best attributes of III–V compound semiconductors stemming from the above properties along with the excellent hole transport properties of Ge in QW configuration²⁵ can enable extremely energy efficient and ultra-high performance computing platform. Moreover, GaAs/Ge epitaxial heterostructures have received a great deal of attention as starting materials for the fabrication of space quality solar cells^{24,25} compared to the conventional GaAs/GaAs solar cells. As large area, minority carrier devices, III–V/Ge cells are extremely sensitive to defects. Thus,

^{a)}Electronic mail: mantu.hudait@vt.edu

elimination of antiphase domains (APDs), which are characteristics of the polar (GaAs)-on-nonpolar (Ge) epitaxy, and suppression of large-scale interdiffusion across the GaAs/Ge heterointerface remain key challenges for increased yield, reliability, and performance of solar cells as well as QW devices. The well-controlled interface properties at the GaAs/Ge/GaAs double heterostructures are extremely important to realize high-performance *p*-channel Ge QWFET applications.

Although, several groups succeeded in growing high-quality Ge epitaxial layer on GaAs^{19,26,27,33–43} and GaAs/Ge/GaAs heterostructures,^{44,45} however, these work suffer from the interdiffusion of elements⁴⁶ and arsenic (As) contamination in the Ge layer due to the Ge and III–V material growth carried out in a single molecular beam epitaxy (MBE) chamber^{34,47} or metal-organic vapor-phase epitaxy chamber.⁴² This results in excess As point defects, which nucleate dislocation loops during the growth of GaAs overlayer on Ge. These loops expand during the subsequent high temperature GaAs growth to generate high threading dislocation densities in the thick GaAs film. Moreover, a substantial fraction of a monolayer of excess arsenic on the surface of either GaAs^{48,49} or Ge^{50,51} (surface contamination from background As) is responsible for the reconstruction $c(4 \times 4)$, $c(2 \times 2)$, $c(2 \times 8)$, $p(2 \times 2)$ patterns, as observed by *in situ* reflection high-energy electron diffraction (RHEED) since this excess As is not part of the GaAs lattice. Furthermore, the epitaxy of Ge on GaAs is strongly affected by the GaAs surface reconstruction, since it can have different valance band offsets between the GaAs and Ge according to surface termination, reconstruction, orientation, and growth temperature.^{28,29} It is evident that one should choose the intrinsic (2×4) surface structure of (001) GaAs rather than other surface reconstruction [e.g., (1×1) -As saturated surface, $c(2 \times 8)$ -As stabilized surface, $c(8 \times 2)$ -Ga-stabilized surface, $c(4 \times 4)$ -As stabilized surface]^{35,40} to have well controlled, smooth, and planar growth of Ge/(001)GaAs heterojunction during MBE growth process. The ambiguity of the surface reconstruction of Ge either mixed (1×2) and (2×1) , (2×2) , $c(2 \times 2)$, $c(4 \times 2)$, $p(2 \times 2)$, single-domain (1×2) , or (2×1) reconstruction can be overcome by growing Ge and GaAs layers in a separate growth chamber, connected via ultra-high vacuum transfer chamber.

The growth at higher temperature and lower growth rate may result in the formation of unwanted *p-n* junction due to simultaneous in-diffusion of Ga and As inside the Ge layer during GaAs overlayer growth and Ge out-diffusion during GaAs overlayer. Furthermore, higher growth temperature and the on-axis (100) Ge wafer results in increased APD formation in GaAs overlayer.⁵² Thus, in Ge epitaxial growth on the off-oriented GaAs(001) substrate, the APDs can be controlled by the precise nucleation of GaAs layer with As prelayer and by lowering the lower growth rate.⁵³ This paper presents a comprehensive study of structural, morphological, optical, and band offset properties of *in situ* grown Ge epitaxial layers as well as GaAs/Ge/GaAs double heterostructures on off-oriented (100) GaAs substrates using separate MBE growth chambers for Ge and III–V. Very recently, we

showed that 1.54% bi-axially strained Ge quantum well with GaPAs barrier layers on Si substrate exhibited hole mobility of approximately $4000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ using $6 \times 6 k \cdot p$ simulation.¹⁷ The result from this experimental finding complement and first step toward achieving high-performance Ge quantum well field effect transistor on off-oriented (100) GaAs substrate which can be ultimately heterogeneously integrated to off-oriented Si substrate for the realization of ultra-low power and high-speed logic applications.

II. EXPERIMENT

The undoped Ge epitaxial layer and GaAs/Ge/(001)GaAs double heterostructures were grown by an *in situ* growth process on offcut (100) epi-ready GaAs substrates (2° and 6° off toward [110] direction) using separate solid source MBE growth chambers for Ge and III–V materials, connected via ultra-high vacuum transfer chamber. This unique growth capability enables us to demonstrate superior Ge epilayer as well as precisely control the GaAs/Ge/GaAs double heterostructure interfaces for realization of high-hole mobility *p*-channel Ge quantum well devices. Substrate oxide desorption was done at $\sim 630^\circ \text{C}$ under an arsenic overpressure of $\sim 1 \times 10^{-5}$ torr in a III–V MBE chamber, which was verified by a strong well-known (2×4) RHEED pattern, indicative of an oxide-free (100) GaAs surface. An initial $0.1 \mu\text{m}$ thick undoped GaAs buffer layer was then deposited at $\sim 600^\circ \text{C}$ to generate a smooth surface under a stabilized As_2 flux prior to transferring the GaAs wafer to the Ge MBE chamber for Ge epilayer growth. Ge epilayer was grown in an As-free MBE chamber and the base pressure of the growth chamber was $\sim 6 \times 10^{-11}$ torr and 2.8×10^{-8} torr during the Ge layer growth. The growth rate for all the Ge layers was kept at 450°C and the growth rate was 0.14 \AA/s , as determined by triple axis x-ray diffraction from Pendellösung thickness fringes and 450°C , respectively. After the growth of Ge epitaxial layer, the growth temperature was carefully reduced from 450°C to 50°C and then the wafer was transferred to the III–V MBE chamber for subsequent GaAs layer growth. The high-quality Ge epilayer on offcut GaAs substrate was verified by RHEED pattern, indicating a double step strong (2×2) RHEED pattern. For the GaAs/Ge/(001)GaAs double heterostructures, only the offcut GaAs substrates were used in order to prevent the formation of APDs. Migration enhanced epitaxy (MEE) with As_2 prelayer was used for the subsequent GaAs growth on Ge epilayer with thickness of $\sim 30 \text{ \AA}$ to eliminate APDs at the GaAs/Ge interface. The growth of upper GaAs layer was carried out at a lower substrate temperature of $\sim 350^\circ \text{C}$ to prevent out-diffusion of Ge and simultaneous in-diffusion of Ga and As in Ge. An As_2/Ga ratio of ~ 14 and reduced growth rate of 0.25 \AA/s was maintained at all times. The nucleation of GaAs on Ge was monitored using RHEED to ensure that no APDs or other defects are generated at the interface. In some structures, the 30 \AA MEE GaAs nucleation layer was followed by the growth of a 500 \AA thick GaAs layer which was grown at a higher temperature of $\sim 500^\circ \text{C}$ and the same growth rate of

0.25 Å/s and As₂/Ga ratio of 14. Table I summarizes the details of each test structure that were characterized in this work.

The thickness of the epitaxial Ge layers investigated ranged from about 10 nm to 150 nm. The 15 keV electron beam energy and a glancing incident angle of 1° to 4° RHEED system (Staib Instruments) was used to record RHEED pattern during growth in III–V MBE chamber. The epitaxial films were investigated using atomic force microscopy (AFM) to reveal the surface roughening and other defects, probably APDs, in a contact mode. The epitaxy of undoped Ge and GaAs/Ge/GaAs double heterostructures was confirmed by Panalytical MRD X'Pert Pro triple axis x-ray diffraction system with CuK α 1 x-ray source. Photoluminescence measurements were carried out at a temperature of 300 K and 93 mW laser power. Argon ion laser operating at a wavelength of 5145 Å was used as a source of excitation. PL signal was detected by a InGaAs-photodetector with an operating range of about 0.72–1.24 eV. Dynamic secondary ion mass spectrometry (SIMS) was performed to determine the compositional profile of As, Ga, and Ge atoms at the GaAs/Ge/GaAs heterointerface. SIMS analysis was performed using Cameca IMS-7f GEO with Cs⁺ as primary ion beam. The band offset of each interface of *in situ* grown GaAs/Ge/GaAs heterostructures were investigated by PHI Quantera SXM scanning x-ray photoelectron spectroscopy (XPS).

III. RESULTS AND DISCUSSION

A. RHEED studies on Ge epilayer grown on (001) GaAs-(2 × 4)

To study the surface morphologies of GaAs epilayer, Ge epilayer on GaAs, and GaAs/Ge/GaAs double heterostructure on off-oriented (001) GaAs wafers, RHEED patterns were recorded at the different stages of the growth. In addition to understand the Ge epilayer morphology, these RHEED patterns shed light on the controversy related to the reconstruction of Ge on (001) GaAs substrate. The (001) surface of compound semiconductors, such as GaAs and InP, shows a variety of reconstructions depending on the processing condition and the resultant surface composition. The As-stabilized (2 × 4) surface of (001) GaAs has been most extensively studied, and is widely accepted to have the two As-dimer model.⁵⁴ For the growth of Ge on (001) GaAs by MBE, Ge layer was deposited on a reconstructed (2 × 4) GaAs surface with a surface layer being mainly arsenic. Since there is no excess arsenic on the (2 × 4) surface, Ge can bond directly to the GaAs lattice. Growth of Ge on such

a surface involves mainly Ge-As bonds (possibly some Ge-Ga bonds at the interface) and subsequent growth of a Ge lattice involves only the Ge-Ge bonding between neighboring atoms. Figures 1(a)–1(d) show RHEED patterns on the surface of the 150 nm Ge epilayer along [110] and [1 $\bar{1}$ 0] directions at 150 °C and 350 °C, respectively, grown on 6° offcut (001) GaAs-(2 × 4) substrate with 0.1 μm GaAs epilayer. These RHEED patterns are recorded after transferring the Ge epilayer from Ge MBE chamber to the III–V MBE chamber. The Ge film grown on (100)/6° GaAs surface with (2 × 4) reconstruction at 450 °C shows a reconstructed streaky (2 × 2) RHEED pattern. A streaky (2 × 2) pattern of Ge on (2 × 4) reconstructed (001) GaAs was achieved throughout the thickness range studied in this paper, suggesting a smooth surface morphology. A similar observation of RHEED pattern has also been reported by other researchers^{33,38,53} on the (001) GaAs surface, which has been interpreted by Bauer and Mikkelsen³⁹ as mixed (2 × 1) and (1 × 2) surface domains.

In contrast, Neave *et al.*³⁷ demonstrated that the growth of Ge on a (001) GaAs-(2 × 4) reconstructed surface at lower temperature <470 K exhibits only a (1 × 1) pattern and the Ge surface is not reconstructed. By annealing this low temperature grown Ge on GaAs-(2 × 4) structure or grown at 600 °C on a (2 × 4) reconstructed GaAs surface, it converts to a well ordered c(2 × 2) reconstructed surface. However, the higher temperature annealing can have severe in-diffusion of Ge into GaAs and out-diffusion of As and Ga into the epitaxial Ge layer. As a result, unwanted *p-n* junction can form inside the Ge layer.⁴⁶ A planar and smooth growth of Ge can therefore be easily reached on a (001) GaAs-(2 × 4) reconstructed surface without the excess arsenic present on the surface. Thus, the separate MBE chambers for Ge and III–V and As-free environment for the deposition of Ge layer on (001) GaAs-(2 × 4) is essential for high-quality GaAs/Ge heterostructure. The surface quality of the (100) GaAs substrate is vital for the high-quality Ge epilayer and thus, the surface preparation procedure is important prior to the growth of Ge epilayer. Most of the researchers use the same MBE chamber for both GaAs and Ge layer growth where the base pressure was $\sim 1 \times 10^{-10}$ torr and the chamber pressure due to As was $\sim 5 \times 10^{-7}$ and $\sim 1 \times 10^{-7}$ torr during the growth of GaAs and Ge, respectively.⁵³ This complicates the Ge surface reconstruction and subsequent GaAs layer growth. Furthermore, we have also investigated the effect of As₂ exposure on the (2 × 2) reconstructed Ge surface grown on GaAs-(2 × 4) using RHEED. Arsenic (beam flux of

TABLE I. Summary of *in situ* grown Ge and GaAs/Ge/GaAs heterostructures.

Sample number	GaAs substrate off-cut	Ge growth temperature (°C)	Ge thickness (nm)	MEE GaAs at 350 °C (nm)	GaAs at 500 °C (nm)	Total GaAs thickness (nm)
A	(100)/2°	450	10	—	—	—
B	(100)/2°	450	20	3	50	53
C	(100)/6°	450	120	—	—	—
D	(100)/6°	450	120	3	50	53
E	(100)/6°	450	150	3	0	3

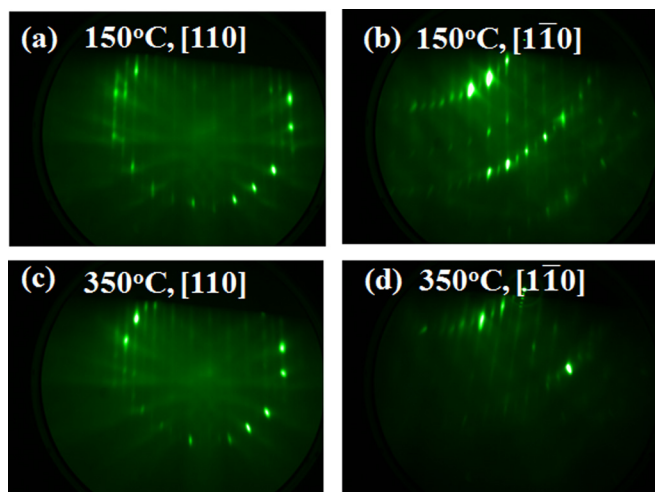


Fig. 1. (Color online) RHEED patterns at 15 kV from the surface of 150 nm Ge epilayer along (a) [110] and (b) $[1\bar{1}0]$ direction at 150 °C, and (c) [110] and (d) $[1\bar{1}0]$ direction at 350 °C, respectively, after the growth on 6° offcut (001)GaAs substrate with 0.1 μm GaAs epilayer. These RHEED patterns were recorded after transfer the Ge epilayer from Ge MBE chamber to III-V MBE chamber. The RHEED patterns exhibited clearly (2×2) Ge surface reconstruction.

$\sim 7 \times 10^{-7}$ torr) exposure for 60 s at 350 °C on such reconstructed Ge surface shows no change of the RHEED pattern, indicates well-constructed Ge surface.

B. RHEED studies on GaAs epilayer grown on Ge-(2 × 2)

The GaAs growth on off-oriented (001) Ge and (001) Ge/SiGe/Si substrates is widely studied. Heteroepitaxy of GaAs/Ge(001) is more complex compared to Ge on (001)GaAs due to polar-on-nonpolar epitaxy. The RHEED studies indicate a basic difference in growth morphology between the growth of GaAs and that of Ge on the polar (100) surface: the growth of Ge on GaAs results in a smooth surface,⁴¹⁻⁴³ whereas the growth of GaAs on Ge produces a rough surface on an atomic scale as observed by several researchers.^{39,55} The observed difference is explained due to an inherent difference in MBE growth mechanism between a compound semiconductor, GaAs, and an elemental semiconductor, Ge. For the growth of (100) GaAs for example, which has a structure consisting of alternating Ga and As layers, the surface layer may be a Ga or an As layer depending on the MBE growth conditions. The growth of Ge onto such a surface could easily give a smooth surface since only one element is involved. During the initial growth of GaAs on Ge, however, both Ga and As atoms can bond to the Ge surface layer. The first layer of GaAs can thus consist of Ga domains containing only Ga atoms and As domains containing only As atoms. Further growth of GaAs would lead to the formation of two different APDs separated by anti-phase boundaries (APBs). We have investigated the growth of GaAs on different thicknesses of Ge(001)-(2 × 2) reconstructed surface. The GaAs layers were grown on Ge/(001)GaAs that are offcut by 2° or 6° toward the [110] directions. The offcut substrate combined with a reconstructed

(2×2) Ge surface and two-step growth process consisting of (i) 30 Å MEE GaAs at low temperature (~ 350 °C) and low growth rate (~ 0.25 Å/s), and (ii) high temperature (~ 500 °C) and low growth rate (~ 0.25 Å/s) were used to eliminate APDs at the GaAs/Ge heterointerface. Figures 2(a) and 2(b) show RHEED pattern on the surface of 30 Å MEE grown GaAs on (001)Ge-(2 × 2) at 350 °C along [110] and [100] direction, respectively. One can find from Fig. 2(a) that the growth of GaAs on (001)Ge-(2 × 2), shows a well-developed twofold along [110] direction and $c(4 \times 4)$ -fold RHEED pattern along [100] direction, as shown in Fig. 2(b). This indicates that the APDs were mostly eliminated using offcut substrate. The growth temperature was not increased in this case for the subsequent high temperature GaAs growth in order to minimize the diffusion process for the use of the undoped Ge layer as a *p*-channel material for high-hole mobility *p*-channel QW structure. An example of the atomic arrangement in different APDs is shown schematically in the upper GaAs layer grown on on-axis (001) Ge in Fig. 3(a) with an APB indicated by a dashed line, and Fig. 3(b) shows the atomic arrangement of the GaAs/Ge/GaAs heterostructure where APDs were eliminated using offcut substrate and proper nucleation conditions as described above. At the (100)Ge/GaAs interface without substrate offcut, both Ge-As and Ge-Ga bonds are polar and could lead to charge accumulation at the interface.

Several interface models for the stoichiometric mixing have been proposed to deal with this charging problem.^{56,57} At the Ge/GaAs interface formed by depositing Ge on a

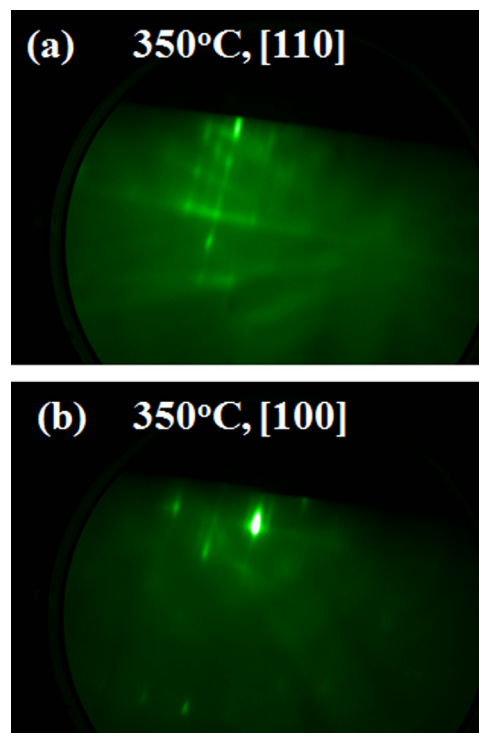


Fig. 2. (Color online) RHEED patterns at 15 kV from the surface of 3 nm GaAs epilayer along (a) [110] and (b) [100] direction at 350 °C grown on epi-Ge/epi-GaAs/(001)GaAs 6° offcut substrate. The fourfold RHEED pattern in (b) corresponds to a $c(4 \times 4)$ surface reconstruction.

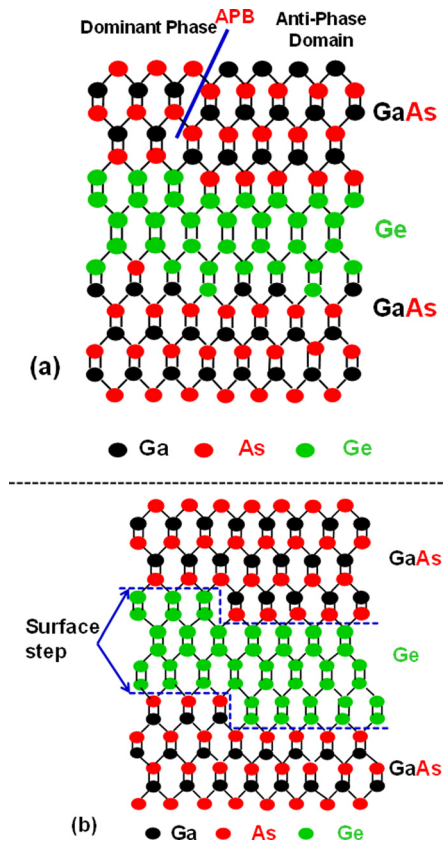


FIG. 3. (Color online) (a) GaAs/Ge/(001)GaAs lattice model which shows APDs separated by APBs where single atomic surface step is not sufficient to eliminate APBs (adopted from Ref. 56) and (b) GaAs/Ge/(001)GaAs with 6° offcut toward [110] direction illustrates double atomic surface step which allows to eliminate APBs using MEE with arsenic prelayer during MBE growth.

GaAs substrate whose surface layer is an As layer, charge neutrality can be achieved by replacing half of the As atoms of this layer by Ge atoms such as that shown at the lower interface of Fig. 3(b). For a GaAs layer grown on Ge, the formation of APDs in the GaAs layer can lead to charge neutrality at the interface if equal areas of Ga domains and As domains are formed in the first layer. However, equal number of As and Ga atoms bonding onto the (001) Ge surface is impossible during MBE growth process since the arsenic has higher vapor pressure and lower sticking coefficient than Ga. On the other hand, by growing GaAs on offcut Ge substrate with As prelayer, lower growth temperature and lower growth rate, the APDs can be eliminated.^{55,58} Thus, the RHEED study of the MBE grown Ge/(001)GaAs-(2 × 4) and GaAs/(001)Ge-(2 × 2) interface has shown different morphologies and it allowed us to estimate the surface roughness for the growth of GaAs on Ge and Ge on GaAs.

C. Surface morphology of Ge/(001)GaAs-(2 × 4) and GaAs/Ge-(2 × 2)/(001)GaAs-(2 × 4) heterostructures

As shown in Secs. III A and III B that RHEED was used to comprehend the growth sequence of both Ge on (001)GaAs-(2 × 4) and GaAs on Ge-(2 × 2)/(001)GaAs-(2 × 4) at different stages of epitaxy. The study not only shows

different growth morphologies of these two cases, it also allows us to estimate the surface roughness in each case. Thus, it is important to characterize the surface morphology on an atomic scale (roughness, APDs, other possible features) for these structures, as this is an important figure of merit. In fact, it is essential to know the surface roughening due to APDs during the MBE growth of GaAs on Ge in order to have structures with truly abrupt and planar interfaces formed during the growth. The morphology of the epitaxial film is influenced by the deposition rate, which controls the adatom population on the surface, and substrate temperature, which affects the surface diffusion rate of the species. Many characteristics of epitaxial growth will be difficult to understand without a better understanding of the surface during growth including doping and the formation and characteristics of superlattice structures. An appropriate knowledge of the epitaxial growth mechanism will allow us to optimize the growth parameters for reproducibly grown APD-free GaAs on Ge by MBE technique. Thus, the careful control of substrate surface structure is essential for realization of APD-free GaAs on Ge/GaAs substrate by MBE technique.

Surface morphology of Ge on (001)GaAs and GaAs on Ge/(001)GaAs structures was examined by AFM in contact mode. AFM images on different length scales have been taken to see the top surface morphology of the epitaxial GaAs and Ge films. AFM micrographs and line profiles of these two structures are shown in Figs. 4(a) and 4(b), respectively. The root mean square (rms) roughness was calculated from AFM micrographs. The rms roughness for Ge on GaAs and GaAs/Ge/GaAs was 0.45 nm and 2.18 nm grown at 450 °C and 350 °C/500 °C, respectively, measured over an area of 10 × 10 μm². From Figs. 4(a) and 4(b), the anticipated extremely uniform and low surface roughness is an indication of high-quality two-dimensional epitaxy of Ge on GaAs as well as GaAs/Ge/GaAs, in complete agreement with the RHEED results and analysis presented above. The peak-to-valley height from line profiles in the two orthogonal ⟨110⟩ direction are also included in these figures. The uniform and smooth surface morphology exhibits the high-quality growth of Ge on 6° off-oriented (001)GaAs-(2 × 4) substrate and higher rms of GaAs/Ge compared to Ge/GaAs is an indicative of polar-on-nonpolar growth at lower temperature. It is evident that the transition of APD-free → APDs → APD-free film with increasing growth temperature has already been found experimentally by Fischer *et al.*⁵⁹ in the MBE grown GaAs on Si. Ringel *et al.*⁴⁷ found that a Ge epitaxial film annealed above 640 °C for 20 min, coupled with a 6° offcut, results in double stepped Ge surface, which greatly suppresses APD formation in GaAs. The significant cross-diffusion at the Ge/GaAs heterointerface at higher growth temperature of GaAs on Ge or annealing of Ge epitaxial layer prior to GaAs top layer would prohibit the purpose of the undoped Ge channel for the high-mobility *p*-channel QWFET option. Thus, the precise optimization of the growth temperature for both Ge and GaAs layer, GaAs surface reconstruction, GaAs substrate offcut, growth rate, As₂/Ga ratio, and no residual arsenic are essential for the high-quality GaAs/Ge/GaAs heterostructure.

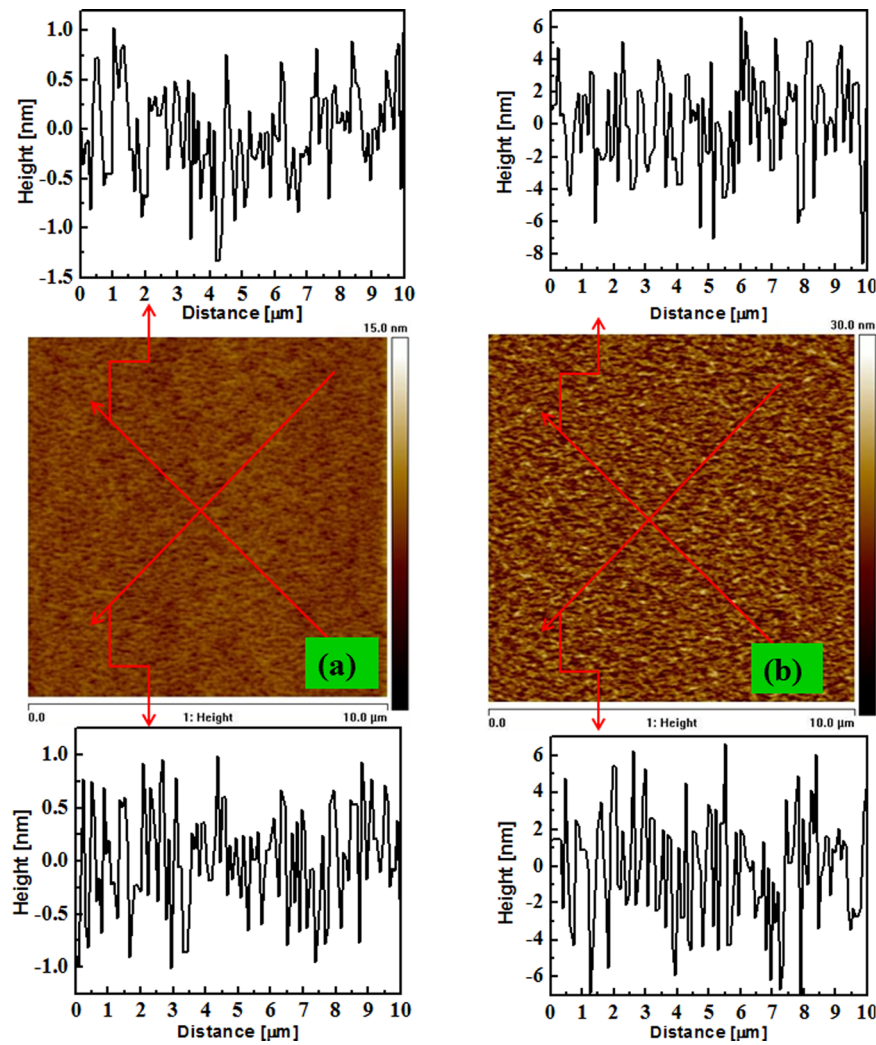


FIG. 4. (Color online) AFM micrographs of (a) 10 nm Ge on (001)GaAs ($rms = 0.45$ nm) and (b) 53 nm GaAs/120 nm Ge/(001)GaAs ($rms = 2.18$ nm) grown at two step growth process where top 50 nm GaAs was grown at 500 °C and 3 nm grown at 350 °C using migration enhanced epitaxy. In both cases, Ge epitaxial film was grown at 450 °C in an arsenic-free environment. The line profiles along the $\langle 110 \rangle$ direction are also included.

D. Strain relaxation properties of GaAs/Ge/GaAs heterostructure

To determine the structural quality and relaxation state of Ge epitaxial film and the GaAs/Ge/GaAs double heterostructure, high-resolution triple crystal x-ray (004) rocking curves were recorded. Figure 5 shows a rocking curve from the (004) Bragg lines of 3 nm GaAs/150 nm Ge/(001) GaAs double heterostructure where the epitaxial Ge layer thickness is significantly lower than the critical layer thickness [$\sim 1.8 \mu\text{m}$ (Ref. 60)]. The angular separation, $\Delta\theta$ between the (004) diffraction peaks of Ge and GaAs resulting from the difference in lattice plane spacing, $\Delta d/d$ along with their diffraction line profiles, provided information about the microstructural quality of the Ge film. The $\Delta\theta$ and the relative lattice mismatch are related by the following equation:

$$\left(\frac{\Delta a}{a}\right)_{\perp} = \left(\frac{\Delta d}{d}\right) = -\frac{2 \sin\left(\frac{\Delta\theta}{2}\right)}{\tan \theta},$$

where $(\Delta a/a)_{\perp}$ is the fractional change in the lattice constant and θ is the Bragg angle for the (004) plane. The

average peak separation between the Ge epilayer and the GaAs substrate is about 145 arc sec. The Ge layer peak appearing on the left side of the GaAs substrate peak confirmed that Ge epilayer lattice constant is higher than that of the GaAs. The appearance of Pendellösung oscillation fringes on both sides of Ge and GaAs peaks implies a parallel and very sharp heterointerface present in this structure. This interference originates from the beating of two x-ray wave fields inside of a crystal. One of the wave fields is generated at the interface between the GaAs and Ge as well as another wave field on the surface of the Ge layer. As a result, interference can only be observed in crystals that have almost perfectly parallel boundaries.⁶¹ The angular position of the Ge diffraction peak is the same as the pseudomorphic position of a Ge layer grown on GaAs.³⁵ The angular separation of the relaxed Ge and the GaAs substrate is ~ 97 arc sec.⁴⁹ If there is presence of either As or Ga atoms inside the epitaxial Ge layer, the angular separation between the reflection peaks of Ge epilayer and the GaAs substrate will significantly increase compared to 145 arc sec due to the increase of Ge lattice constant.³⁵ Hence, we can conclude that the Ge

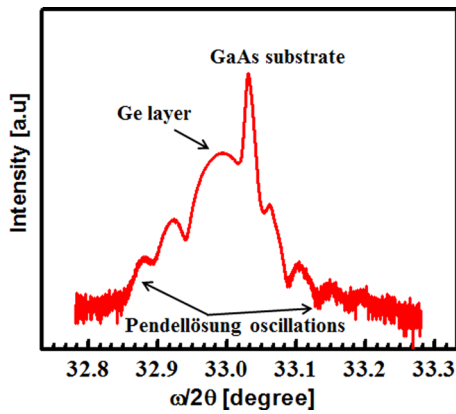


Fig. 5. (Color online) X-ray rocking curve from the (004) reflection of 3 nm GaAs/150 nm Ge/(001)GaAs heterostructure. The Pendellösung oscillations in the rocking curve confirm the high crystalline quality of Ge epilayer.

epitaxial film is pseudomorphic and the interface is abrupt that produces intensity oscillations.

The relaxation state of Ge layer was obtained from symmetric (004) and asymmetric (115) reflections of reciprocal space maps (RSMs) measured using triple axis x-ray diffraction. Figures 6(a) and 6(b) show the RSMs for (004) and (115) reflections obtained from a 3 nm GaAs/150 nm Ge/GaAs heterostructure. The RSMs exhibit two distinct

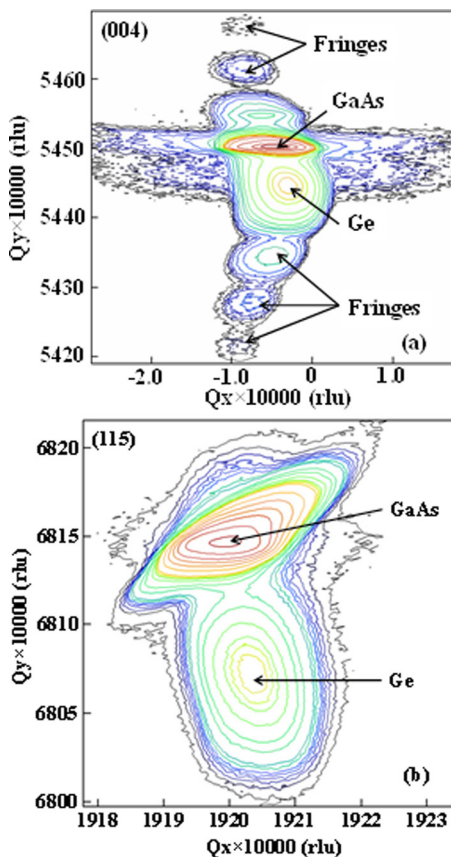


Fig. 6. (Color online) (a) Symmetric (004) and (b) asymmetric (115) RSMs of 3 nm GaAs/150 nm Ge/(001)GaAs (6° offcut toward [110] direction) double heterostructure. The RSMs are plotted in reciprocal space coordinates and each epilayer peak corresponding to reciprocal lattice point is indicated in this figure.

reciprocal lattice point (RLP) maxima and the peak assignments corresponding to those RLP maxima are from (i) the GaAs substrate and (ii) the Ge epilayer. The thickness fringes are clearly visible from this heterostructure. One can find from these RSMs that the thickness of the fringes as shown in Fig. 5 associated with a thin layer now become contours of intensity, the maxima of which run along a line normal to the specimen surface. As the substrate surface was 6° offcut from the [001] direction, the line of the interface maxima does not coincide with the Q_y direction. From these RSMs, one can determine the lattice parameter in the out-of-plane (growth direction), a_\perp (from the symmetric reflection), and the lattice parameter in the growth plane, a_\parallel (from the asymmetric reflection). The degree of relaxation of the Ge layer can be calculated from the measured lattice parameters and the Poisson's ratio with respect to GaAs substrate. Using RSMs from Fig. 6, the measured lattice constants along the out-of-plane and in-plane directions of the Ge layer were found to be 5.6597 \AA and 5.6536 \AA , respectively. With this information, the degree of relaxation⁶² of the 150 nm Ge layer was limited to only 5%, which is expected since the critical layer thickness of Ge is about $1.8 \mu\text{m}$. We can conclude from the minimal relaxation and the thickness fringes observed here that the quality of the GaAs/Ge/GaAs heterostructure can be used for the *p*-channel Ge quantum well field effect transistor application.

E. Photoluminescence properties of Ge/(001)GaAs

In order to determine the direct bandgap emission from Ge epitaxial layer, room temperature photoluminescence spectrum was taken on the Ge/GaAs structure. Figure 7 shows the 300 K PL spectrum of 120 nm Ge epilayer grown on (001) GaAs (6° off toward [110] direction) in an arsenic-free environment. The PL peaks at bandgap of $E_g = 0.783 \text{ eV}$, within an experimental error, corresponding to a wavelength of $\lambda = 1583 \text{ nm}$, reveals that the electrons in Γ valley recombine with holes in the valence band at room temperature.^{41,42} A shift of 23 nm peak as compared to relaxed Ge is observed, where the direct bandgap recombination of relaxed Ge peaks

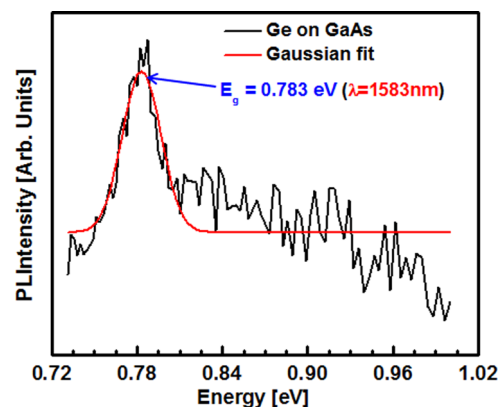


Fig. 7. (Color online) Room temperature photoluminescence spectrum from the 120 nm thick Ge film grown on (001) GaAs 6° offcut toward [110] direction substrate. The direct bandgap emission of the Ge peaks at 0.783 eV ($\lambda = 1583 \text{ nm}$). The direct bandgap recombination of relaxed Ge peaks at 1550 nm (not shown).

at 1550 nm. The direct radiative transition rate is about 1600 times that of the indirect transition at higher power excitation and, hence, only the direct band-to-band transition was observed in room temperature PL measurement. Thus, the photoluminescence is indicative of the quality of Ge epitaxial layer grown on GaAs substrate and is not intended to address the interface properties in our work presented here.

F. SIMS depth profiles of GaAs/Ge/GaAs heterostructure

Dynamic SIMS depth profile was also used to determine the extent of chemical diffusion or reaction at GaAs/Ge/GaAs interfaces. Such interactions can take place due to thermodynamic driving forces, especially at growth temperature. Higher growth temperature promotes movement of atoms across surfaces as well as interfaces. In the case of GaAs/Ge/GaAs heterostructure for which the optimum growth temperatures of each layer were different. The growth of Ge layer at lower temperature ($\sim 450^\circ\text{C}$) is followed by growth of the upper GaAs layer at both 350°C and 500°C . Figure 8 shows the Ga, As, and Ge depth profiles of the GaAs/Ge/GaAs double heterostructure in which Ge and GaAs layers were grown in separate MBE chambers. All depth profiles illustrate constant Ga, As, and Ge intensities within each layer, indicating good growth uniformity. Besides, the depth profiles display an abrupt Ge/GaAs bottom heterointerface, a transition between Ge/GaAs of less than 15 nm, within the sputter-induced broadening of the ion beam, indicating low value of Ga, As, and Ge intermixing at the Ge/GaAs bottom interface. Thus, dynamic SIMS spectra underscore the delicate balance between growth conditions and interface intermixing at the GaAs/Ge/GaAs double heterostructure.

G. Band offset properties of GaAs/Ge/GaAs heterointerfaces

There is no unique value for the band offset of GaAs/Ge/GaAs heterojunction and experiments must therefore

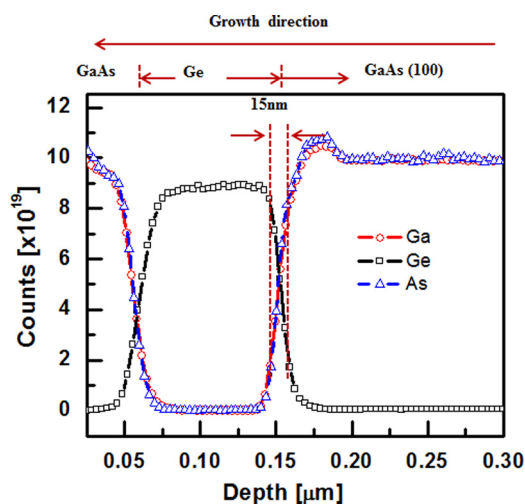


Fig. 8. (Color online) Cs^+ SIMS depth profile of GaAs/Ge/GaAs double heterostructure. Arrow indicates the interface broadening at the Ge/GaAs heterointerface.

provide better insight into structure-property correlations for *in situ* grown Ge in an arsenic-free environment for GaAs/Ge/GaAs heterojunction using separate MBE chambers for Ge and GaAs epitaxial layers. As we know that the two semiconductors having different bandgap results in band discontinuities when in contact and these offsets play a crucial role in the electrical transport properties of the heterojunction. The transport properties of all heterojunction devices strongly depend on three interface characteristics: band discontinuities, interface states, and potential-barrier height. The change in the forbidden gap across the heterointerface is distributed between a valence-band discontinuity, ΔE_v , and a conduction-band discontinuity, ΔE_c . These discontinuities may form barriers for the charge carriers crossing the interface and dramatically influence the properties of heterojunction devices like quantum well FETs and tunnel FETs. Most theoretical treatments of heterojunction band lineups have assumed abrupt, lattice-matched interfaces. Likewise, most assume that there is an absolute energy associated with each semiconductor so that the band offsets reflect differences in those energies. Experimentally, however, it has been observed that the electrical properties can be related to the chemical and geometric structure at the interface and can be dictated by deviations from perfection.^{26,39,63} In particular, band offsets can depend on such variables as substrate orientation, overlayer crystallinity, the order of deposition (i.e., Ge on GaAs or GaAs on Ge), surface reconstruction, deposition temperature, deposition rate, microscopic interface dipole, and interdiffusion or reactivity. In particular, offset variations up to ~ 0.9 eV due to microscopic interface dipoles are expected for polar interface of lattice matched Ge/GaAs (100) junction. These dipoles originate from oriented pairs of atoms at the interface.⁶⁴ Experimentally, mainly x-ray photoemission experiments have been performed to study dipole contributions to the band lineup.⁶⁵ Grant *et al.*²⁶ found that ΔE_v varying from 0.3 eV to 0.66 eV for (001) GaAs surfaces and measured a difference in ΔE_v between the polar (100) and the nonpolar Ge/(110)GaAs interface of ~ 0.1 eV. On the other hand, Katnani *et al.*^{66,67} reported a value of $\Delta E_v = 0.47$ eV, within experimental error, for Ge/GaAs interfaces regardless of several different initial GaAs surface reconstructions and ΔE_v did not depend on the crystallographic configuration.

The valence band offset, ΔE_v , at the GaAs/Ge and Ge/GaAs heterointerfaces was determined using XPS system with monochromatic Al-K α x-ray source (1486.6 eV) and a 45° exit angle, an angle integrated photoelectron energy distribution curve for the valence band maximum (VBM) and As 3d, Ga 3d, and Ge 3d core levels spectra were recorded. All the samples were mounted on a sample stage and transferred to an XPS system through an ultra-high vacuum transfer stage. The binding energy was corrected by adjusting the C 1s core-level peak position to 285.0 eV for each sample surface. Using this approach, the XPS spectra were recorded from the following four samples: GaAs wafer, thin Ge on GaAs substrate, thick Ge on GaAs substrate, and thin GaAs on Ge/(001)GaAs. Figure 9 shows XPS spectra of (a) As 3d

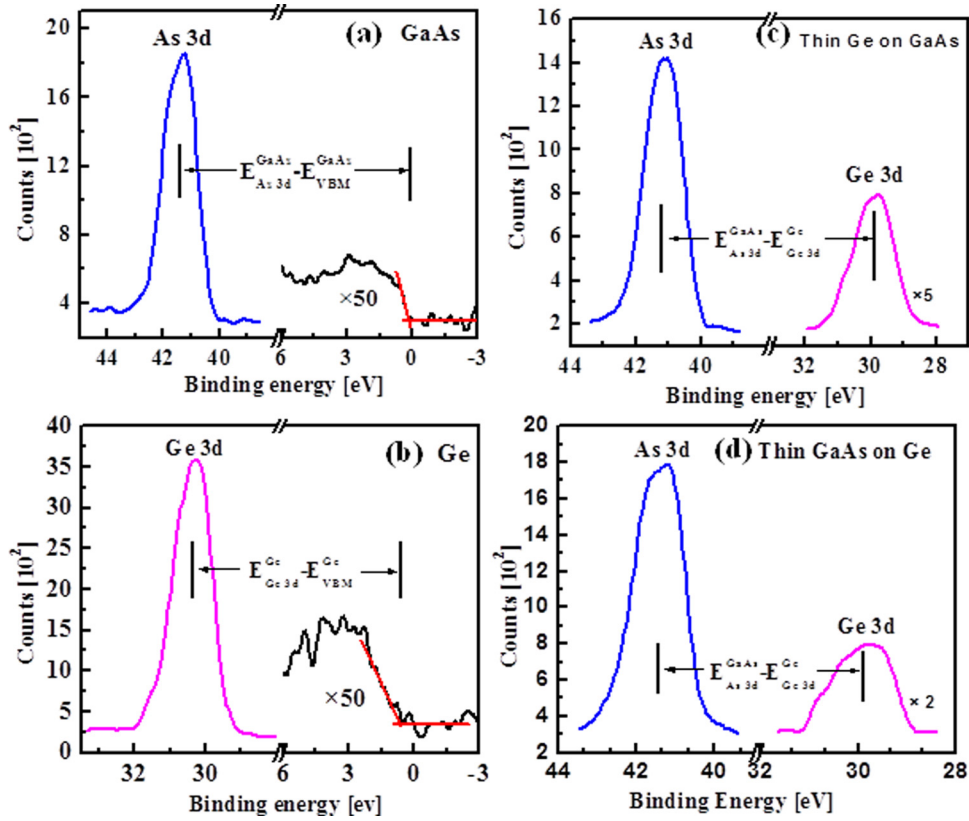


FIG. 9. (Color online) XPS spectra of (a) As 3d core level (E_{As3d}^{GaAs}) and valence band maximum VBM (E_{VBM}^{GaAs}) of GaAs film; (b) As 3d core level (E_{As3d}^{GaAs}) and Ge 3d core level (E_{Ge3d}^{Ge}) at thin Ge/GaAs interface; (c) Ge 3d core level (E_{Ge3d}^{Ge}) and VBM (E_{VBM}^{Ge}) of thick Ge film; and (d) As 3d core level (E_{As3d}^{GaAs}) and Ge 3d core level (E_{Ge3d}^{Ge}) at thin GaAs/Ge interface.

core level (E_{As3d}^{GaAs}) and VBM (E_{VBM}^{GaAs}) of GaAs film; (b) As 3d core level (E_{As3d}^{GaAs}) and Ge 3d core level (E_{Ge3d}^{Ge}) at thin Ge/GaAs interface; (c) Ge 3d core level (E_{Ge3d}^{Ge}) and VBM (E_{VBM}^{Ge}) of thick Ge film; and (d) As 3d core level (E_{As3d}^{GaAs}) and Ge 3d core level (E_{Ge3d}^{Ge}) of thin GaAs/Ge interface. The bottom Ge/(001)GaAs interface valence band offset value, ΔE_V^{Bottom} , was determined with the following equation:²⁷

$$\begin{aligned} \Delta E_V^{Bottom}(Ge/GaAs) &= (E_{As3d}^{GaAs} - E_{VBM}^{GaAs})^{GaAs} \\ &\quad - (E_{Ge3d}^{Ge} - E_{VBM}^{Ge})^{Ge} \\ &\quad - (E_{As3d}^{GaAs} - E_{Ge3d}^{Ge})^{interface} \\ &= 0.40 \pm 0.05 \text{ eV}, \end{aligned}$$

where ΔE_V is determined from the difference between As 3d core level (E_{As3d}^{GaAs}) and VBM (E_{VBM}^{GaAs}) of GaAs wafer, As 3d core level (E_{As3d}^{GaAs}) and Ge 3d core level (E_{Ge3d}^{Ge}) at thin Ge/(001)GaAs heterointerface, Ge 3d core level (E_{Ge3d}^{Ge}) and VBM (E_{VBM}^{Ge}) for thick Ge film. Similarly, the upper heterointerface GaAs/Ge valence band offset, ΔE_V^{Top} can be determined from the following equation,²⁷ where the As 3d core level (E_{As3d}^{GaAs}) and VBM (E_{VBM}^{GaAs}) of thick GaAs layer, As 3d core level (E_{As3d}^{GaAs}) and Ge 3d core level (E_{Ge3d}^{Ge}) at thin GaAs/Ge(001) heterointerface, Ge 3d core level (E_{Ge3d}^{Ge}) and VBM (E_{VBM}^{Ge}) for thick Ge film:

$$\begin{aligned} \Delta E_V^{Top}(GaAs/Ge) &= (E_{As3d}^{GaAs} - E_{VBM}^{GaAs})^{GaAs} \\ &\quad - (E_{Ge3d}^{Ge} - E_{VBM}^{Ge})^{Ge} \\ &\quad - (E_{As3d}^{GaAs} - E_{Ge3d}^{Ge})^{interface} \\ &= 0.20 \pm 0.05 \text{ eV}. \end{aligned}$$

The results obtained from analysis of this data shown in Fig. 9 are also presented in Table II. The present value of measured ΔE_V of the bottom Ge/GaAs and upper GaAs/Ge heterointerfaces is an excellent agreement with the experimental results obtained by Katnani *et al.*,^{66,67} Sorba *et al.*,⁶⁸ Biasiol *et al.*,⁴⁵ and theoretical prediction by Harrison⁶⁹ and Cardona and Christensen.⁷⁰ Most experimental Ge/(001) GaAs ΔE_V data are in the 0.4 eV–0.7 eV range, but the spread of the experimental values is quite substantial and the average ΔE_V is 0.55 ± 0.13 eV, where the quoted error is the standard deviation. It is surprising to see that the measured ΔE_V for Ge on (001)GaAs is in wide range, especially in view of the fact that most of the data were obtained for a well characterized epitaxial system and it is a nonpolar on polar epitaxy where the heterojunction is thought to be abrupt and of high-quality. Also, it is quite clear from the wide range of band offset values reported for Ge/(001)GaAs heterojunction prepared under different conditions that the detailed atomic structure of the Ge/GaAs interface can have a substantial effect on band offset values. The dependence of the Ge/(001)GaAs ΔE_V on growth conditions such as same

TABLE II. Core-level to VBM binding-energy difference for Ge and GaAs.

Material and interface	Binding energy difference	Measured valence band offset, ΔE_V of GaAs/Ge/GaAs (001)	
		Bottom Ge/GaAs (001) interface	Top GaAs/Ge interface
GaAs	$E_{As3d}^{GaAs} - E_{VBM}^{GaAs} = 41.15 \pm 0.05$ eV		
Thin Ge on GaAs	$E_{As3d}^{GaAs} - E_{Ge3d}^{Ge} = 11.60 \pm 0.05$ eV	0.40 ± 0.05 eV	
Thick Ge	$E_{Ge3d}^{Ge} - E_{VBM}^{Ge} = 29.75 \pm 0.05$ eV		
Thin GaAs on Ge	$E_{As3d}^{GaAs} - E_{Ge3d}^{Ge} = 11.40 \pm 0.05$ eV		0.20 ± 0.05 eV
GaAs	$E_{As3d}^{GaAs} - E_{VBM}^{GaAs} = 41.15 \pm 0.05$ eV		

chamber for both Ge and GaAs layers growth, growth temperature, surface reconstruction, and doping may be responsible for the wide range of experimental ΔE_V reported in supposedly abrupt Ge/(001)GaAs heterojunction.

A great deal of attention has been devoted to the determination of ΔE_V of Ge on GaAs heterojunction; however, minimal work has been done on the determination of the band offset of GaAs/Ge. It was due to the more challenging polar-on-nonpolar epitaxy of GaAs/Ge heterojunction. When GaAs is epitaxially grown on the (001)Ge substrate without any off-orientation, the APDs mostly occur at the interface, and to prepare a APD-free GaAs/Ge heterostructure, we must account for the off-cut substrate, as shown in Fig. 3. Furthermore, when GaAs is epitaxially grown on the Ge surface, the interdiffusion must be controlled. Moreover, Ge surfaces after deposition on GaAs substrate demonstrate a spectrum of surface reconstructions and the preferred Ge surface orientation is (2×2) , as discussed above. It was assumed that the surface off-orientation of the Ge is the same as the starting GaAs substrate since the Ge epilayer was deposited using MBE growth process. Clean GaAs surfaces demonstrate a spectrum of reconstruction that are either Ga or As rich. This could contribute to the quality of the Ge layer at different deposition temperature. The growth mechanisms for thin Ge films on GaAs have been studied rather extensively. It was shown that Ge films grown on (001)GaAs fall under layer-by-layer (Frank-van der

Merwe) mode at temperatures $<400^\circ\text{C}$, whereas at higher temperatures growth is by island mechanisms (Stranski-Krastanov).⁷¹ In our case, the lower growth temperature and lower growth rate using MEE during MBE growth process was used to prevent the formation of APDs in the upper GaAs layer as well as to prevent interdiffusion. Using such a process, the measured ΔE_V of the upper GaAs/Ge heterointerface was found to be 0.20 ± 0.05 eV, which is in agreement with the experimental results by Sorba *et al.*⁶⁸ and theoretically by Biasiol *et al.*⁴⁵ Figure 10 shows the schematic band alignment based on the reported bandgap values of GaAs and Ge, calculated conduction band offset ΔE_C from $\Delta E_g = \Delta E_V + \Delta E_C$, and the present result of ΔE_V by XPS from this work. Thus, comparison of band offset between experiment and theory is undoubtedly exciting and our *in situ* grown Ge in an As-free environment for GaAs/Ge/(001)GaAs heterostructure with proper surface offcut using MBE provide a promising path for *p*-channel quantum well field effect transistor applications. To prevent the carrier spill-off to the upper barrier layer due to the lower ΔE_V at the top GaAs/Ge interface compared to Ge/GaAs bottom interface, composite high-*k* dielectric (e.g., Al_2O_3 , HfO_2 , TaSiO_x) on upper GaAs would enable high-performance *p*-channel Ge quantum well FETs for low-power and high-speed computing platform.

IV. SUMMARY AND CONCLUSIONS

In conclusion, we have shown that the high-quality epitaxial Ge in an arsenic-free environment for GaAs/Ge/GaAs heterostructures can be grown *in situ* using two separate molecular beam epitaxy chambers, confirmed by RHEED intensity oscillation and x-ray diffraction. AFM microscopy reveals smooth and uniform morphology and room temperature photoluminescence spectroscopy confirmed direct bandgap emission at 1583 nm. Dynamic SIMS depth profiles of Ga, As, and Ge display a low value of Ga, As, and Ge intermixing at the Ge/GaAs interface. The valence band offset at the upper GaAs/Ge and bottom Ge/GaAs heterointerface of GaAs/Ge/GaAs double heterostructure is 0.20 eV and 0.40 eV, respectively, which is consistent with the theoretical values. Thus, the high-quality heterointerface and band offset for carrier confinement obtained in MBE grown GaAs/Ge/GaAs heterostructures can offer a promising virtual substrate technology integrated on Si substrate for extending the performance and application of Ge-based *p*-channel

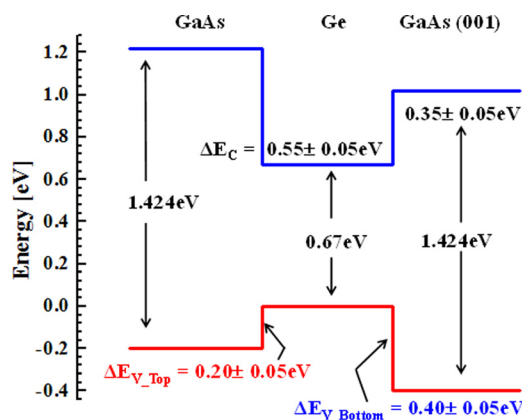


FIG. 10. (Color online) Schematic band alignment of the GaAs/Ge/(001)GaAs double heterostructure based on the measured ΔE_V using XPS. The conduction band discontinuity, ΔE_C was calculated based on the measured ΔE_V and the difference in bandgap of GaAs and Ge, where $\Delta E_g = \Delta E_V + \Delta E_C$.

high-hole mobility MOSFET and quantum well field effect transistors.

ACKNOWLEDGMENTS

This work is supported in part by Intel Corporation and the Institute for Critical Technology and Applied Sciences (ICTAS) at Virginia Tech.

- ¹R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, *Nature Mater.* **6**, 810 (2007).
- ²M. K. Hudait, *ECS Trans.* **45**, 581 (2012).
- ³M. K. Hudait *et al.*, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)*, Washington DC, 10–12 December 2007 (IEEE, New York, 2007), p. 625.
- ⁴M. Radosavljevic *et al.*, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)*, Baltimore, 7–9 December 2009 (IEEE, New York, 2009), p. 319.
- ⁵L. Ming, L. Haiou, T. Chak Wah, and L. Kei May, *IEEE Electron. Device Lett.* **33**, 498 (2012).
- ⁶M. Radosavljevic *et al.*, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)*, San Francisco, 14–17 December 2008 (IEEE, New York, 2008), p. 727.
- ⁷A. Nainani *et al.*, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)*, Baltimore, 7–9 December 2009 (IEEE, New York, 2009), p. 857.
- ⁸J. B. Boos *et al.*, *IEICE Trans. Electron.* **E91-C**, 1050 (2008).
- ⁹J. F. Klem, J. A. Lott, J. E. Schirber, S. R. Kurtz, and S. Y. Lin, *J. Electron. Mater.* **22**, 315 (1993).
- ¹⁰C. Liao and K. Y. Cheng, *J. Vac. Sci. Technol. B* **28**, C3C29 (2010).
- ¹¹B. R. Bennett, M. G. Ancona, and J. B. Boos, *MRS Bull.* **34**, 530 (2009).
- ¹²L. F. Luo, K. F. Longenbach, and W. I. Wang, *Electron. Lett.* **27**, 472 (1991).
- ¹³M. Jaffe, J. E. Oh, J. Pamulapati, J. Singh, and P. Bhattacharya, *Appl. Phys. Lett.* **54**, 2345 (1989).
- ¹⁴M. Jaffe, Y. Sekiguchi, and J. Singh, *Appl. Phys. Lett.* **51**, 1943 (1987).
- ¹⁵J. M. Hinckley and J. Singh, *Appl. Phys. Lett.* **53**, 785 (1988).
- ¹⁶M. V. Fischetti and S. E. Laux, *J. Appl. Phys.* **80**, 2234 (1996).
- ¹⁷A. Saha and M. K. Hudait (unpublished).
- ¹⁸R. R. King, *Nat. Photonics* **2**, 284 (2008).
- ¹⁹M. Zhu, H. C. Chin, G. S. Samudra, and Y. C. Yeo, *J. Electrochem. Soc.* **155**, H76 (2008).
- ²⁰S. H. Tang, C. I. Kuo, H. D. Trinh, M. K. Hudait, E. Y. Chang, C. Y. Hsu, Y. H. Su, G.-L. Luo, and H. Q. Nguyen, *Microelectron. Eng.* **92**, 16 (2012).
- ²¹A. Christou, W. T. Anderson, J. E. Davey, M. L. Bark, and Y. Anand, *Electron. Lett.* **16**, 254 (1980).
- ²²V. F. Mitin, V. V. Kholevchuk, and B. P. Kolodych, *Cryogenics* **51**, 68 (2011).
- ²³V. F. Mitin, Y. A. Tkhonik, and E. F. Venger, *Microelectron. J.* **28**, 617 (1997).
- ²⁴N. Chand, J. Klem, and H. Morkoc, *Appl. Phys. Lett.* **48**, 484 (1986).
- ²⁵R. Pillarisetty *et al.*, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)*, San Francisco, 6–8 December 2010 (IEEE, New York, 2010), p. 150.
- ²⁶R. W. Grant, J. R. Waldrop, and E. A. Kraut, *J. Vac. Sci. Technol.* **15**, 1451 (1978).
- ²⁷E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Kowalczyk, *Phys. Rev. Lett.* **44**, 1620 (1980).
- ²⁸E. T. Yu, J. O. McCaldin, and T. C. McGill, *Solid State Phys.* **46**, 1 (1992).
- ²⁹A. Franciosi and C. G. Van de Walle, *Surf. Sci. Rep.* **25**, 1 (1996).
- ³⁰H. D. Trinh *et al.*, *Appl. Phys. Lett.* **97**, 042903 (2010).
- ³¹M. K. Hudait, Y. Lin, M. N. Palmisiano, C. Tivarus, J. P. Pelz, and S. A. Ringel, *J. Appl. Phys.* **95**, 3952 (2004).
- ³²A. K. Baraskar, M. A. Wistey, V. Jain, U. Singiseti, G. Burek, B. J. Thibeault, Y. J. Lee, A. C. Gossard, and M. J. W. Rodwell, *J. Vac. Sci. Technol. B* **27**, 2036 (2009).
- ³³C. A. Chang, *J. Appl. Phys.* **53**, 1253 (1982).
- ³⁴C. A. Chang, *Appl. Phys. Lett.* **40**, 1037 (1982).
- ³⁵B. Salazar-Hernández, M. A. Vidal, H. Navarro-Contreras, and C. Vázquez-López, *Thin Solid Films* **352**, 269 (1999).
- ³⁶E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Kowalczyk, *Phys. Rev. B* **28**, 1965 (1983).
- ³⁷J. H. Neave, P. K. Larsen, B. A. Joyce, J. P. Gowers, and J. F. Vanderveen, *J. Vac. Sci. Technol. B* **1**, 668 (1983).
- ³⁸R. A. Stall, C. E. C. Wood, K. Board, N. Dandekar, L. F. Eastman, and J. Devlin, *J. Appl. Phys.* **52**, 4062 (1981).
- ³⁹R. S. Bauer and J. C. Mikkelsen, *J. Vac. Sci. Technol.* **21**, 491 (1982).
- ⁴⁰X.-S. Wang, K. Self, V. Bressler-Hill, R. Maboudian, and W. H. Weinberg, *Phys. Rev. B* **49**, 4775 (1994).
- ⁴¹S. H. Tang, E. Y. Chang, M. K. Hudait, J. S. Maa, C. W. Liu, G. L. Luo, H. D. Trinh, and Y. H. Su, *Appl. Phys. Lett.* **98**, 161905 (2011).
- ⁴²Y. Bai, M. T. Bulsara, and E. A. Fitzgerald, *J. Appl. Phys.* **111**, 013502 (2012).
- ⁴³M. Bosi and G. Attolini, *Prog. Cryst. Growth Charact. Mater.* **56**, 146 (2010).
- ⁴⁴A. Franciosi, L. Sorba, G. Bratina, and G. Biasiol, *J. Vac. Sci. Technol. B* **11**, 1628 (1993).
- ⁴⁵G. Biasiol, L. Sorba, G. Bratina, R. Nicolini, A. Franciosi, M. Peressi, S. Baroni, R. Resta, and A. Baldereschi, *Phys. Rev. Lett.* **69**, 1283 (1992).
- ⁴⁶M. Bosi, G. Attolini, C. Ferrari, C. Frigeri, M. Calicchio, F. Rossi, V. Kalman, C. Attila, and Z. Zsolt, *J. Cryst. Growth* **318**, 367 (2011).
- ⁴⁷S. A. Ringel *et al.*, *Prog. Photovoltaics* **10**, 417 (2002).
- ⁴⁸G. P. Srivastava, *Rep. Prog. Phys.* **60**, 561 (1997).
- ⁴⁹W. G. Schmidt, S. Mirbt, and F. Bechstedt, *Phys. Rev. B* **62**, 8087 (2000).
- ⁵⁰M. C. Payne, M. Needels, and J. D. Joannopoulos, *J. Phys.: Condens Matter* **1**, SB63 (1989).
- ⁵¹S. Kevan, *Phys. Rev. B* **32**, 2344 (1985).
- ⁵²H. Kroemer, *J. Cryst. Growth* **81**, 193 (1987).
- ⁵³C. A. Chang and T. S. Kuan, *J. Vac. Sci. Technol. B* **1**, 315 (1983).
- ⁵⁴Q. K. Xue, T. Hashizume, and T. Sakurai, *Prog. Surf. Sci.* **56**, 1 (1997).
- ⁵⁵R. M. Sieg, S. A. Ringel, S. M. Ting, E. A. Fitzgerald, and R. N. Sacks, *J. Electron Mater.* **27**, 900 (1998).
- ⁵⁶W. A. Harrison, E. A. Kraut, J. R. Waldrop, and R. W. Grant, *Phys. Rev. B* **18**, 4402 (1978).
- ⁵⁷K. Kunc and R. M. Martin, *Phys. Rev. B* **24**, 3445 (1981).
- ⁵⁸M. K. Hudait and S. B. Krupanidhi, *J. Appl. Phys.* **89**, 5972 (2001).
- ⁵⁹R. Fischer, H. Morkoc, B. A. Neuman, H. Zabel, C. Choi, N. Otsuka, M. Longebone, and L. P. Erickson, *J. Appl. Phys.* **60**, 1640 (1986).
- ⁶⁰A. Navarro-Quezada, A. G. Rodríguez, M. A. Vidal, G. Hernández-Sosa, and H. Navarro-Contreras, *Revista Superficies y Vacío* **16**, 42 (2003).
- ⁶¹W. T. Stacy and M. M. Janssen, *J. Cryst. Growth* **27**, 282 (1974).
- ⁶²M. K. Hudait, Y. Lin, and S. A. Ringel, *J. Appl. Phys.* **105**, 061643 (2009).
- ⁶³J. R. Waldrop, S. P. Kowalczyk, R. W. Grant, E. A. Kraut, and D. L. Miller, *J. Vac. Sci. Technol.* **19**, 573 (1981).
- ⁶⁴Y.-C. Ruan and W. Y. Ching, *J. Appl. Phys.* **62**, 2885 (1987).
- ⁶⁵A. D. Katnani and G. Margaritondo, *Phys. Rev. B* **28**, 1944 (1983).
- ⁶⁶A. D. Katnani, P. Chiaradia, H. W. Sang, and R. S. Bauer, *J. Vac. Sci. Technol. B* **2**, 471 (1984).
- ⁶⁷A. D. Katnani, P. Chiaradia, J. Sang, H. W. P. Zurcher, and R. S. Bauer, *Phys. Rev. B* **31**, 2146 (1985).
- ⁶⁸L. Sorba, G. Biasiol, G. Bratina, R. Nicolini, and A. Franciosi, *J. Cryst. Growth* **127**, 93 (1993).
- ⁶⁹W. A. Harrison, *J. Vac. Sci. Technol.* **14**, 1016 (1977).
- ⁷⁰M. Cardona and N. E. Christensen, *Phys. Rev. B* **35**, 6182 (1987).
- ⁷¹X.-S. Wang, K. Self, and W. H. Weinberg, *J. Vac. Sci. Technol. A* **12**, 1920 (1994).