

Structural, morphological, and band alignment properties of GaAs/Ge/GaAs heterostructures on (100), (110), and (111)A GaAs substrates

Mantu K. Hudait,^{a)} Yan Zhu, and Nikhil Jain

Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, Virginia 24061

Jerry L. Hunter, Jr.

Nanoscale Fabrication and Characterization Laboratory, Institute for Critical Technology and Applied Science, Virginia Tech, Blacksburg, Virginia 24061

(Received 12 September 2012; accepted 21 November 2012; published 12 December 2012)

Structural, morphological, and band offset properties of GaAs/Ge/GaAs heterostructures grown *in situ* on (100), (110), and (111)A GaAs substrates using two separate molecular beam epitaxy chambers, connected via vacuum transfer chamber, were investigated. Reflection high energy electron diffraction (RHEED) studies in all cases exhibited a streaky reconstructed surface pattern for Ge. Sharp RHEED patterns from the surface of GaAs on epitaxial Ge/(111)A GaAs and Ge/(110)GaAs demonstrated a superior interface quality than on Ge/(100)GaAs. Atomic force microscopy reveals smooth and uniform morphology with surface roughness of Ge about 0.2–0.3 nm. High-resolution triple axis x-ray rocking curves demonstrate a high-quality Ge epitaxial layer as well as GaAs/Ge/GaAs heterostructures by observing Pendellösung oscillations. Valence band offset, ΔE_v , have been derived from x-ray photoelectron spectroscopy (XPS) data on GaAs/Ge/GaAs interfaces for three crystallographic orientations. The ΔE_v values for epitaxial GaAs layers grown on Ge and Ge layers grown on (100), (110), and (111)A GaAs substrates are 0.23, 0.26, 0.31 eV (upper GaAs/Ge interface) and 0.42, 0.57, 0.61 eV (bottom Ge/GaAs interface), respectively. Using XPS data obtained from these heterostructures, variations in band discontinuities related to the crystallographic orientation have been observed and established a band offset relation of $\Delta E_v(111)Ga > \Delta E_v(110) > \Delta E_v(100)As$ in both upper and lower interfaces. © 2013 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4770070>]

I. INTRODUCTION

With continued transistor scaling, new channel materials and device architectures are needed for transistor miniaturization and to enhance transistor performance.¹ According to the International Technology Roadmap for Semiconductors (ITRS),² new channel materials with superior transport properties are required for further increases in transistor drive current and resultant ULSI performance improvement, in addition to metal gate/high- k gate dielectric and multi-gate transistor configuration in a CMOS logic device under 10 nm regime. $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($0.53 \leq x \leq 1$) with high electron mobility and low effective mass has been demonstrated as n-channel quantum well (QW) device configuration on Si substrate operating at 0.5 V;^{3–7} however, the demonstration of a high hole mobility and high-performance p-channel device within the same material system with similar performance remains elusive to date due to low hole mobility in III–V materials. For this reason, the enhancement of carrier transport properties in the channel using high hole mobility channel materials,^{8–10} different surface orientations to improve the carrier mobility,^{11–16} strain engineering during growth and process induced strain,^{11,16–18} device architecture,^{8–10} and optimal channel direction^{19–23} have been proposed for further enhancement of CMOS devices. For example, Si p-channel metal-oxide semiconductor field-effect transistor (MOSFET) exhibits the highest hole

mobility along the $\langle 110 \rangle$ channel direction on (110)-oriented Si substrates due to the lowest effective mass of holes along the $\langle 110 \rangle$ direction.^{24–27} Very recently, it has been demonstrated that the carrier mobility of Ge MOSFETs can be enhanced by utilizing a Ge channel with different orientations; the carrier mobility was expected to be high in (111)Ge for electrons²⁸ and in (110)Ge for holes.²² In fact, transistors fabricated on (111)Ge substrates exhibited higher electron mobilities of $\sim 1100 \text{ cm}^2/\text{Vs}$ ²⁹ and hole mobilities of $\sim 650 \text{ cm}^2/\text{Vs}$ on (110)Ge substrate along $\langle 110 \rangle$ direction.¹⁸ According to Yang *et al.*,¹⁹ the electron mobility of Ge with (111) orientation is $1.8\times$ higher than the electron mobility of Ge with (100) and (110) orientations. Furthermore, Dissanayake *et al.*²⁰ shows that the hole mobility of (110) Ge channel orientation along the $\langle 110 \rangle$ direction exhibited $2.3\times$ higher hole mobility compared with the (100) Ge surface. Thus, germanium has received a great deal of attention as a p-channel channel material for next generation low-power MOSFETs due to its larger bulk hole mobility than Si or any of the III–V materials.

Even though significant research has been reported on (110)Ge and (111)Ge substrates for boosting hole mobility and electron mobility, respectively, the detailed growth, structural properties, and band alignment properties of the epitaxial Ge on large band gap different off-oriented substrates are required for a predefined channel thickness in high performance CMOS devices. In fact, the ultimate extremely high mobility CMOS logic device can be achieved using a combination of n-channel III–V n-MOSFET (or

^{a)}Electronic mail: mantu.hudait@vt.edu

quantum well FET) and p-channel Ge p-MOSFET (or quantum well FET) heterogeneously integrated on Si substrate.³⁰ Considering several material choices and strain engineering in the channel, Ge epitaxial films grown on a large bandgap GaAs material is of immense interest due to lattice match (mismatch $\sim 0.07\%$) which ensures larger critical thickness, lower dislocation density, and strain-free Ge epitaxial film. As a result, high-hole mobility of Ge and its narrow bandgap ($E_g = 0.67$ eV) make the GaAs/Ge heterojunction suitable for the fabrication of p-channel QW field effect transistors, solar cells,³¹ MOSFETs,^{32,33} and tunnel transistors.³⁴ Ge QW transistor structures on GaAs/Si with a GaAs upper barrier in a QW configuration are essential in order (i) to eliminate parallel conduction,^{2,3} (ii) to provide large valence band offset^{35–38} for hole confinement, (iii) to achieve high-quality high- k /III–V barrier interface with lower Dit,³⁹ (iv) to control lattice mismatch,³ (v) to have better interface properties, (vi) to provide modulation doping^{4,8} in the Ge QW structure, (vii) to control the OFF state leakage, and (viii) to improve Ohmic contact. In the past, only the band alignment properties of the discrete GaAs on Ge or Ge on GaAs heterointerfaces were reported and minimal work was reported on the band alignment properties of the GaAs/Ge/GaAs double heterostructure grown on (100), (110), and (111)A GaAs substrates. This paper presents a comprehensive study of the structural, morphological, and band alignment properties of epitaxial Ge and GaAs/Ge/GaAs heterostructures on (100)/6°, (110), and (111)A GaAs substrates grown by separate molecular beam epitaxy (MBE) growth chambers for Ge and III–V layers. The results from this experimental finding complement and are the first steps toward achieving high-performance Ge channel material on (110) GaAs for p-type QW field effect transistor and on (111)A GaAs for n-type QWFETs, respectively, which can ultimately heterogeneously integrate to Si substrates through a III–V buffer layer for the realization of ultralow power and high-speed CMOS logic applications.

II. EXPERIMENT

The undoped epitaxial Ge layer and GaAs/Ge/GaAs double heterostructures were grown by an *in situ* growth process on 6° offcut (100) toward the [110] direction, (110), and (111)A epi-ready GaAs substrates using separate solid source MBE growth chambers for Ge and III–V materials, connected *via* ultrahigh vacuum transfer chamber. Substrate oxide desorption was done at ~ 680 °C for (100)/6°-oriented GaAs, ~ 580 °C for (110)-oriented GaAs, and ~ 550 °C for (111)A-oriented GaAs substrates under an arsenic overpressure of $\sim 1 \times 10^{-5}$ Torr in a III–V MBE chamber. During the substrate oxide desorption, GaAs layer growth, and Ge layer after growth, reflection high energy electron diffraction (RHEED) patterns were recorded for each step of the growth process. An initial 0.2 μm thick undoped GaAs buffer layer was then deposited on each GaAs substrate to generate a smooth surface at 650, 550 and 500 °C for (100), (110), and (111)A, respectively, under a stabilized As₂ flux prior to transferring each GaAs wafer to the Ge MBE chamber for

Ge epilayer growth. Since the (100) GaAs is polar surface, the growth temperature for the homoepitaxy of GaAs on such surface can be higher than other crystallographic orientations. On the other hand, the growth temperature of GaAs on (110) GaAs should be lower than on (100) GaAs substrate due to the nonpolar surface (mixture of As and Ga atoms), and the required As₂/Ga flux ratio for a smooth surface is higher than that on (100) GaAs surface. By lowering the growth temperature, one can reduce the surface ad-atoms mobility of Ga and keeping the higher over pressure of As₂ can prevent the As desorption. However, the surface of (111)A GaAs is terminated by Ga (also called polar surface), the measure must be taken during the growth of GaAs on (111)A GaAs and lowering the growth temperature along with As₂ prelayer would help to minimize the Ga atom desorption from the surface. Thus, the growth temperature was selected based on the surface terminated atoms of the GaAs substrate. A Ge epilayer was grown on each GaAs substrate with a chamber base pressure of 2.8×10^{-8} Torr. The growth rate for all the Ge layers studied here were ~ 0.07 , 0.078, and 0.10 Å/s on (100), (110), and (111)A GaAs substrates, respectively, as determined by triple axis x-ray diffraction from Pendellösung thickness fringes as well as cross-sectional transmission electron microscopy. The growth temperature of Ge was in the range of 400–450 °C and it was selected in order to prevent the indiffusion of Ge into GaAs and outdiffusion of Ga and As into Ge film. After the growth of Ge epitaxial layer on each substrate orientation, the growth temperature was carefully reduced to ~ 50 °C and selected wafers were then transferred to III–V MBE chamber for subsequent GaAs layer growth. The surface reconstruction of each Ge layer was recorded by the RHEED system. Migration enhanced epitaxy (MEE) with As₂ prelayer was used for the subsequent GaAs growth on Ge epilayer with thickness of ~ 30 Å. The growth of upper GaAs layer was carried out at a lower substrate temperature of ~ 350 °C in all cases to prevent out-diffusion of Ge and simultaneous in-diffusion of Ga and As into Ge. An As₂/Ga ratio of ~ 14 and reduced growth rate of 0.25 Å/s was maintained at all times. The nucleation of GaAs on Ge was also monitored using the RHEED system. Table I summarizes the details of each test structure that were characterized in this work.

The thickness of the epitaxial Ge layers investigated ranged from about 75 to 150 nm. A 15 keV electron beam energy at a glancing incident angle of 1°–4° on the RHEED system was used to record the RHEED pattern during the growth in III–V MBE chamber. Epitaxial films were investigated using contact mode atomic force microscopy (AFM) to reveal surface morphology. The epitaxy of undoped Ge and GaAs/Ge/GaAs double heterostructures were confirmed using a Panalytical MRD X'Pert Pro triple axis x-ray diffraction system with a CuK α 1 line-focused x-ray source. Dynamic secondary ion mass spectrometry (SIMS) was used to determine the depth profile of As, Ga, and Ge atoms at the interface of GaAs/Ge/GaAs double heterostructures grown on three crystallographic GaAs substrates. SIMS analysis was performed using a Cameca IMS-7f GEO with 5 kV Cs⁺

TABLE I. Summary of *in situ* MBE grown Ge and GaAs/Ge/GaAs heterostructures on (100)/6°, (110), and (111)A GaAs substrates.

Sample number	GaAs substrate	Ge growth temperature (°C)	Ge thickness (nm)	MEE GaAs at 350 °C (nm)	GaAs at 500 °C (nm)	Surface <i>rms</i> roughness (nm)
A	(100)/6°	450	10	—	—	0.488
B	(100)/6°	450	75	3	50	—
C	(100)/6°	450	150	3	50	2.45
D	(110)	400	112	—	—	0.208
E	(110)	400	84	3	50	0.273
F	(111)A	400	140	—	—	0.315
G	(111)A	400	70	3	50	2.47

bombardment and MCs^+ detection to reduce matrix effects. The band alignment of each interface of *in situ* grown GaAs/Ge/GaAs heterostructures was investigated using scanning x-ray photoelectron spectroscopy (XPS) on a PHI Quantera SXM XPS system. The GaAs and Ge epilayers were wet etched using $NH_4OH:H_2O_2:H_2O$ (2:1:200 volume ratio) for a required thickness of ~ 5 –8 nm and the surface oxide in each layer was removed prior to the XPS measurements. The valence band offset is an important parameter to confine the hole carrier inside of the Ge QW and it also depends on the order it was deposited: valence band offset of GaAs epilayer on Ge is different from the Ge epilayer on GaAs.⁴⁰ Therefore, this work provides comprehensive information on the band alignment properties of the two interfaces of GaAs/Ge/GaAs heterostructures grown by MBE.

III. RESULTS AND DISCUSSION

A. RHEED studies on epitaxial GaAs/Ge/GaAs heterostructure

To study the surface morphologies of the GaAs epilayer, Ge epilayer on GaAs, and upper GaAs on Ge grown on (100)/6°, (110), and (111)A GaAs substrates, RHEED patterns were recorded at different stages of the growth. These RHEED patterns shed light on the reconstruction of epitaxial Ge layer grown on three crystallographic GaAs substrates. The (001) surface of compound semiconductors, such as GaAs and InP, shows a variety of reconstructions depending on the processing conditions and the resultant surface composition. The As-stabilized (2×4) surface of (001) GaAs has been most extensively studied and is widely accepted to have the two As-dimer model.⁴¹ A Ge layer was deposited on a reconstructed (2×4) GaAs surface with a surface layer being mainly arsenic. Growth of Ge on such a surface involves mainly Ge–As bonds (possibly some Ge–Ga bonds at the interface) and subsequent growth of a Ge lattice involves only the Ge–Ge bonding between neighboring atoms. Recently, we have demonstrated the (2×2) surface reconstruction of Ge layer grown on (100)/6° GaAs substrate.⁴⁰ Figure 1 shows the RHEED patterns along the [100] azimuth for the growth sequence of GaAs/Ge/(100)GaAs: (a) (100)/2° GaAs substrate shows a (2×4) pattern (similar to 6° offcut (100)GaAs substrate), (b) Ge film on (100)/6° GaAs exhibits (2×2) -fold surface reconstruction, and (c) upper GaAs layer on Ge/(100)/6° GaAs shows $(2 \times \text{weak-4})$ surface

reconstruction. The RHEED patterns from the surface of the Ge epilayer were recorded after transferring the Ge epilayer from the Ge MBE chamber to the III–V MBE chamber. Figure 2 shows streaky RHEED patterns along the [110] azimuth for the growth sequence of GaAs/Ge/(110)GaAs: (a) (110) GaAs substrate shows a (1×1) pattern, (b) Ge film on GaAs exhibits (3×4) -fold surface reconstruction, and (c) upper GaAs layer on Ge/GaAs shows (1×1) surface reconstruction. The (110)GaAs surface exhibits a (1×1) RHEED pattern, consistent with the other researchers.^{35,42–44} The Ge epitaxial film shows a streaky (3×4) RHEED pattern compared to the (1×1) , (2×3) , or (4×4) RHEED patterns observed by Chang and Kaun⁴³ under different growth conditions. Sharp and streaky RHEED patterns were observed from the growth of Ge on GaAs (110) and upper GaAs on

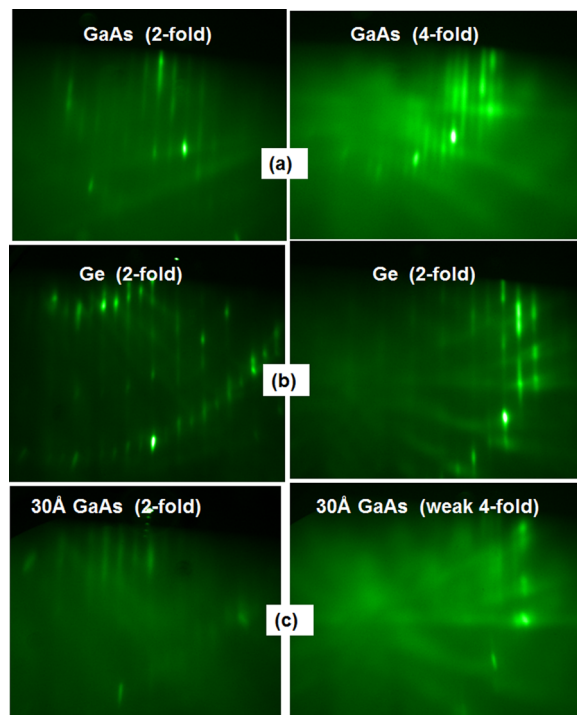


FIG. 1. (Color online) RHEED patterns at 15 keV from the surface of (a) a representative (100) GaAs substrate, (b) Ge epilayer, and (c) upper GaAs epitaxial layer along the azimuth of [100]. These RHEED patterns were recorded after transferring the Ge epilayer from Ge MBE chamber to III–V MBE chamber. The RHEED patterns exhibited streaky (2×4) , (2×2) , and $(2 \times \text{weak-4})$ surface reconstruction of (100) GaAs substrate, Ge epilayer, and upper GaAs layer grown on Ge, respectively.

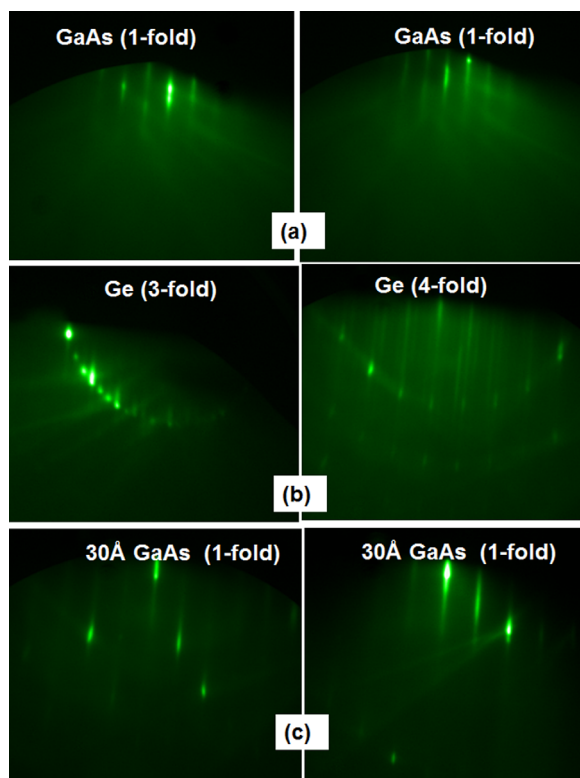


Fig. 2. (Color online) RHEED patterns at 15 keV from the surface of (a) (110) GaAs substrate, (b) Ge epilayer, and (c) upper GaAs epitaxial layer along the azimuth of [110]. The RHEED patterns exhibited streaky (1×1) , (3×4) , and (1×1) surface reconstruction of (110) GaAs substrate, Ge epilayer, and upper GaAs layer grown on Ge, respectively.

Ge/GaAs. Figure 3 shows the RHEED patterns along the [111] azimuth for the growth sequence of GaAs/Ge/(111)A GaAs: (a) (111)A GaAs substrate shows a streaky (2×2) pattern, (b) the Ge epilayer on GaAs shows a (1×1) pattern, and (c) the top GaAs epilayer on Ge/GaAs exhibits a (2×2) surface reconstruction. It is interesting to note that the upper GaAs layer shows a streaky (2×2) pattern compared to the starting (111)A GaAs substrate RHEED pattern. Surface reconstruction of (2×2) has been observed for the homoepitaxial (111)A GaAs by Cho⁴⁵ and Woolf *et al.*⁴⁶ The RHEED observations on the GaAs/Ge/(111)A GaAs heterostructure show two major differences with those of GaAs/Ge/(110)GaAs where the Ge epilayer on (110) GaAs shows (3×4) pattern compared to (1×1) on (111)A GaAs and upper GaAs epilayer on (110) GaAs shows (1×1) pattern.

B. Surface morphology of epitaxial Ge and GaAs/Ge/GaAs heterostructures

As shown in Sec. III A that RHEED study was used to comprehend the growth sequence of Ge on (100), (110) or (111)A GaAs, and GaAs/Ge/GaAs heterostructures at different stages of epitaxy. The study not only shows a different growth mechanism due to different RHEED patterns in these three cases, it also allows us to estimate the surface roughness in each case. Thus, it is important to characterize the surface roughness on an atomic scale for these

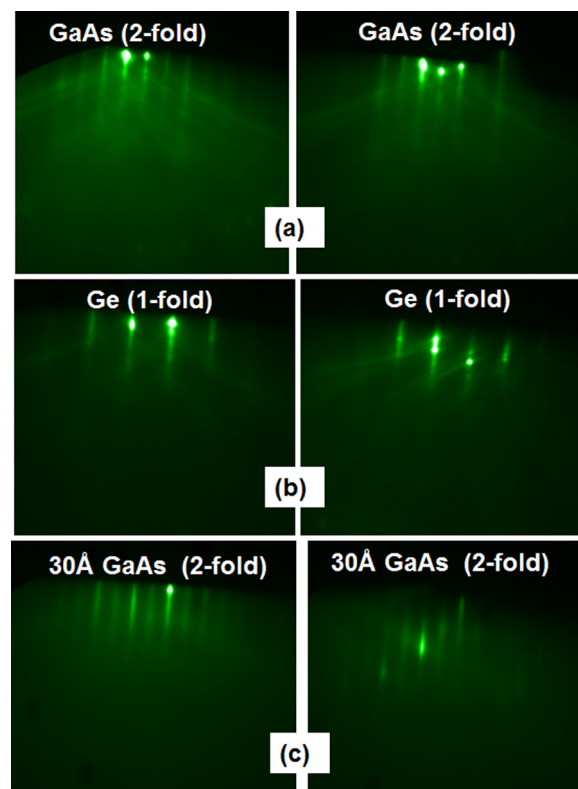


Fig. 3. (Color online) RHEED patterns at 15 keV from the surface of (a) (111) GaAs substrate, (b) Ge epilayer, and (c) upper GaAs epitaxial layer along the azimuth of [111]. The RHEED patterns exhibited streaky (2×2) , (1×1) , and (2×2) surface reconstruction of (110) GaAs substrate, Ge epilayer, and upper GaAs layer grown on Ge, respectively.

structures, as this is an important figure of merit. Surface morphology of Ge on (100)GaAs, (110)GaAs, (111)A GaAs as well as GaAs/Ge/GaAs heterostructures on three crystallographic GaAs substrates was examined by AFM in contact mode. AFM micrographs of these structures are shown in Figs. 4(a)–4(f). The root mean square (*rms*) roughness for Ge on (a) (100)/6° GaAs, (b) GaAs/Ge/(100)6° GaAs, (c) (110)GaAs, (d) GaAs/Ge/(110)GaAs, (e) Ge on (111)A GaAs, and (f) GaAs/Ge/(111)A GaAs heterostructure was 0.488, 2.45, 0.208, 0.273, 0.315, and 2.47 nm, respectively, measured over an area of $1 \times 1 \mu\text{m}^2$. From these figures, the anticipated extremely uniform and low surface roughness is an indication of high-quality two-dimensional epitaxy of Ge on GaAs as well as GaAs/Ge/GaAs heterostructure, in complete agreement with the RHEED results and analysis presented above. The surface *rms* from Ge films grown on (110) and (111)A were lower than Ge on (100)GaAs substrate using the similar process conditions, reported earlier⁴⁰ as well as shown in Fig. 4(a).

C. Strain relaxation properties of GaAs/Ge/GaAs heterostructures

To determine the structural quality and relaxation state of Ge epitaxial film and the GaAs/Ge/GaAs double heterostructure grown on different crystallographic GaAs substrates, high-resolution triple axis x-ray (004) rocking curves were recorded. Figure 5 shows a rocking curve from the (004)

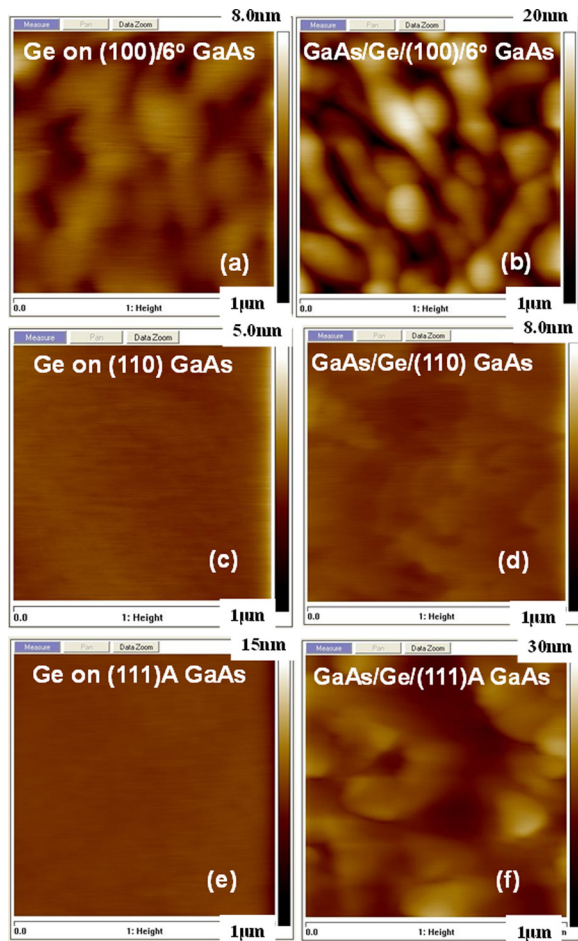


FIG. 4. (Color online) AFM micrographs of (a) 10 nm Ge on (100) 6° GaAs ($rms = 0.488$ nm), (b) 53 nm GaAs/150 nm Ge/(100) 6° GaAs ($rms = 2.45$ nm); (c) 112 nm Ge on (110) GaAs ($rms = 0.208$ nm), (d) 53 nm GaAs/84 nm Ge/(110)GaAs ($rms = 0.273$ nm); (e) 140 nm Ge on (111)AGaAs ($rms = 0.315$ nm) and (f) 53 nm GaAs/70 nm Ge/(111)AGaAs ($rms = 2.47$ nm), respectively, grown at two step growth process where upper 50 nm GaAs was grown at 500 $^\circ$ C and 3 nm grown at 350 $^\circ$ C using migration enhanced epitaxy.

Bragg lines of GaAs/Ge/GaAs double heterostructure grown on (100) 6° , (110), and (111)A GaAs substrates, where the epitaxial Ge layer thickness is significantly lower than the critical layer thickness. The angular separation between

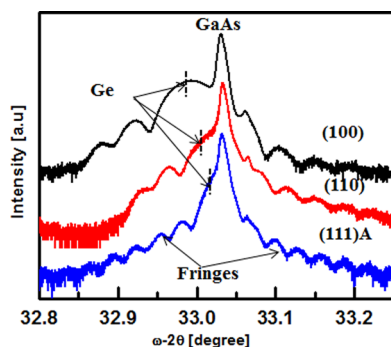


FIG. 5. (Color online) X-ray rocking curves from the (004) reflection of (a) 53 nm GaAs/150 nm Ge/GaAs heterostructure on (100) 6° GaAs, (b) 112 nm Ge on (110)GaAs, and (c) 140 nm Ge on (111)A GaAs substrate, respectively. The Pendellösung oscillations in the rocking curve confirm the high crystalline quality of the Ge epitaxial layer.

the (004) diffraction peaks of Ge and GaAs results from the difference in lattice plane spacing along with their diffraction line profiles, providing information about the microstructural quality of the Ge film. The average peak separation between the Ge epilayer and the different oriented GaAs substrate is from 60 to 145 arc sec. The appearance of Pendellösung oscillation fringes on both sides of Ge and GaAs peaks implies a parallel and very sharp heterointerface presents in this structure. This interference originates from the beating of two x-ray wave fields inside of a crystal. One of the wave fields is generated at the interface between the GaAs and Ge as well as another wave field on the surface of the Ge layer. As a result, interference can only be observed in crystals that have almost perfectly parallel boundaries.⁴⁷ The relaxation state of Ge layer in each substrate orientation was also measured from symmetric (004) and asymmetric (115) reflections of reciprocal space maps (RSMs) measured using triple axis x-ray diffraction (not shown here). From these RSMs, one can determine the lattice parameter in the out-of-plane (growth direction), a_\perp (from the symmetric reflection), and the lattice parameter in the growth plane, a_\parallel (from the asymmetric reflection). The degree of relaxation of the Ge layer was limited to only 5% in each case, which is expected since the critical layer thickness of Ge is about 1.8 μ m. We can conclude from the minimal relaxation and the thickness fringes observed here that the quality of the GaAs/Ge/GaAs heterostructure on (100), (110), or (111)A GaAs substrates is high.

D. SIMS depth profiles of GaAs/Ge/GaAs heterostructures

Dynamic SIMS depth profiling was used to determine the extent of elemental diffusion or reaction at each of the GaAs/Ge/GaAs interfaces on (100), (110), and (111)A GaAs substrates. Such interactions can take place due to thermodynamic driving forces, especially at growth temperatures. Higher growth temperature promotes movement of atoms across surfaces as well as interfaces. The growth temperature has been selected which allows epitaxial formation of both the Ge and GaAs layers but negligible intermixing of the species at each heterointerface. In the case of GaAs/Ge/GaAs, heterostructure grown on crystallographic oriented GaAs substrates for which the optimum growth temperatures of each layer were different due to the ad-atoms surface mobility and the termination of surface atoms. The growth of Ge layer at lower temperature (≤ 450 $^\circ$ C) is followed by growth of the upper GaAs layer at both 350 (30 \AA MEE layer) and 500 $^\circ$ C (500 \AA). SIMS measurements were performed monitoring the molecular Cs ions (CsAs^+ , CsGe^+ , and CsGa^+) as this method suffers less from mass interference issues and reduces matrix effects giving a truer picture of the signal variation between layers. The depth scale was established using thickness measurements of the layers from transmission electron microscopy measurements with an estimated error of $\sim 10\%$. Figures 6(a)–6(c) show the Ga, As, and Ge depth profiles of the GaAs/Ge/GaAs double heterostructure grown on (100), (110), and (111)A GaAs

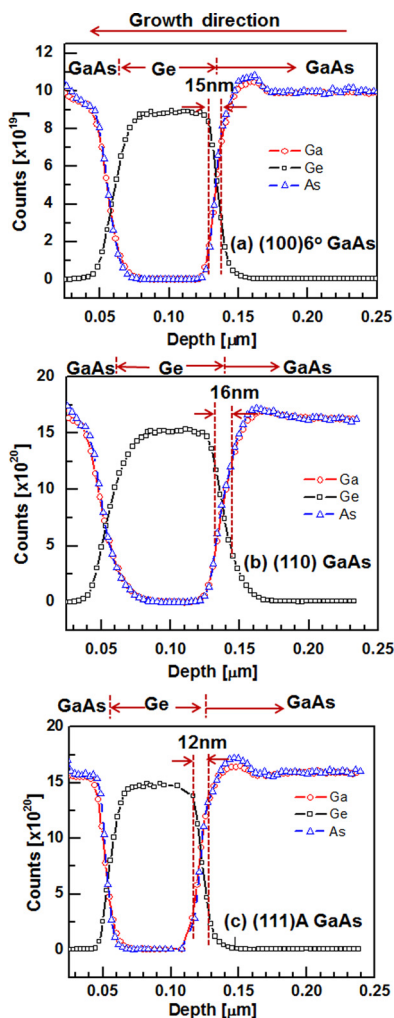


FIG. 6. (Color online) SIMS profiles of GaAs/Ge/GaAs double heterostructures grown on (a) (100) 6° GaAs, (b) (110) GaAs, and (c) (111)A GaAs substrates, respectively.

substrates, respectively, in which Ge and GaAs layers were grown in separate MBE chambers. All depth profiles illustrate constant Ga, As, and Ge intensities within each layer, indicating good growth uniformity. One can find from this figure that As and Ga levels are very low inside the Ge layer that can affect the doping characteristics of the undoped Ge layer. Besides, the depth profiles display an abrupt Ge/GaAs bottom heterointerface, a transition between Ge/GaAs of less than 15 nm, within the sputter-induced broadening of the ion beam, indicating low value of Ga, As, and Ge intermixing at the Ge/GaAs bottom interface of each layer structure studied in this work. In addition, for all the three samples, Ga and As profiles show a hump at the Ge/GaAs (bottom) interface and it was due to the SIMS artifact caused by ion yield due to the change of matrix element (Ga, As, and Ge) transient effect. As pointed out by Bai *et al.*⁴⁸ for planar Ge films at the lowest possible thickness, Ga-rich surfaces are desired; however, Ga-rich surfaces result in significant Ga exchange, resulting in high Ga concentrations in the Ge film. Interestingly, our SIMS depth profiles and the interface broadening on the (111)A GaAs surface exhibited the lowest interface broadening compared to either (100) or (110) GaAs substrates. Also,

the incorporation path of Ga and As atoms during the growth of Ge on GaAs surfaces are independent on the surface orientations with the carefully designed process growth parameters. Furthermore, the Ge outdiffusion into the top GaAs layer or the Ga and As indiffusion to the Ge epilayer were minimal using the process conditions described above. Thus, dynamic SIMS depth profiles underscore the delicate balance between growth conditions, substrate orientation, surface reconstruction, and interface intermixing at the GaAs/Ge/GaAs double heterostructures.

E. Band alignment properties of GaAs/Ge/GaAs heterostructures

There is no unique band offset value for each of the heterointerfaces of the GaAs/Ge/GaAs double heterojunction and experiments must therefore provide better insight into structure-property correlations for *in situ* growth of Ge in an arsenic-free environment for GaAs/Ge/GaAs heterojunction on (100) 6° , (110), and (111)A GaAs substrates. Conduction band offsets varying from 0.09 to 0.54 eV can be found in the literature, a range corresponding to 68% of the energy gap of Ge.⁴⁹ The reason is partly due to measurement errors and polar on nonpolar growth.⁴⁹ As we know that the two semiconductors having different bandgap result in band discontinuities (valence-band discontinuity, ΔE_v , and a conduction-band discontinuity, ΔE_c , such that $\Delta E_g = \Delta E_v + \Delta E_c$) when in contact and these band discontinuities play a crucial role in the electrical transport properties of a heterojunction devices like quantum well field effect transistors, heterojunction bipolar transistors, tunnel FETs, III-V multijunction solar cells, superlattice photodetectors, heterostructure lasers, etc. The transport properties of all these heterojunction based devices strongly depend on (i) band discontinuities, (ii) interface states, and (iii) potential-barrier height.

Most theoretical treatments of heterojunction band lineups have assumed abrupt, lattice-matched interfaces. Likewise, most assume that there is an absolute energy associated with each semiconductor so that the band offsets reflect differences in those energies. Experimentally, however, it has been observed that the electrical properties can be related to the chemical and geometric structure at the interface and can be dictated by deviations from perfection.^{35,50,51} In particular, band offsets can depend on such variables as substrate orientation, overlayer crystallinity, surface reconstruction, deposition temperature, deposition rate, microscopic interface dipole, and interdiffusion or reactivity.⁵² Growth sequence or the order of deposition (i.e., Ge on GaAs or GaAs on Ge) can also influence the band offset properties of the heterojunction.⁴⁰ Zurcher and Bauer⁵³ measured a ΔE_v of 0.23–0.26 eV for GaAs deposited on Ge (110), which is significantly lowered compared to the band offset value of Ge on GaAs (110) where ΔE_v is 0.42 (Ref. 54) or 0.53 eV.³⁶ On the other hand, GaAs epitaxial layer grown on either (100) or (111) polar Ge surfaces can produce antiphase domains (APDs) and rough surface morphology in an atomic scale compared to GaAs grown on Ge (110), where the surface morphology is similar to the (100) homoepitaxial MBE grown GaAs. As a result,

the surface morphology is smooth on (110), suggesting that if APDs are formed,⁵⁵ their effect on the surface morphology is less significant compared to (100) and (111) orientations. In particular, offset variations up to ~ 0.9 eV due to microscopic interface dipoles were theoretically calculated by Baraff *et al.*⁵⁶ for the lattice matched Ge/GaAs (100) interface. These dipoles are originated from oriented pairs of atoms at the interface.⁵⁷

X-ray photoelectron experiments have been performed to determine the band discontinuities of Ge on GaAs and yielded $\Delta E_v = -0.56 \pm 0.04$ eV for Ge on GaAs (110), $\Delta E_v \sim 0.3$ eV for GaAs on Ge (110), ΔE_v varying from -0.3 to -0.66 eV for Ge on GaAs (100) and $\Delta E_v = 0.17$ – 0.3 eV for GaAs on Ge (100), substrates, respectively. Moreover, arsenic saturation of the (110) Ge surface prior to the deposition of GaAs during MBE growth by the formation of uncontrolled composition of GeAs_x layer strongly favors a surface reconstruction that generates Ga-like sites, to which As atoms can bond.⁵⁶ Very limited experimental band offset data for the GaAs/Ge/GaAs heterostructures are available to date on the (111)A GaAs substrate,⁵⁸ which has a significant advantage for the enhancement of electron mobility in Ge material. Furthermore, the heteroepitaxial growth of GaAs on (111) Ge surface exhibits poor surface morphology due to formation of stacking faults⁵⁹ compared to other orientations; however, antiphase domain boundaries are never observed on this orientation than on (100) or (110) Ge substrates⁶⁰ though (111) is a polar surface. This prompted us to determine the band offset value carefully of each interface of GaAs/Ge/GaAs heterostructures grown on (100), (110), and (111)A GaAs substrates and its correlation in a relationship in structural and morphological properties of GaAs/Ge/GaAs heterostructures grown *in situ* using two separate MBE chambers, as described earlier.

1. GaAs/Ge/(100)GaAs

The value of ΔE_v at the GaAs on Ge and Ge on GaAs heterointerfaces was determined using the Phi Quanterra XPS system with a monochromatic Al-K α x-ray source (1486.6 eV) and a 45° take-off angle. An angle integrated photoelectron energy distribution curves for the valence band maximum (VBM) and As 3d_{5/2}, Ga 3d_{3/2}, and Ge 3d_{3/2} core levels spectra were recorded at each interface for each orientation. We have selected As 3d_{5/2} core level spectra than As 3d_{3/2} since the binding energy separation between As 3d_{5/2} and As 3d_{3/2} peaks is fixed to 0.7 eV during curve fitting. As a result, the band offset result would not change if we select As 3d_{3/2} as the core level binding energy peak. On the other hand, the binding energy difference between Ga 3d_{5/2} and Ga 3d_{3/2} is limited to only 0.2 eV. Therefore, it is difficult to resolve the two binding energy levels during the XPS measurement. All the samples were cleaned and mounted on a sample stage prior to transfer to the XPS system using an ultrahigh vacuum ($\sim 10^{-7}$ Torr) transfer stage. The binding energy was corrected by adjusting the C 1s core-level peak position to 285.0 eV for each sample surface. Using this approach, the XPS spectra were recorded from the following

five samples for each orientation: (i) GaAs wafer, (ii) thin Ge on GaAs substrate, (iii) thick Ge on GaAs substrate, (iv) thin GaAs on Ge, and (v) thick top GaAs layer. Figure 7 shows XPS spectra for upper GaAs on Ge interface of (a) As 3d_{5/2} core level ($E_{\text{As}3d}^{\text{GaAs}}$) and (b) VBM ($E_{\text{VBM}}^{\text{GaAs}}$) of thick GaAs film; (c) Ge 3d_{3/2} core level ($E_{\text{Ge}3d}^{\text{Ge}}$) and (d) VBM ($E_{\text{VBM}}^{\text{Ge}}$) of thick Ge film; (e) As 3d_{5/2} core level ($E_{\text{As}3d}^{\text{GaAs}}$) and (f) Ge 3d_{3/2} core level ($E_{\text{Ge}3d}^{\text{Ge}}$) of thin GaAs on Ge interface, respectively. Similarly, Fig. 8 shows (a) As 3d_{5/2} core level ($E_{\text{As}3d}^{\text{GaAs}}$) and (b) VBM ($E_{\text{VBM}}^{\text{GaAs}}$) of GaAs substrate, (c) As 3d_{5/2} core level ($E_{\text{As}3d}^{\text{GaAs}}$) and (d) Ge 3d_{3/2} core level ($E_{\text{Ge}3d}^{\text{Ge}}$) of thin Ge on GaAs interface. The upper GaAs on Ge interface valence band offset value, $\Delta E_v^{\text{Upper}}$, was determined with the

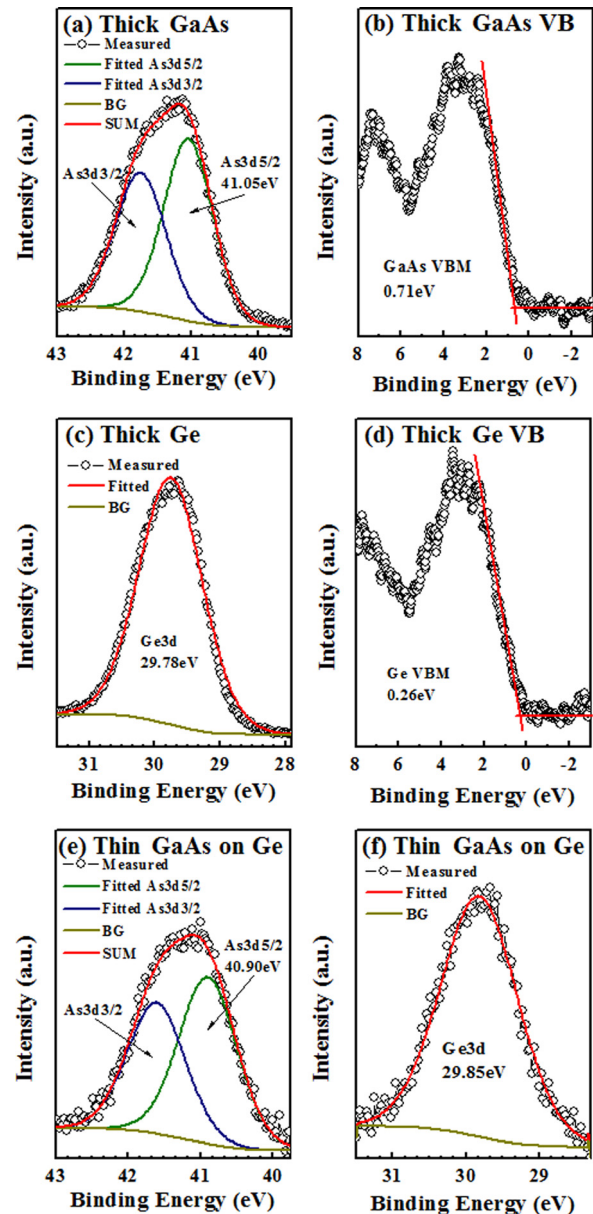


Fig. 7. (Color online) XPS spectra (upper GaAs on Ge) of (a) As 3d_{5/2} core level ($E_{\text{As}3d}^{\text{GaAs}}$) and (b) VBM ($E_{\text{VBM}}^{\text{GaAs}}$) of GaAs film; (c) Ge 3d_{3/2} core level ($E_{\text{Ge}3d}^{\text{Ge}}$) and (d) VBM ($E_{\text{VBM}}^{\text{Ge}}$) of thick Ge film; (e) As 3d_{5/2} core level ($E_{\text{As}3d}^{\text{GaAs}}$) and (f) Ge 3d_{3/2} core level ($E_{\text{Ge}3d}^{\text{Ge}}$) at thin upper GaAs/Ge interface grown on (100)/6° GaAs, respectively.

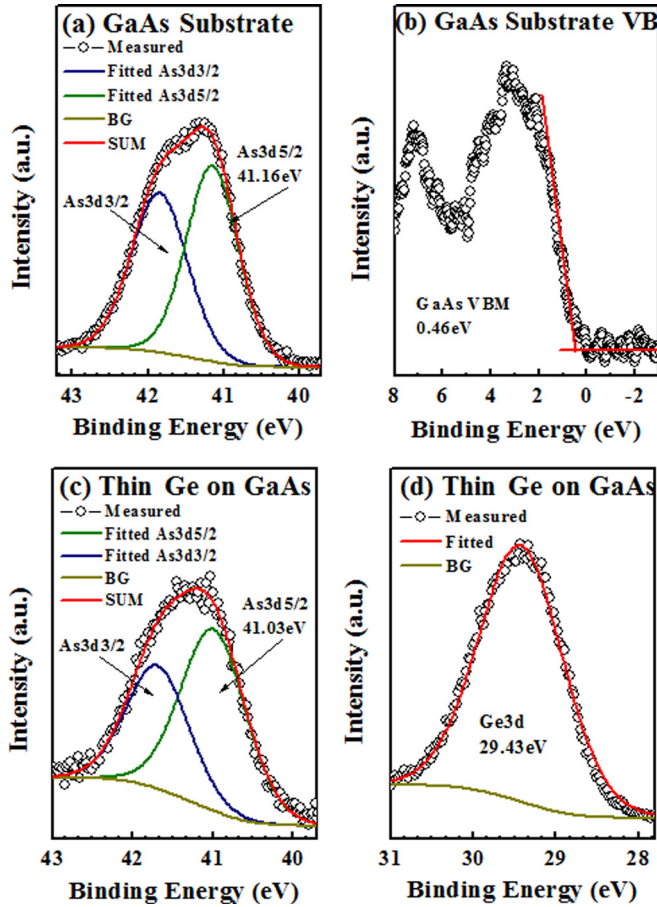


FIG. 8. (Color online) XPS spectra (bottom Ge on GaAs) of (a) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (b) VBM (E_{VBM}^{GaAs}) of GaAs film; (c) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (d) Ge $3d_{3/2}$ core level (E_{Ge3d}^{Ge}) at thin Ge/(100)/6° GaAs interface, respectively.

following equation³⁶ for each orientation using their respective core level spectra:

$$\Delta E_V^{Upper} \left(\frac{GaAs}{Ge} \right) = \left(E_{As3d_{5/2}}^{GaAs} - E_{Ge3d_{3/2}}^{Ge} \right)^{interface} - \left\{ \left(E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs} \right)^{GaAs} - \left(E_{Ge3d_{3/2}}^{Ge} - E_{VBM}^{Ge} \right)^{Ge} \right\}. \quad (1)$$

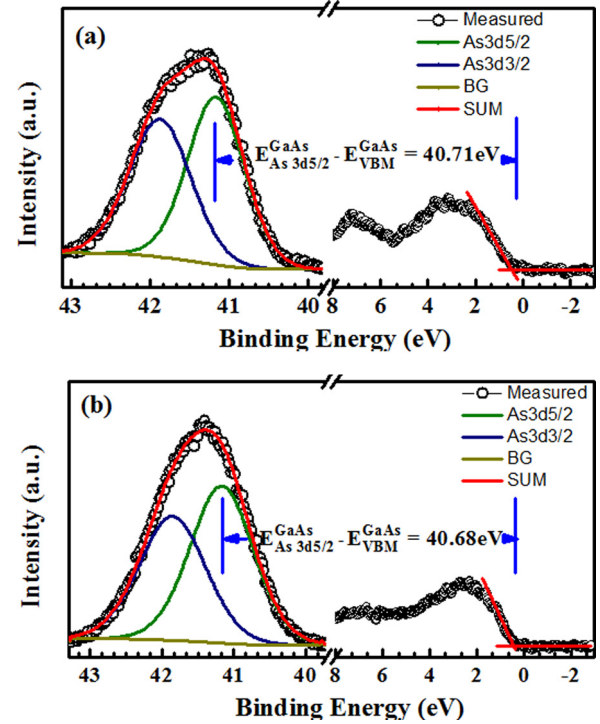


FIG. 9. (Color online) XPS spectra of (a) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (b) VBM (E_{VBM}^{GaAs}) difference of GaAs film after wet cleaning; (c) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (b) VBM (E_{VBM}^{GaAs}) difference of GaAs film after 15 s sputter inside the XPS chamber using 3 kV Ar^+ ions to remove the surface oxygen (if any). Note that similar value of $E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs}$ indicate that the presence of surface oxygen (if any after the wet cleaning prior to XPS measurement) does not influence for the determination of valence band offset in this work.

Similarly, the bottom heterointerface Ge on GaAs valence band offset, ΔE_V^{Bottom} , can be determined from the following equation³⁶ for each orientation using their respective core level spectra:

$$\Delta E_V^{Bottom} \left(\frac{Ge}{GaAs} \right) = \left(E_{As3d_{5/2}}^{GaAs} - E_{Ge3d_{3/2}}^{Ge} \right)^{interface} - \left\{ \left(E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs} \right)^{GaAs} - \left(E_{Ge3d_{3/2}}^{Ge} - E_{VBM}^{Ge} \right)^{Ge} \right\}. \quad (2)$$

TABLE II. Core-level to VBM binding-energy difference for epitaxial Ge and (100)/6° GaAs.

Material and interface	Binding energy difference	Measured valence band offset, ΔE_V , of GaAs/Ge/GaAs (100)/6°	
		Bottom Ge/GaAs (100) interface	Top GaAs/Ge interface
GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs} = 40.34 \pm 0.05$ eV	0.42 ± 0.05 eV	—
Thin Ge on GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{Ge3d_{3/2}}^{Ge} = 11.05 \pm 0.05$ eV	—	—
Thick Ge	$E_{Ge3d_{3/2}}^{Ge} - E_{VBM}^{Ge} = 29.52 \pm 0.05$ eV	—	0.23 ± 0.05 eV
Thin GaAs on Ge	$E_{As3d_{5/2}}^{GaAs} - E_{Ge3d_{3/2}}^{Ge} = 11.60 \pm 0.05$ eV	—	—
GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs} = 40.70 \pm 0.05$ eV	—	—

The result obtained from analysis of this data is presented in Table II. The present value of measured ΔE_v of the top GaAs on Ge ($\Delta E_v = 0.23 \pm 0.05$ eV) as well as bottom Ge on GaAs ($\Delta E_v = 0.42 \pm 0.05$ eV) heterointerface is in excellent agreement with the experimental results obtained by other researchers^{58,61–63} and theoretical predictions of Harrison⁶⁴ and Cardona and Christensen.⁶⁵ It is evident that most experimental ΔE_v data of Ge on GaAs are in the 0.4–0.7 eV range and the average ΔE_v is 0.55 ± 0.13 eV. The dependence of the Ge on GaAs ΔE_v on growth conditions such as use of the same chamber for both Ge and GaAs layer growth, growth temperature, surface reconstruction, and doping may be responsible for the wide range of experimental ΔE_v reported in supposedly abrupt Ge/(001)GaAs heterojunction.

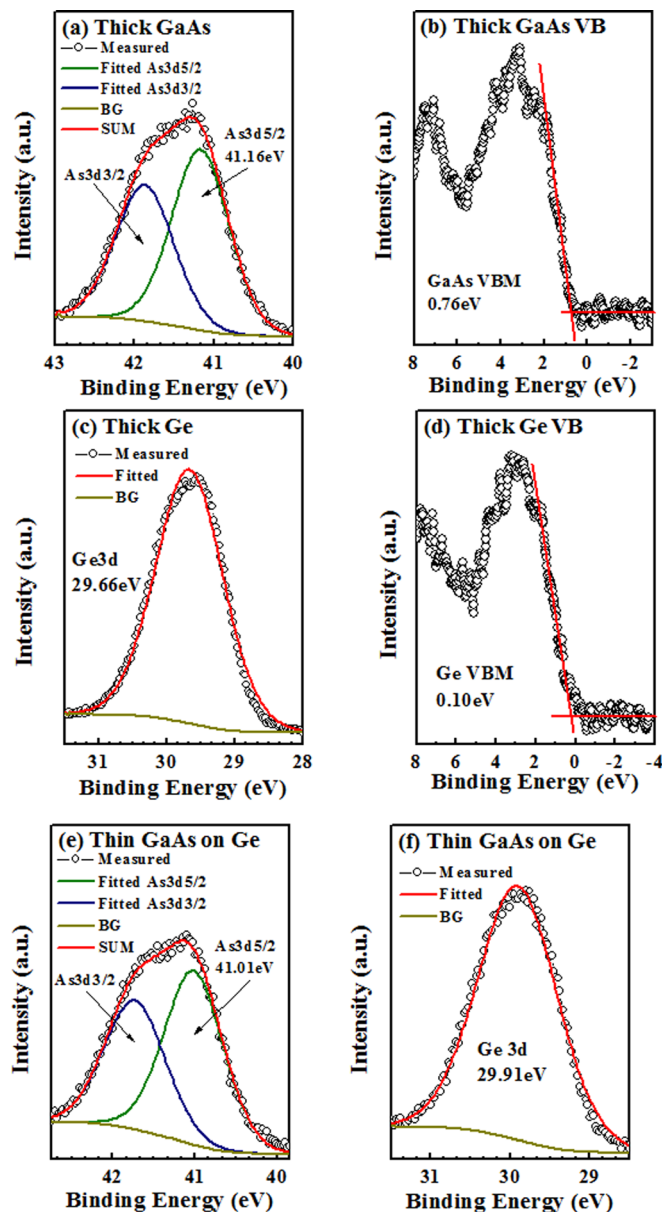


Fig. 10. (Color online) XPS spectra (upper GaAs on Ge) of (a) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (b) VBM (E_{VBM}^{GaAs}) of GaAs film; (c) Ge $3d_{3/2}$ core level (E_{Ge3d}^{Ge}) and (d) VBM (E_{VBM}^{Ge}) of thick Ge film; (e) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (f) Ge $3d_{3/2}$ core level (E_{Ge3d}^{Ge}) at thin upper GaAs/Ge interface grown on (110)GaAs, respectively.

The thin and thick GaAs samples might have different amount of oxides on the surface although the oxide was removed using dilute HCl solution prior to XPS measurement of GaAs on Ge/GaAs and GaAs substrate. This oxide layer formation could happen inside the XPS chamber or duration of the XPS measurement. It has been also argued that the valence band spectrum obtained from XPS measurement could be the weighted partial density-of-states (DOS) from the clean surface and the presence of oxygen on the surface. The spectrum line shape could be different from the true DOS on the clean sample surface without presence of oxygen component and simply using a linear extrapolation of measured spectrum to define valence band maximum might cause error in the determination of band offset value. In order to address this concern and provide a solution, we performed depth dependent XPS measurements from the surface of GaAs grown on Ge/GaAs(100) to see if the surface oxygen shifts the upper valence band offset value. Figure 9 shows the core level valence band XPS spectra from the surface of (a) GaAs (5 min inside the XPS chamber after removing oxide using HCl) and (b) the GaAs surface was *in situ* sputter cleaned using 3 kV Ar^+ ion for 15 s in the XPS analysis chamber. Figure 9 shows that the value of $E_{GaAs} - E_{VBM}$ from the above two cases are almost identical within the experimental error and thus, the measured VBM position is accurate for the GaAs layer and hence the value of valence band offset. The oxide layer from the surface of Ge was removed by deionized water prior to

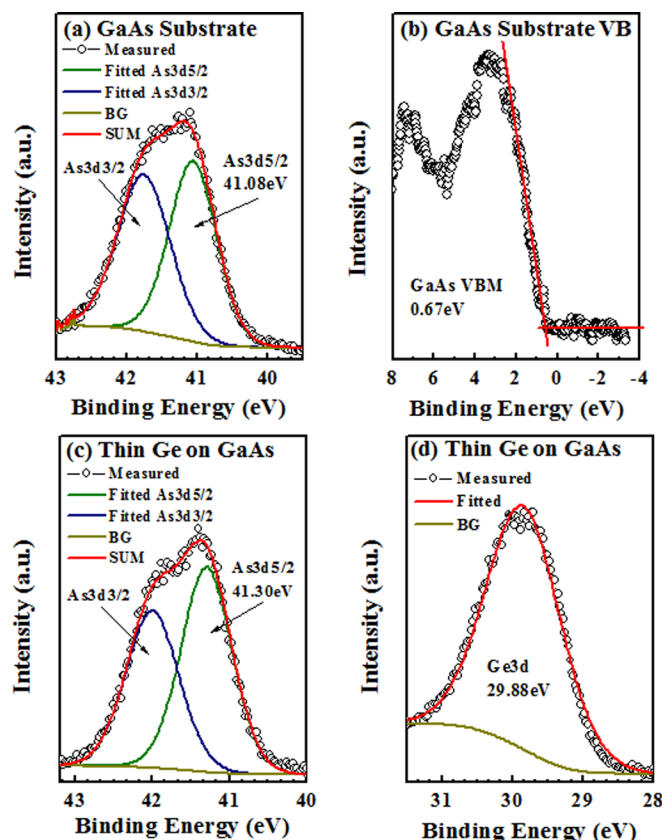


Fig. 11. (Color online) XPS spectra (bottom Ge on GaAs) of (a) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (b) VBM (E_{VBM}^{GaAs}) of GaAs film; (c) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (d) Ge $3d_{3/2}$ core level (E_{Ge3d}^{Ge}) at thin Ge/(110)GaAs interface, respectively.

loading in XPS chamber so the depth dependent core level and valence band spectra were not collected. Thus, the surface oxide layer (if any) has a negligible effect on the determination of valence band offset of the GaAs/Ge heterostructures once the surface of GaAs was cleaned prior loading to XPS chamber for measurement.

2. GaAs/Ge/(110) GaAs

It has been suggested that the (110) orientation is the preferred orientation for the MBE growth of zinc blende-on-diamond system⁵⁵ as well as the importance of the technological requirement for the enhancement of hole mobility on this orientation, as discussed earlier. The valence band discontinuities have been measured for each interface of the GaAs/Ge/(110)GaAs heterostructure and the offsets were evaluated

using Eqs. (1) and (2). The core-level to valence band energy difference and the resulting band offset parameters are presented in Table III. It should be noted that isolated interface of Ge on GaAs(110) or GaAs on Ge(110) was investigated by other researchers^{37,38} but there is no prior work reported on the band offset properties of the GaAs/Ge/GaAs(110) double heterostructure grown using two separate MBE chambers. Figures 10 and 11 show the core level XPS spectra for the upper GaAs on Ge and bottom Ge on (110) GaAs interface, respectively. The measured values of ΔE_v for the GaAs on Ge and Ge on (110) GaAs are 0.26 ± 0.05 and 0.57 ± 0.05 eV, respectively. The average experimental ΔE_v for the GaAs on Ge is 0.23 ± 0.05 and 0.55 ± 0.05 eV^{37,38} for Ge on (110) GaAs, consistent with our results.

3. GaAs/Ge/(111)A GaAs

Figures 12 and 13 show the core level XPS spectra for the upper GaAs on Ge and bottom Ge on (111)A GaAs interface, respectively. The measured values of ΔE_v for the GaAs on Ge and Ge on (111)A GaAs are 0.31 ± 0.05 eV and 0.61 ± 0.05 eV, respectively. These offset values are higher than on (100)GaAs or (110)GaAs substrates. The band offset parameters obtained from each interface of GaAs/Ge/(111)A GaAs heterostructure is presented in Table IV. Figure 14 shows the band alignment of the GaAs/Ge/GaAs double heterostructures grown on (a) (100) GaAs, (b) (110) GaAs, and

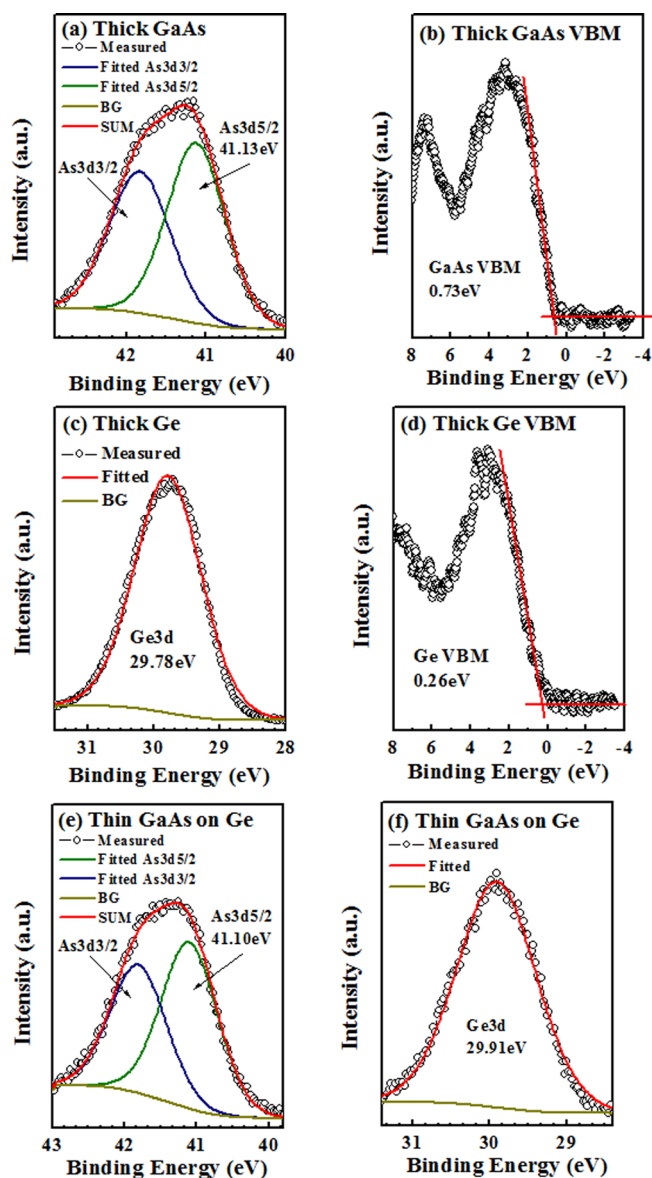


Fig. 12. (Color online) XPS spectra (upper GaAs on Ge) of (a) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (b) VBM (E_{VBM}^{GaAs}) of GaAs film; (c) Ge $3d_{3/2}$ core level (E_{Ge3d}^{Ge}) and (d) VBM (E_{VBM}^{Ge}) of thick Ge film; (e) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (f) Ge $3d_{3/2}$ core level (E_{Ge3d}^{Ge}) at thin upper GaAs/Ge interface grown on (111)A GaAs, respectively.

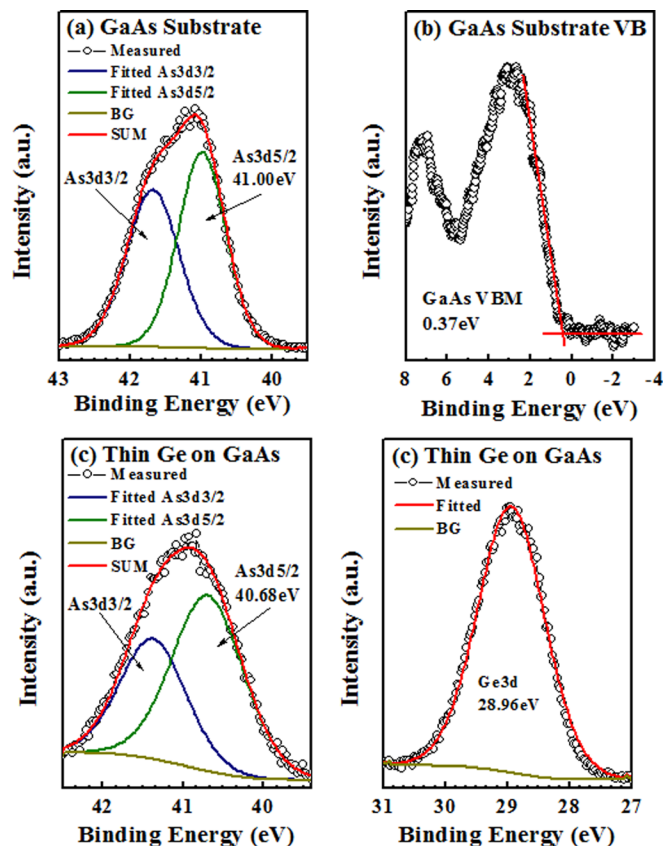


Fig. 13. (Color online) XPS spectra (bottom Ge on GaAs) of (a) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (b) VBM (E_{VBM}^{GaAs}) of GaAs film; (c) As $3d_{5/2}$ core level (E_{As3d}^{GaAs}) and (d) Ge $3d_{3/2}$ core level (E_{Ge3d}^{Ge}) at thin Ge/(111)A GaAs interface, respectively.

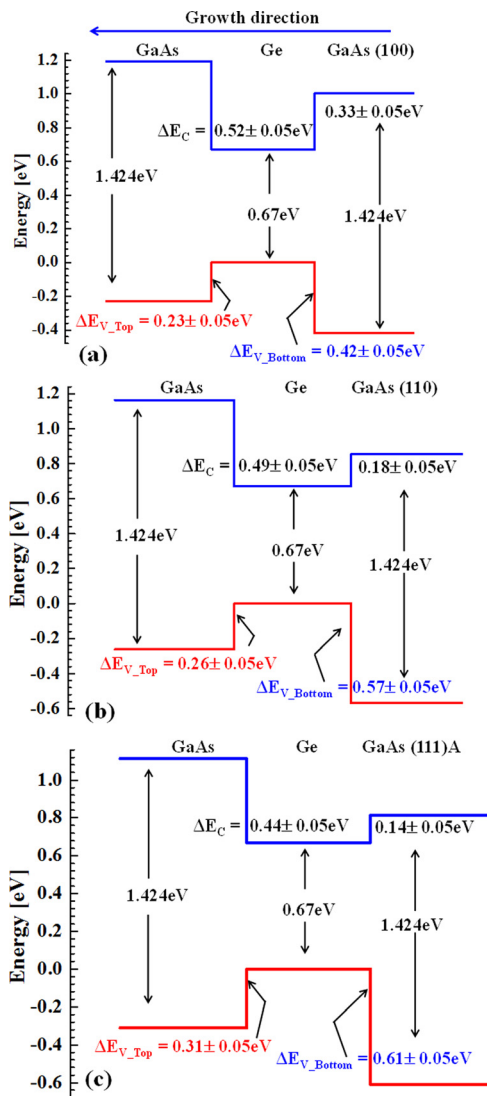


FIG. 14. (Color online) Schematic band alignment of GaAs/Ge/GaAs double heterostructures grown on (a) (100)/6° GaAs, (b) (110) GaAs, and (c) (111) A GaAs substrates, based on the measured ΔE_V using XPS. The conduction band discontinuity, ΔE_C , has been calculated based on the measured ΔE_V and the difference in bandgap of GaAs and Ge, where $\Delta E_g = \Delta E_V + \Delta E_C$.

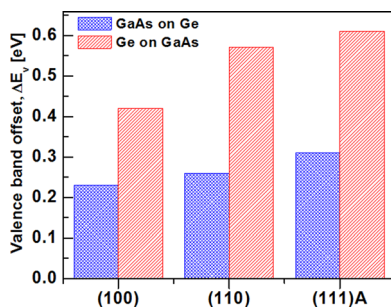


FIG. 15. (Color online) Histogram of valence band offset distribution obtained from GaAs/Ge/GaAs double heterostructures grown on (100)/6° GaAs, (110) GaAs, and (111)A GaAs substrates. The highest ΔE_V value for both upper and bottom interface of GaAs/Ge/GaAs was obtained on (111)A GaAs substrate.

(c) (111) A GaAs substrates, based on the measured ΔE_V values. The conduction band discontinuity, ΔE_C , can be calculated based on the measured ΔE_V and the difference in bandgap of GaAs and Ge, where $\Delta E_g = \Delta E_V + \Delta E_C$. One can find that the substrate orientation has a strong influence on the band offset properties, which is believed to be the quality of the heterojunction growth, the surface reconstruction, and charge neutrality at each heterointerface. Several models have been developed⁵² to explain the difference in band offset values. Fang and Howard⁶⁶ and Grant *et al.*^{35,67} have carried out the valence band offset of Ge on different oriented GaAs substrates and demonstrated a relationship of $\Delta E_V(111)Ga < \Delta E_V(\bar{1}\bar{1}\bar{1})As < \Delta E_V(110)$ and $\Delta E_V(111)Ga < \Delta E_V(100)Ga < \Delta E_V(110) < \Delta E_V(100)As < \Delta E_V(\bar{1}\bar{1}\bar{1})As$ using capacitance–voltage and XPS method, respectively. Although, the magnitude of the variation of the ΔE_V they have observed is consistent in some orientations, our results contradict the valence band offset relation above and achieved a valence band offset relation of $\Delta E_V(111)Ga > \Delta E_V(110) > \Delta E_V(100)As$ after careful investigation of XPS

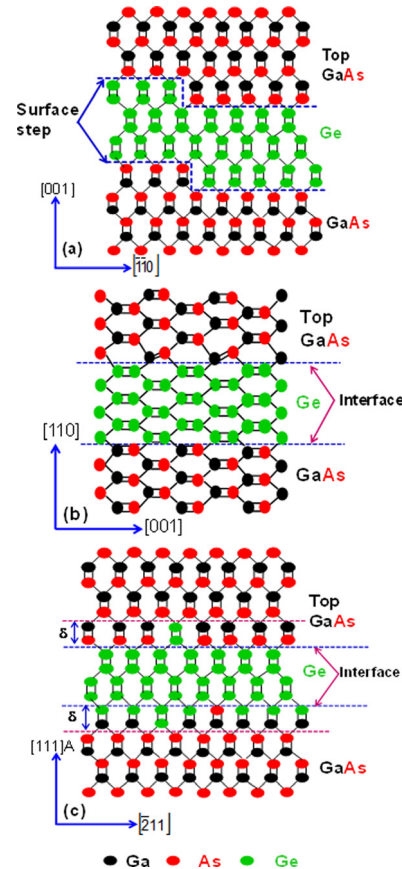


FIG. 16. (Color online) Lattice representation of (a) GaAs/Ge/(001)GaAs with 6° offcut toward [110] direction illustrates double atomic surface step which allows to eliminate APBs using MEE with arsenic prelayer during MBE growth (adapted from Ref. 40); (b) GaAs/Ge/(110)GaAs double heterojunction, and (c) GaAs/Ge/(111)A GaAs heterostructure. Dashed line signifies the interface plane in these schematics. In case of (b), every atomic plane of atoms parallel to the junction is neutral on average, corresponds to a nonpolar heterojunction and in case of (c) (adapted from Ref. 55), the two transition plane junction denoted by δ with the first plane 1/8 As and the second plane 7/8 Ga (adapted from Ref. 70).

TABLE III. Core-level to VBM binding-energy difference for epitaxial Ge and (110) GaAs.

Material and interface	Binding energy difference	Measured valence band offset, ΔE_V , of GaAs/Ge/(110) GaAs	
		Top GaAs/Ge interface	Bottom Ge/GaAs (110) interface
GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs} = 40.40 \pm 0.05$ eV	0.26 ± 0.05 eV	—
Thin GaAs on Ge	$E_{As3d_{5/2}}^{GaAs} - E_{Ge3d_{5/2}}^{Ge} = 11.10 \pm 0.05$ eV		
Thick Ge	$E_{Ge3d_{5/2}}^{Ge} - E_{VBM}^{Ge} = 29.56 \pm 0.05$ eV		0.57 ± 0.05 eV
Thin Ge on GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{Ge3d_{5/2}}^{Ge} = 11.42 \pm 0.05$ eV	—	
GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs} = 40.41 \pm 0.05$ eV		

results. Furthermore, this valence band offset relation holds good for the growth of GaAs on Ge which was grown on (100), (110), and (111)A GaAs substrates. Figure 15 shows the histogram of ΔE_V distribution obtained from GaAs/Ge/GaAs double heterostructures grown on (100)/6° GaAs, (110) GaAs, and (111) A GaAs substrates. The highest ΔE_V value for both upper and bottom interface of GaAs/Ge/GaAs was obtained on (111)A GaAs substrate. Table V shows the substrate orientation, surface reconstruction and band offset parameters of GaAs/Ge/GaAs heterostructures obtained from this work.

A great deal of attention has been devoted to the determination of ΔE_V of Ge on GaAs heterojunction; however, minimal work has been done on the determination of the band offset of GaAs on epitaxial Ge grown on different crystallographic GaAs substrates. It was believed due to the more challenging polar-on-nonpolar epitaxy of GaAs on Ge heterojunction. In all crystallographic orientations from this work and by other researchers,^{37,38,67} the measured ΔE_V of the GaAs/Ge heterointerface was lower by 0.20–0.3 eV from the inverse heterojunction where Ge layer was grown epitaxially on GaAs. In fact, this nonsymmetry is also observed in the AlAs-GaAs (Ref. 51) and ZnSe-Ge (Ref. 68) lattice matched systems. It is interesting to note that an average of 0.25 eV difference in ΔE_V was observed in the AlAs-GaAs(110)⁵¹ and ZnSe-Ge(110)⁶⁸ systems, where the lower ΔE_V always observed for the growth of high bandgap on low bandgap material than the inverse case. A possible mechanism for the growth of GaAs on Ge(110) is the APDs separated by antiphase boundaries (APBs)⁶⁹ and microscopic interface electrostatic dipole effects for AlAs-GaAs or Ge-ZnSe system⁶⁹ are the main cause to decrease the value of ΔE_V , respectively. The super-

rior surface morphology of GaAs on Ge(110) is due to the absence of surface reconstruction⁵² and the free-surface reconstruction of the (110) surface favors the subsequent layer growth without any APBs.⁵² However, from our RHEED pattern shown in Fig. 2(b) and also the work by Chang⁴² that the possible surface reconstructions of the Ge layer grown on GaAs(110) are (3 × 4), (2 × 3), (4 × 4), and (1 × 1). Kroemer *et al.*⁵⁵ argued that epitaxial growth of GaAs on a reconstructed Ge(110) surface closely resembles homoepitaxial growth on a GaAs(110) surface. This is indeed the case for the growth of GaAs on Ge/GaAs(110) where the lowest surface *rms* roughness was observed compared to other crystallographic orientations as shown in Fig. 4. This is quite different on polar surfaces, (100) or (111). The band structure at the semiconductor–semiconductor heterointerface, band bending with or without bias applied in the device structure, and contributions of interface dipoles are the dominant mechanisms for the difference in observed ΔE_V . Deviations from linearity (Ge on GaAs vs GaAs/Ge) correspond to interface dipole contributions⁵² in all surface orientations studied in this work. Figure 16 illustrates a lattice representation of (a) GaAs/Ge/(001)GaAs with 6° offcut toward [110] direction,⁴⁰ (b) GaAs/Ge/(110)GaAs double heterojunction, and (c) GaAs/Ge/(111)A GaAs heterostructures. In Fig. 16(b), every atomic plane of atoms parallel to the junction is neutral on average, corresponds to a nonpolar junction (adapted from Ref. 55), and in Fig. 16(c), the two transition plane junction is denoted by δ with the first plane 1/8 As and the second plane 7/8 Ga (adapted from Ref. 70). The different crystallographic orientations display a larger band offset than the different surface reconstruction or growth sequence found by other researchers.⁵² Thus, comparison of band offset

TABLE IV. Core-level to VBM binding-energy difference for Ge and (111)A GaAs.

Material and interface	Binding energy difference	Measured valence band offset, ΔE_V , of GaAs/Ge/(111)A GaAs	
		Top GaAs/Ge interface	Bottom Ge/GaAs (111)A interface
GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs} = 40.40 \pm 0.05$ eV	0.31 ± 0.05 eV	—
Thin GaAs on Ge	$E_{As3d_{5/2}}^{GaAs} - E_{Ge3d_{5/2}}^{Ge} = 11.19 \pm 0.05$ eV		
Thick Ge	$E_{Ge3d_{5/2}}^{Ge} - E_{VBM}^{Ge} = 29.52 \pm 0.05$ eV		0.61 ± 0.05 eV
Thin Ge on GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{Ge3d_{5/2}}^{Ge} = 11.72 \pm 0.05$ eV	—	
GaAs	$E_{As3d_{5/2}}^{GaAs} - E_{VBM}^{GaAs} = 40.63 \pm 0.05$ eV		

TABLE V. Summary of substrate surface construction, Ge layer surface reconstruction, upper GaAs surface reconstruction, and valence band discontinuities for top GaAs layer Ge and bottom Ge layer on various GaAs substrates orientations.

GaAs substrate surface and reconstruction	Ge surface reconstruction	Top GaAs surface reconstruction	ΔE_v (eV) of top GaAs/Ge	ΔE_v (eV) of bottom Ge/GaAs
(100)/6° (2 × 4)	(2 × 2)	c(2 × 4)	0.23 ± 0.05	0.42 ± 0.05
(110) (1 × 1)	(3 × 4)	(1 × 1)	0.26 ± 0.05	0.57 ± 0.05
(111)A (2 × 1)	(1 × 1)	(2 × 2)	0.31 ± 0.05	0.61 ± 0.05

between experiment and theory is undoubtedly exciting and our *in situ* grown Ge in an As-free environment for GaAs/Ge/GaAs heterostructures with crystallographic orientations using MBE provides a promising path for both p- and n-channel quantum well field effect transistor applications. To prevent the carrier spill-off to the upper barrier layer due to the lower ΔE_v at the upper GaAs/Ge interface compared to Ge/GaAs bottom interface, composite gate dielectric consists of GaAs and high-*k* layer (e.g., HfO₂, TaSiO_x) on upper GaAs would enable high-performance quantum well FETs for low-power and high-speed computing platforms.

IV. SUMMARY AND CONCLUSIONS

In conclusion, we have shown that high-quality epitaxial GaAs/Ge/GaAs heterostructures can be grown *in situ* on (100), (110), and (111)A GaAs substrates using two separate molecular beam epitaxy chambers, confirmed by RHEED intensity oscillation and x-ray diffraction. Sharp RHEED patterns from the surface of GaAs on epitaxial Ge/(111)A GaAs and Ge/(110)GaAs demonstrated a superior interface quality than on Ge/(100)GaAs. Atomic force microscopy reveals smooth and uniform morphology with surface roughness of Ge about 0.2–0.3 nm. Valence band offset of 0.23, 0.26, 0.31 eV for upper GaAs/Ge interface and 0.42, 0.57, 0.61 eV for bottom Ge/GaAs interface, respectively, have been derived from x-ray photoelectron spectroscopy data on GaAs/Ge/GaAs interfaces on (100), (110), and (111)A GaAs substrates. Using XPS data, variations in band discontinuities related to the crystallographic orientation is $\Delta E_v(111)Ga > \Delta E_v(110) > \Delta E_v(100)As$. Thus, the high-quality heterointerface and band offset for carrier confinement obtained in MBE grown GaAs/Ge/GaAs heterostructures can offer a promising virtual substrate technology integrated on Si substrate for extending the performance and application of Ge-based p- and n-channel quantum well field effect transistors.

ACKNOWLEDGMENT

This work was supported in part by Intel Corporation.

¹R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, *Nature Mater.* **6**, 810 (2007).

²International Technology Roadmap for Semiconductors (ITRS), 2011 edition, Process Integration, Devices, and Structures (PIDS) Chapter (2011).

³M. K. Hudait, *ECS Trans.* **45**, 581 (2012).

- ⁴M. K. Hudait et al., in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2007), p. 625.
- ⁵M. Radosavljevic et al., in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2009), p. 319.
- ⁶L. Ming, L. Haiou, T. C. Wah, and L. K. May, *IEEE Electron Device Lett.* **33**, 498 (2012).
- ⁷M. Radosavljevic et al., in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2008), p. 727.
- ⁸R. Pillarisetty et al., in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2010), p. 150.
- ⁹A. Nainani et al., in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2009), p. 857.
- ¹⁰J. B. Boos et al., *IEICE Trans. Electron.* **E91-C**, 1050 (2008).
- ¹¹Y. Sun, S. E. Thompson, and T. Nishida, *Strain Effect in Semiconductors: Theory and Device Applications*, 1st ed. (Springer, New York, 2010).
- ¹²M. V. Fischetti and S. E. Laux, *J. Appl. Phys.* **80**, 2234 (1996).
- ¹³J. Kim and M. V. Fischetti, *J. Appl. Phys.* **108**, 013710 (2010).
- ¹⁴Y. Zhang and M. V. Fischetti, in *13th International Workshop on Computational Electronics* (Beijing, China, 2009), p. 1.
- ¹⁵Y. Sun, S. E. Thompson, and T. Nishida, *J. Appl. Phys.* **101**, 104503 (2007).
- ¹⁶M. Uchida, Y. Kamakura, and K. Taniguchi, in *International Conference on Simulation of Semiconductor Processes and Devices* (Tokyo, Tokyo, Japan, 2005), p. 315.
- ¹⁷M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, *J. Appl. Phys.* **97**, 011101 (2005).
- ¹⁸B.-F. Hsieh and S.-T. Chang, *Solid State Electron.* **60**, 37 (2011).
- ¹⁹S. Dissanayake, Y. Zhao, S. Sugahara, M. Takenaka, and S. Takagi, *J. Appl. Phys.* **109**, 033709 (2011).
- ²⁰T. Low, M. F. Li, G. Samudra, Y. Yeo, C. Zhu, A. Chin, and D. Kwong, *IEEE Trans. Electron. Device* **52**, 2430 (2005).
- ²¹T. Krishnamohan, D. Kim, T. V. Dinh, A. Pham, B. Meinerzhagen, C. Jungemann, and K. Saraswat, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2008), p. 899.
- ²²S. Dissanayake, K. Tomiyama, S. Sugahara, M. Takenaka, and S. Takagi, *Appl. Phys. Express* **3**, 041302 (2010).
- ²³S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, *Appl. Phys. Lett.* **83**, 3516 (2003).
- ²⁴M. Yang et al., *IEEE Electron. Device Lett.* **24**, 339 (2003).
- ²⁵M. V. Fischetti, Z. Ren, P. M. Solomon, M. Yang, and K. Rim, *J. Appl. Phys.* **94**, 1079 (2003).
- ²⁶S. Takagi and M. Takenaka, *Jpn. J. Appl. Phys., Part 1* **50**, 010110 (2011).
- ²⁷K. Minami, Y. Nakamura, S. Yamasaka, O. Yoshitake, J. Kikkawa, K. Izunome, and A. Sakai, *Thin Solid Films* **520**, 3232 (2012).
- ²⁸C. H. Lee, T. Nishimura, N. Saido, K. Nagashio, K. Kita, and A. Toriumi, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2009), p. 457.
- ²⁹Y. J. Yang, W. S. Ho, C. F. Haung, S. T. Chang, and C. W. Liu, *Appl. Phys. Lett.* **91**, 102103 (2007).
- ³⁰S. Datta, M. K. Hudait, M. L. Docz, J. T. Kavalieros, A. Mazundar, J. K. Brask, B.-Y. Jin, M. Metz, and R. S. Chau, "Extreme high mobility CMOS logic," U.S. patent 8,183,556 (22 May 2012).
- ³¹R. R. King, *Nat. Photonics* **2**, 284 (2008).
- ³²M. Zhu, H. C. Chin, G. S. Samudra, and Y. C. Yeo, *J. Electrochem. Soc.* **155**, H76 (2008).
- ³³S. H. Tang, C. I. Kuo, H. D. Trinh, M. K. Hudait, E. Y. Chang, C. Y. Hsu, Y. H. Su, G.-L. Luo, and H. Q. Nguyen, *Microelectron. Eng.* **97**, 16 (2012).
- ³⁴S. Cho, I. M. Kang, T. I. Kamins, B.-G. Park, and J. S. Harris, Jr., *Appl. Phys. Lett.* **99**, 243505 (2011).
- ³⁵R. W. Grant, J. R. Waldrop, and E. A. Kraut, *J. Vac. Sci. Technol.* **15**, 1451 (1978).
- ³⁶E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Kowalczyk, *Phys. Rev. Lett.* **44**, 1620 (1980).
- ³⁷E. T. Yu, J. O. McCaldin, and T. C. McGill, *Solid State Phys.* **46**, 1 (1992).
- ³⁸A. Franciosi and C. G. Van de Walle, *Surf. Sci. Rep.* **25**, 1 (1996).
- ³⁹H. D. Trinh et al., *Appl. Phys. Lett.* **97**, 042903 (2010).
- ⁴⁰M. K. Hudait, Y. Zhu, N. Jain, S. Vijayaraghavan, A. Saha, T. Merritt, and G. A. Khodaparast, *J. Vac. Sci. Technol. B* **30**, 051205 (2012).
- ⁴¹Q. K. Xue, T. Hashizume, and T. Sakurai, *Prog. Surf. Sci.* **56**, 1 (1997).
- ⁴²C. A. Chang, *Appl. Phys. Lett.* **40**, 1037 (1982).
- ⁴³C. A. Chang and T. S. Kuan, *J. Vac. Sci. Technol. B* **1**, 315 (1983).
- ⁴⁴R. W. Grant, J. R. Waldrop, and E. A. Kraut, *Phys. Rev. Lett.* **40**, 656 (1978).

- ⁴⁵A. Y. Cho, *J. Appl. Phys.* **41**, 2780 (1970).
- ⁴⁶D. A. Woolf, D. I. Westwood, and R. H. Williams, *Semicond. Sci. Technol.* **8**, 1075 (1993).
- ⁴⁷W. T. Stacy and M. M. Janssen, *J. Cryst. Growth* **27**, 282 (1974).
- ⁴⁸Y. Bai, M. T. Bulsara, and E. A. Fitzgerald, *J. Appl. Phys.* **111**, 013502 (2012).
- ⁴⁹H. Kroemer, *Surf. Sci.* **132**, 543 (1983).
- ⁵⁰R. S. Bauer and J. C. Mikkelsen, *J. Vac. Sci. Technol.* **21**, 491 (1982).
- ⁵¹J. R. Waldrop, S. P. Kowalczyk, R. W. Grant, E. A. Kraut, and D. L. Miller, *J. Vac. Sci. Technol.* **19**, 573 (1981).
- ⁵²L. J. Brillson, *Surfaces and Interfaces of Electronic Materials* (Wiley-VCH, Germany, 2010).
- ⁵³P. Zurcher and R. S. Bauer, *J. Vac. Sci. Technol. A* **1**, 695 (1983).
- ⁵⁴W. Mönch, R. S. Bauer, H. Gant, and R. Murschall, *J. Vac. Sci. Technol.* **21**, 498 (1982).
- ⁵⁵H. Kroemer, K. J. Polasko, and S. C. Wright, *Appl. Phys. Lett.* **36**, 763 (1980).
- ⁵⁶G. A. Baraff, J. A. Appelbaum, and D. R. Hamann, *Phys. Rev. Lett.* **38**, 237 (1977).
- ⁵⁷Y.-C. Ruan and W. Y. Ching, *J. Appl. Phys.* **62**, 2885 (1987).
- ⁵⁸A. D. Katnani, P. Chiaradia, H. W. Sang, and R. S. Bauer, *J. Vac. Sci. Technol. B* **2**, 471 (1984).
- ⁵⁹T. Gabor, *J. Electrochem. Soc.* **111**, 817, 821, 825 (1964).
- ⁶⁰K. Morizane, *J. Cryst. Growth* **38**, 249 (1977).
- ⁶¹A. D. Katnani, P. Chiaradia, H. W. Sang, Jr., P. Zurcher, and R. S. Bauer, *Phys. Rev. B* **31**, 2146 (1985).
- ⁶²L. L. Sorba, G. Biasiol, G. Bratina, R. Nicolini, and A. Franciosi, *J. Cryst. Growth* **127**, 93 (1993).
- ⁶³G. Biasiol, L. Sorba, G. Bratina, R. Nicolini, A. Franciosi, M. Peressi, S. Baroni, R. Resta, and A. Baldereschi, *Phys. Rev. Lett.* **69**, 1283 (1992).
- ⁶⁴W. A. Harrison, *J. Vac. Sci. Technol.* **14**, 1016 (1977).
- ⁶⁵M. Cardona and N. E. Christensen, *Phys. Rev. B* **35**, 6182 (1987).
- ⁶⁶F. F. Fang and W. E. Howard, *J. Appl. Phys.* **35**, 612 (1964).
- ⁶⁷J. R. Waldrop, E. A. Kraut, S. P. Kowalczyk, and R. W. Grant, *Surf. Sci.* **132**, 513 (1983).
- ⁶⁸S. P. Kowalczyk, E. A. Kraut, J. R. Waldrop, and R. W. Grant, *J. Vac. Sci. Technol.* **21**, 482 (1982).
- ⁶⁹R. W. Grant, J. R. Waldrop, S. P. Kowalczyk, and E. A. Kraut, *J. Vac. Sci. Technol. B* **3**, 1295 (1985).
- ⁷⁰W. A. Harrison, E. A. Kraut, J. R. Waldrop, and R. W. Grant, *Phys. Rev. B* **18**, 4402 (1978).