Reliability Studies on High-temperature Operation of Mixed As/Sb Staggered Gap Tunnel FET Material and Devices

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***Abstract*—The reliability of structural and electrical properties of mixed As/Sb staggered gap tunnel field-effect transistors (TFETs) for high-temperature operation was investigated comprehensively from 25°C to 150°C. Temperature dependent x-ray measurements showed identical strain relaxation of the active region, indicating no additional dislocations were introduced at 150°C. Symmetric two-dimensional surface crosshatch patterns before and after annealing suggested no significant structural properties change during high temperature operation. No extra inter-diffusion of species at the source/channel heterointerface was observed at 150°C, confirmed by secondary ion mass spectrometry measurement. The leakage current of the fabricated reverse-biased p^+-i-n^+ diode increased exponentially with increasing temperature due to Shockley-Read-Hall generation-recombination mechanism. The ON-state drain current of the TFET device showed weak temperature dependence, and it decreased with increasing temperature from 25°C to 100°C due to the variation of Fermi distribution and the increase in channel resistance but increased from 100°C to 150°C due to the reduction of both bandgap energy as well as the effective tunneling barrier height. The subthreshold slope has a strong positive temperature dependent property especially at higher temperature due to trap-assisted tunneling process. These experimental results demonstrated stable structural properties and distinguished device characteristics of the mixed As/Sb staggered gap TFETs at higher operating temperature. The temperature dependent structural and device properties of the mixed As/Sb staggered gap TFET highlights the importance of the reliability on high temperature operation of TFETs for future low-power digital logic applications.**

***Index Terms*—Tunnel field effect transistor (TFET), high-temperature reliability, mixed As/Sb, staggered gap heterostructure**

I. Introduction

THE downscaling of Si metal-oxide semiconductor field-effect transistors (MOSFETs) faces immense challenges as it leads to increased power dissipation in current microprocessors. Due to the fundamental lower limit (60mV/dec at 300K) in the subthreshold slope (SS) for a traditional MOSFET, which relies on the thermionic emission transport mechanism, the reduction of threshold voltage would result in increase in OFF-state current (I_{OFF}) and static power consumption. Since interband tunneling field-effect transistors (TFETs) with gate-controlled Zener tunneling junction can achieve SS < 60 mV/dec and operate at lower supply voltage [1]-[3], they are considered as a promising candidate to replace Si MOSFET at low operating voltage for low-power logic operation. A major drawback of Si TFET is the low ON-state current (I_{ON}) [3]-[5]; however, III-V material based TFETs can achieve larger tunneling current due to smaller bandgap as well as lower effective carrier mass [5]-[7]. Additionally, some heterostructures can provide a staggered band alignment, allowing a steeper band structure profile over the source/channel junction than that achievable by doping modulation only [7], [8]. Among them, mixed As/Sb based heterostructures namely, $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ allow a wide range of bandgaps and staggered band alignments depending on the alloy compositions in the source and channel materials [9]-[12]. Band alignments at the source/channel heterointerface can be tailored-made by carefully controlling the compositions of the mixed As/Sb material system [11]. As a result, the mixed As/Sb staggered gap TFET is considered as a promising option for high-performance, low standby power and energy efficient logic application.

In practice, there is a growing demand for higher temperature tolerance of the logic transistors in aircraft, automotive, space technology and for very-large-scale integration application [13], [14]. This leads to the necessity for the transistors to be operated at high temperature working environment without degradation of the device performance. However, for the mixed As/Sb staggered gap TFET structures, due to large lattice mismatch between active layers ($GaAs_{1-y}Sb_y/In_xGa_{1-x}As$) and the substrate, there will be some residual strain exists within the active region [9]. The residual strain tends to relax during high temperature operation, which will generate dislocations in these layers. Furthermore, fixed charges caused by defects and dislocations at the heterointerface [9] will convert the energy band alignment from staggered gap to broken gap [11], which will drastically increase the I_{OFF} and decrease I_{ON}/I_{OFF} ratio [11]. Moreover,

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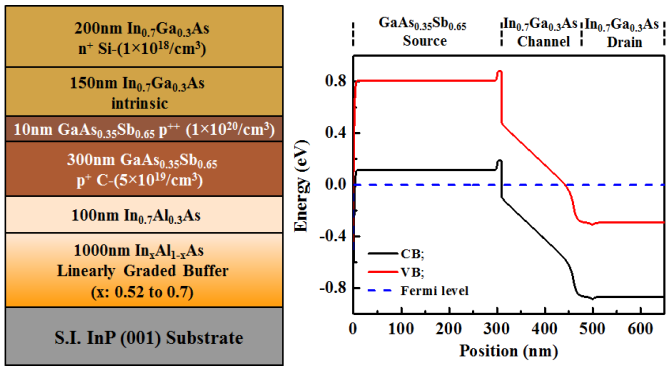

Figure 1 (a) Schematic diagram of n-channel TFET layer structure. (b) Energy band diagram of the structure. The 10nm p^{++} heavily C doped GaAsSb layer is clearly shown in the band diagram.

the high temperature operation may aggravate the intermixing of Sb and As at the $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ heterointerface that will result in uncontrolled layer composition, which will lead to uncontrolled band alignment and may introduce high dislocation density due to compositional mismatch. Besides, high temperature operation may lead to decrease in bandgap of materials in the active layers as well as increase in channel resistance [15], both of which will influence the ON-state performance of TFET devices [6]. Furthermore, due to the enhanced Shockley-Read-Hall (SRH) generation-recombination (G-R) and the increased traps assisted tunneling (TAT) process during high temperature operation [6]-[8], [16], I_{OFF} may be significantly increased compared with that at room temperature. Although, there have been some earlier reports on the temperature dependent characteristics of homojunction TFETs [6], [7], [15], [16], no high operation temperature studies of mixed As/Sb TFET devices were reported in the literature. Therefore, it is necessary to perform a comprehensive experimental investigation on the reliability of mixed As/Sb staggered gap heterojunction TFET materials and devices for high temperature operation.

In this work, both the structural properties and device performances of a $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ staggered gap TFET in the temperature range of 25°C to 150°C were thoroughly investigated. Experimental results showed that the relaxation state, surface morphology and depth profiles of the TFET structure were kept stable during the high temperature operation up to 150°C. The electrical performance of the fabricated TFET devices showed distinguished features over homojunctions with changing temperature. These reliability studies of high-temperature operation of mixed As/Sb staggered gap tunnel FET material and devices will contribute to better understanding the operation principles within these devices at high operating temperature and will provide important guidance on the material growth optimization and device fabrication for future TFETs.

II. Experimental

$GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ n-channel TFET structure was

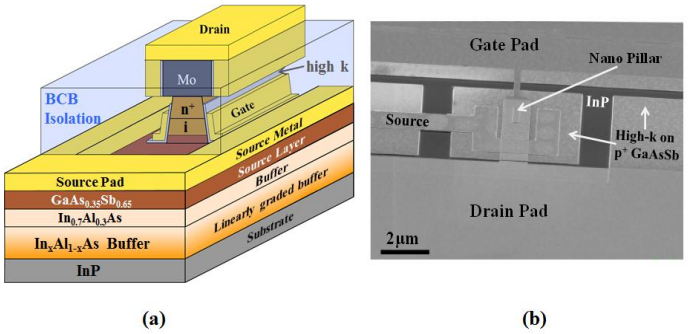

Figure 2 (a) Schematic of self-aligned gate nano-pillar staggered gap TFET device and (b) tilted view SEM micrograph of the TFET device.

grown by solid source molecular beam epitaxy (MBE) on semi-insulating (100) InP substrate and the schematic of the layer structure was shown in Fig. 1 (a). Figure 1 (b) shows the energy band diagram of this TFET structure. The 10nm p^{++} $GaAs_{0.35}Sb_{0.65}$ layer with heavily carbon (C) doping of $1\times10^{20}/cm^3$ in the source region was used to create abrupt doped junction and thus increase tunneling probability [7]. The detailed growth process can be found elsewhere [9]. Temperature dependent x-ray diffraction (XRD) measurements were performed on this structure from 25°C to 150°C with 25°C as a temperature step. Reciprocal space maps (RSMs) from both symmetric (004) and asymmetric (115) reflections were recorded to characterize the strain relaxation properties of the TFET structure at each temperature step. In order to quantify the change of relaxation states after high temperature operation at 150°C, RSMs were repeated on the same sample at 25°C. The XRD measurements were carried out using Panalytical X'pert Pro system with Cu Kα1 line focused x-ray source. Contact mode atomic force microscopy (AFM) was used to characterize the surface morphology of the TFET structure before and after temperature cycle. Dynamic secondary ion mass spectrometry (SIMS) using Cameca IMS-7f GEO with Cs^+ as primary ion beam was used to determine the compositional profile, the change of doping concentration and the atomic intermixing. Nano-pillar TFET devices using self-aligned metal gate were fabricated from the structure shown in Fig. 1(a). The detailed TFET fabrication process flow can be found elsewhere [9], [17]. A 3D schematic diagram of fabricated nano-pillar TFET device and the corresponding tilted view scanning electron microscopy (SEM) micrograph of such device were shown in Fig. 2(a) and 2(b), respectively. The current-voltage (I-V) characteristics of the reverse-biased p^+-i-n^+ diode, which determines the OFF-state current of the TFET device [16], were measured with temperature ranging from 25°C to 150°C, using 25°C as a step. In order to determine the switching properties of the TFET device at different temperature, transfer characteristics (I_{DS}-V_{GS}) of the TFET was carried out from 25°C to 150°C. Moreover, the p^+-i-n^+ leakage current and the transfer characteristics were also measured at 25°C after temperature cycle to determine the effect of high temperature operation on the performance of TFET device.

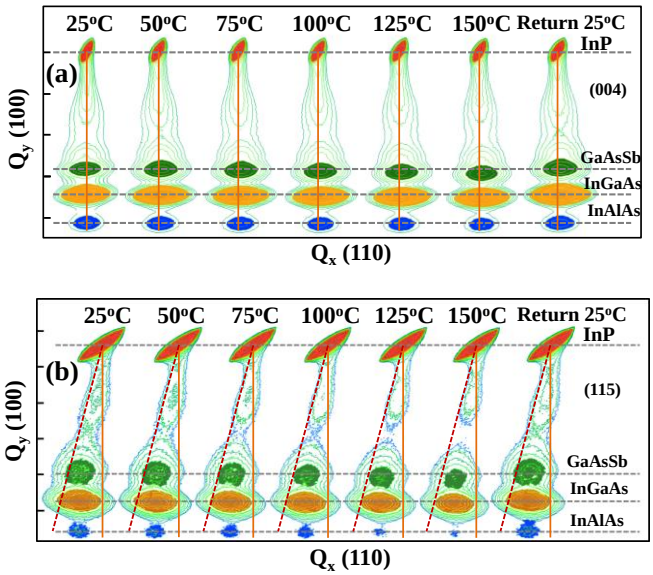

Figure 3 (a) Symmetric (004) and (b) asymmetric (115) reciprocal space maps of the TFET structure at different temperature. Similar strain relaxation values were extracted from RSMs at different temperatures, indicating the strain relaxation properties of this structure keep stable up to 150°C.

TABLE I
SUMMARY OF STRAIN RELAXATION VALUES OF EPILAYERS WITH RESPECT TO INP SUBSTRATE AT DIFFERENT TEMPERATURES.

Temperature	Strain Relaxation Values (%)		
	$In_{0.7}Ga_{0.3}As$	$GaAs_{0.35}Sb_{0.65}$	$In_{0.7}Al_{0.3}As$
25°C	75	81	72
50°C	79	83	74
75°C	78	82	73
100°C	72	81	70
125°C	77	84	74
150°C	71	80	69
Back to 25°C	74	84	71

III. RESULTS AND DISCUSSION

A. *Strain Relaxation properties*

The relaxation state and residual strain of epilayers at each temperature step were obtained from symmetric (004) and asymmetric (115) reflections of RSMs. For each measurement, a 5 minutes pause was used to allow the temperature to increase and stabilize at a preselected value. The temperature was kept constant during the entire period of (004) and (115) x-ray data acquisition at each temperature step. Figures 3 (a) and 3 (b) showed symmetric (004) and asymmetric (115) RSMs of the structure at different temperatures steps, respectively. Each layer was labeled to its corresponding reciprocal lattice point (RLP) based on earlier performed wet chemical etching experiments [9]. It can be seen from Fig. 3 (a) and 3 (b) that four distinct RLP maxima were shown in symmetric (004) and asymmetric (115) RSMs at each temperature step, corresponding to (1) the InP substrate, (2) $GaAs_{0.35}Sb_{0.65}$ source layer, (3) $In_{0.7}Ga_{0.3}As$ channel/drain layer, and (4) the 100nm $In_{0.7}Al_{0.3}As$ uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer. The $In_{0.7}Al_{0.3}As$ uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer, the $GaAs_{0.35}Sb_{0.65}$ source layer and the $In_{0.7}Ga_{0.3}As$ channel/drain layer were designed to be internally lattice matched in this TFET structure as shown in Fig. 1(a). However, high indium (In) composition in the $In_xAl_{1-x}As$ buffer inhibits high growth temperature during MBE growth process due to the higher surface ad-atoms mobility of In. Thus, the graded buffer grown at low temperature was no longer to be expected as nearly fully relaxed since the threading dislocations density velocity was reduced [18]. This will lead to certain amount of residual strain present within the layer [18]. Moreover, due to heavily C doping caused lattice contraction in the $GaAs_{0.35}Sb_{0.65}$ layer [9] and the compositional fluctuation [19] during MBE growth, the $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ layers were pseudomorphic respect to the $In_{0.7}Al_{0.3}As$ buffer layer rather than internally lattice matched. As a result, epilayers with different materials were shown in separated RLPs. The residual strain within the $In_{0.7}Al_{0.3}As$ buffer layer and the pseudomorphic nature of $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ active layers at room temperature were confirmed from the measured (004) and (115) RSMs. The strain relaxation value of the $In_{0.7}Al_{0.3}As$ buffer was calculated to be 72% with respect to the InP substrate at 25°C, leaving a strain value of 1.29%. In addition, only ~10% strain relaxation was extracted from the $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ layers with respect to $In_{0.7}Al_{0.3}As$ "virtual substrate" at 25°C.

In order to determine if the residual strain presents within the $In_{0.7}Al_{0.3}As$ buffer and the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ layers will relax during high temperature operation, analysis were performed at each temperature step using the symmetric (004) and asymmetric (115) RSMs. The detailed analysis procedure at room temperature was reported earlier [9]. Similar strain relaxation values at each temperature step (~ 75% for $In_{0.7}Ga_{0.3}As$, ~ 82% for $GaAs_{0.35}Sb_{0.65}$ and ~ 72% for $In_{0.7}Al_{0.3}As$) as those at 25°C from each epilayer respect to InP substrate were extracted. The calculated strain relaxation values were summarized in Table I. The nearly identical strain relaxation states of each epilayer at different temperature steps indicate that the pseudomorphic nature of $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ layers were well maintained and negligible residual strain was relaxed during the high temperature operation. It also indicates that no extra dislocations caused by strain relaxation should be expected during high temperature operation up to 150°C. The similar strain relaxation state of each epilayer during high temperature operation is also supported by comparing the position of each RLP with respect to the fully relaxed line (the red dashed line) in (115) RSMs at different temperature steps. As shown in Fig. 3 (b), almost the same distance from the center of each RLP to the fully relaxed line was observed at different temperature, indicating nearly identical strain relaxation states of each layer. It can also be seen from Fig. 3 (a) that the RLPs of epilayers were marginally moving away from the InP substrate with increasing temperature. This may be caused by the lattice constant change at higher temperature measurement. The change of lattice parameter of each epilayer recovered after the sample was cooled down to room temperature, which can be

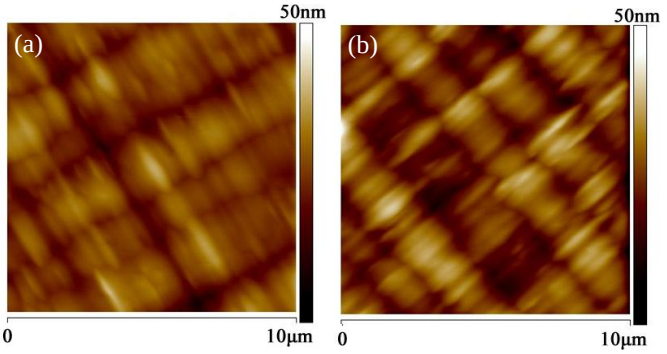

Figure 4 10μm × 10μm AFM surface morphology of the TFET structure (a) before temperature cycle with *rms* roughness of 3.17nm and (b) after temperature cycle with *rms* roughness of 2.66nm. Typical crosshatch patterns were observed in both cases. The well maintained crosshatch pattern and similar surface morphology after the temperature cycle suggests no significant structural properties change was generated in the structure up to 150°C.

confirmed by the RSMs recorded after the temperature cycle. The intensity of each RLP was decreased at high temperature and it was caused by the small displacements of atoms due to thermal vibrations [20]. In fact, the reduction of intensity was recovered when the sample was cooled down to room temperature after temperature cycle. Furthermore, the identical features of (004) and (115) RSMs before and after the temperature cycle measured at 25°C indicate that the strain relaxation properties of this structure does not affect by the high temperature operation up to 150°C.

B. *Surface morphology*

Since the surface crosshatch pattern relates to the strain relaxation properties of the structure, characterization of the surface morphology is an important metric for metamorphic TFET structures. In fact, the studies of surface morphology variation before and after high temperature operation of the TFET structure will help us to understand the variation of relaxation states and the stability of structural properties. The 10μm × 10μm AFM micrographs of the TFET structure before and after temperature cycle were shown in Fig. 4 (a) and 4 (b), respectively. From Fig. 4 (a) and 4 (b), the anticipated two-dimensional (2-D) crosshatch patterns were well developed and quite uniform, as expected for ideal graded buffer [21], [22], from both surfaces before and after high temperature operation. The undulating surface morphology exhibits ridges and grooves parallel to the [110] and [1$\bar{1}$0] directions and the uniform distribution of the crosshatch pattern along the [110] and [1$\bar{1}$0] directions indicates a symmetric relaxation of the linearly graded buffer [9]. Moreover, the well maintained 2-D crosshatch patterns and similar surface morphology after the high temperature cycle also suggests that the strain within the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ layers were not relaxed during the high temperature operation. Otherwise, dislocations would be formed in these layers and the 2-D crosshatch pattern developed by the graded buffer will be sheltered by high density dislocations and a grainy texture with higher surface roughness will be expected [9]. The surface root-mean-square (*rms*) roughness before and after temperature cycle were measured to be 3.17nm and 2.66nm, respectively. Despite of the experimental error, the surface was smoother after high temperature operation. Similar improvements of crystalline quality by high temperature annealing on metamorphic structures were also reported by other researchers where the lattice reformation might have resulted in the improvements in the structural quality [23]-[25]. In our case, although the annealing temperature was limited to 150°C, the sample was kept at the specific temperature for long time (~ 2 hours) during the collection of RSMs data at each temperature step. The annealing temperature was not set high to relax the residual strain within the epilayers, however, some defects (i.e., point defects) might have annihilated during the long annealing duration by the redistribution of atoms and hence improve the surface morphology. In fact, the improvement of crystalline quality by reduction of defects was also confirmed by the decrease of the p^+-i-n^+ leakage current of the fabricated TFET devices, which will be disused in *Sec. III D* of this paper.

C. *SIMS depth profiles*

There could be a potential concern of the mixed As/Sb staggered gap TFET devices for high temperature operation due to the possible intermixing between As and Sb atoms at the source/channel heterointerface. The intermixing between different atoms will be more promoted at higher temperature due to the enhanced ad-atoms diffusion. The intermixing of As and Sb at the heterointerface will lead to uncontrolled layer composition, which will result in the change of band alignment as well as the deterioration of device performance [11]. Besides, high temperature operation may also cause the diffusion of dopant atoms (C) from heavily doped $GaAs_{0.35}Sb_{0.65}$ source to the intrinsic $In_{0.7}Ga_{0.3}As$ channel layer. This will reduce the abruptness of the doping profile at the tunnel junction, which will in turn reduce the tunneling probability and lead to decrease in I_{ON} of the TFET devices [6], [7]. In order to determine the influence of high temperature operation on the junction and doping profiles of the TFET structure, dynamic SIMS measurements were performed to characterize the compositional profiles of As, Sb, Ga, In, Si and C atoms at the interface before and after temperature cycle. Figure 5 (a) showed Ga, In, As and Sb depth profiles of the TFET structure before temperature cycle, which displayed an abrupt $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface. The transition between $GaAs_{0.35}Sb_{0.65}$ to $In_{0.7}Ga_{0.3}As$ was less than 10nm, within the sputter-induced broadening of the ion beam, indicating low value of As and Sb intermixing at the heterointerface. Figure 5 (b) showed the C and Si doping profiles in the source and drain regions of the TFET structure. It depicted an abrupt junction profile at the source/channel interface with an expected C pocket doping concentration of $\sim 1\times10^{20}/cm^3$. Similarly, the Ga, In, As, Sb depth profiles and C, Si doping profiles after the temperature cycle were shown in Fig. 6 (a) and 6 (b), respectively. Almost identical, sharp junction and abrupt doping profile as that before the temperature cycle were obtained, which indicated

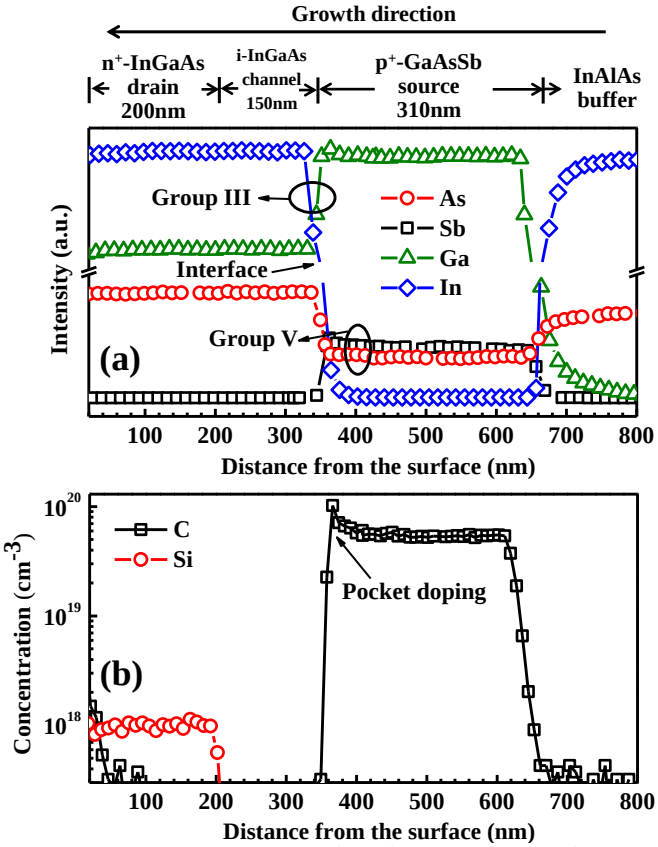

Figure 5 (a) Dynamic SIMS depth profiles of Ga, In, As and Sb of the TFET structure before temperature cycle. An abrupt $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ interface with a transition less than 10nm was confirmed. (b) Doping concentration profiles of C in the source and Si in the drain region before temperature cycle. An abrupt doping profile was observed at the interfaces.

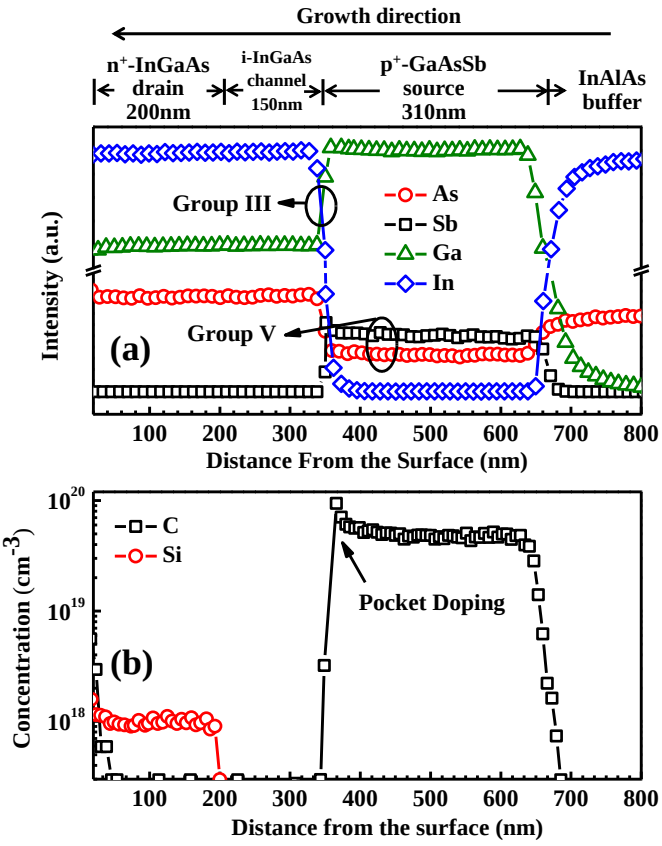

Figure 6 (a) Dynamic SIMS depth profiles of Ga, In, As and Sb of the TFET structure after temperature cycle. (b) Doping concentration profiles of C in the source and Si in the drain region after temperature cycle. The junction and doping profiles were similar as those before temperature cycle, indicating no detectable intermixing was taken place within the heterointerface up to 150°C.

that no detectable intermixing was taken place within the heterointerface up to 150°C. The stability of junction profiles assured the anticipated staggered band alignment with desired effective tunneling barrier height (E_{beff}) and sharp tunnel junction interface with minimal tunneling width for the TFET to operate at high temperature.

D. OFF-state leakage properties

One of the main attractions of TFET devices is their potential to reduce the OFF-state leakage current and lower the standby power dissipation in the circuits. Theoretically, the I_{OFF} of TFET can be extremely low due to the lack of final states at appropriate energies for tunneling at OFF-state [26]. However, in reality, SRH G-R [16], TAT [8] and even direct BTBT [9] process can contribute to I_{OFF} of TFET, all of which will deteriorate the device performance. Both the SRH G-R and TAT process were strongly temperature dependent [6], [8], [9], [16]; as a result, the I_{OFF} will be amplified at higher temperature, which may lead to the TFET devices losing their effectiveness at high operating temperature. Thus, the OFF-state transport mechanism of the mixed As/Sb staggered gap TFET should be investigated and the OFF-state current of the device at different working temperature should be measured to evaluate the reliability of the TFET device for high temperature operation.

In order to gain insight into the OFF-state transport mechanism of the TFET device, temperature dependent current-voltage (I-V) measurements were carried out on the reverse-biased p^+-i-n^+ diode with temperature ranging from 25°C to 150°C. Besides, the measurement was repeated at 25°C on the same device after the temperature cycle to determine the influence of the temperature cycle on the OFF-state performance. Figure 7 (a) showed the measured leakage current of the reverse-biased p^+-i-n^+ diode at different temperature steps. It can be seen from this figure that at each fixed reverse-bias, the leakage current increased exponentially with increasing temperature, as expected. The variation tendency of I_{OFF} with temperature was consistent with the SRH-dominated OFF-state transport mechanism, within which the main contribution to the temperature dependent factor arises from the intrinsic carrier concentration which is proportional to $\exp(-E_G/2kT)$, where E_G is the bandgap energy of active layers materials, k is the Boltzmann constant, and T is the temperature. In order to confirm this proposition, numerical simulations were performed using a SRH G-R model to determine the OFF-state transport of the TFET device. All simulations were performed using Sentaurus [27] with temperature ranging from 25°C to 150°C. As shown in Fig. 7 (a) (solid lines), the simulated I-V characteristics of the

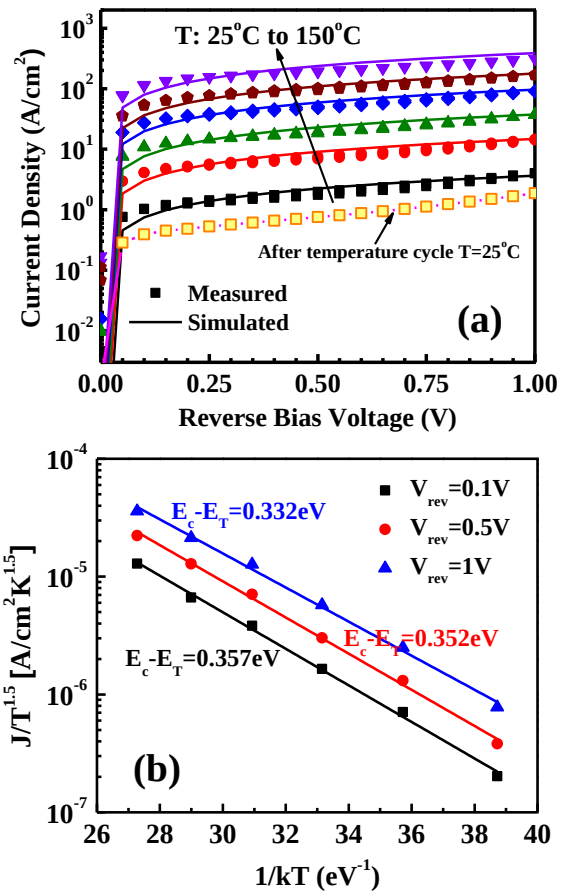

Figure 7 (a) Measured and simulated I-V characteristics of the reverse-biased p^+-i-n^+ diode with temperature ranging from 25°C to 150°C and (b) an extraction of the activation energy for the leakage current. The activation energy was between $E_G/2$ of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, indicating SRH G-R from both mid-gap interface traps and mid-gap bulk traps dominate the OFF-state transport of the TFET devices.

reverse-biased p^+-i-n^+ diode is in agreement with the measured data (scattered line) at all temperatures, suggesting the validation of this model. The SRH-dominated OFF-state transport mechanism was also confirmed by the Arrhenius plot, shown in Fig. 7 (b). The extracted activation energy is 0.33eV, 0.35eV, and 0.36eV at a reverse-bias of 1V, 0.5V, and 0.1V, respectively. All of these values were approximately $E_G/2$ of $In_{0.7}Ga_{0.3}As$ (~ 0.6eV at 300K) and $GaAs_{0.35}Sb_{0.65}$ (~ 0.72eV at 300K), indicating I_{OFF} components of SRH G-R were from both mid-gap interface traps and mid-gap bulk traps.

Different from the results reported by other researchers within the homojunction TFETs, where a combined SRH G-R and TAT mechanism dominated the OFF-state transport of the devices and the activation energy is much less than $E_G/2$ [6], [28], in the present study, the SRH G-R mechanism was the only dominated factor to control the I_{OFF} at temperature up to 150°C. The removal of tunneling component from the I_{OFF} may be benefitted from the staggered gap alignment of mixed As/Sb heterojunction at source/channel interface. The staggered band alignment of this heterojunction with an effective tunneling barrier ($E_{beff} = E_C^{Channel} - E_V^{Source}$) of 0.21eV was confirmed by x-ray photoelectron spectroscopy (XPS) measurements at room temperature [11], [12]. This E_{beff} would provide high ON-state tunneling current at low gate voltage [5], [29]; in the meanwhile, it will also effectively block tunneling at OFF-state condition. Moreover, the staggered band alignment was preserved up to 150°C since the OFF-state leakage current has a single slope with temperature. Otherwise, a broken band alignment will be formed and a direct BTBT mechanism will dominate the OFF-state transport, where a much higher leakage current with weak temperature dependence would be expected [9], [11].

It is interesting to find that the room temperature leakage current of the reverse-biased p^+-i-n^+ diode was reduced by almost 2× after the temperature cycle. This may be due to removal of some deep level traps during high temperature operation. The G-R centers in the mid-gap of bulk materials and within the depletion region of each junction were reduced by atom reformation during the long duration of temperature cycle [23], which will reduce the contribution of SRH G-R current. The improvement of crystalline quality can also be supported by the reduction of *rms* roughness after temperature cycle discussed earlier.

E. Transfer characteristics

The transfer characteristics (I_{DS}-V_{GS}) of TFETs showed distinguished features over traditional MOSFETs due to the distinct transport mechanism for TFETs at both ON and OFF-states. In order to gain insight into the reliability of the switching properties of the mixed As/Sb staggered gap TFETs at high operating temperature, transfer characteristics of these TFET devices were measured at both V_{DS} = 0.05V and 0.5V from 25°C to 150°C using 25°C as a temperature step.

Figure 8 (a) showed the transfer characteristics of the TFET device measured at V_{DS} = 0.05V with different temperature. As shown in this figure, at low gate voltages (<-0.3V), the drain current was almost constant without gate modulation, which set the leakage floor of the device, and increased exponentially with rising temperature. With increasing gate voltages from -0.3V to 0.4V, the I_{DS} was less temperature dependent, which indicated that the BTBT current was becoming the dominant current component. For V_{GS} > 0.4V, I_{DS} is weak temperature dependent and it corresponds to the drive current (I_{DR}) of the TFET. In order to further study the impact of high operating temperature on I_{DR}, the I_{DS}-V_{GS} characteristics was re-plotted in a linear scale with V_{GS} from 1.0V to 1.5V, which was shown in Fig. 8 (b). As shown in Fig. 8 (b), I_{DR} has a weak temperature dependent characteristics corresponding to the BTBT current at ON-state condition. The inset of Fig. 8 (b) shows the changing trend of I_{DS} with temperature at V_{GS} = 1.5V. It is interesting to find that I_{DS} was decreasing with rising temperature from 25°C to 100°C, but increasing from 100°C to 150°C. The former trend of I_{DS} can be explained by the variation of Fermi distribution with temperature and the latter can be explained by the reduction of bandgap energy of active region materials as well as the decrease of effective tunneling barrier height. According to

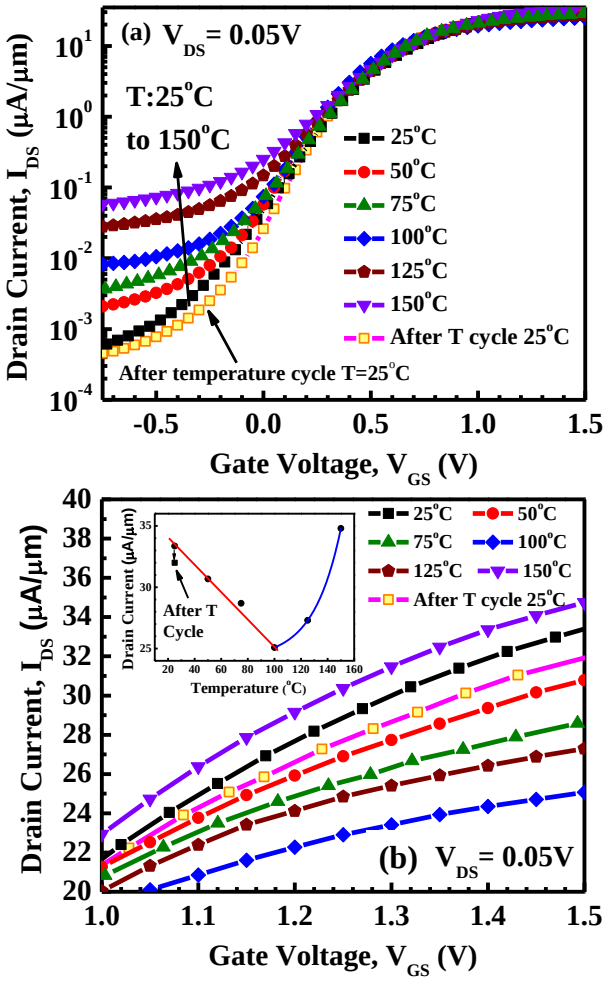

Figure 8 (a) Transfer (I_{DS}-V_{GS}) characteristics of the TFET devices at V_{DS} = 0.05V with I_{DS} in a log scale from 25°C to 150°C. (b) I_{DS} (V_{GS} from 1.0V to 1.5V) of the TFET devices at V_{DS} = 0.05V with I_{DS} in a linear scale from 25°C to 150°C. The inset shows the changing trend of I_{DS} with temperature at V_{GS} = 1.5V. I_{DS} decreases from 25°C to 100°C due to the variation of Fermi distribution with temperature but increases from 100°C to 150°C due to the reduction of E_G.

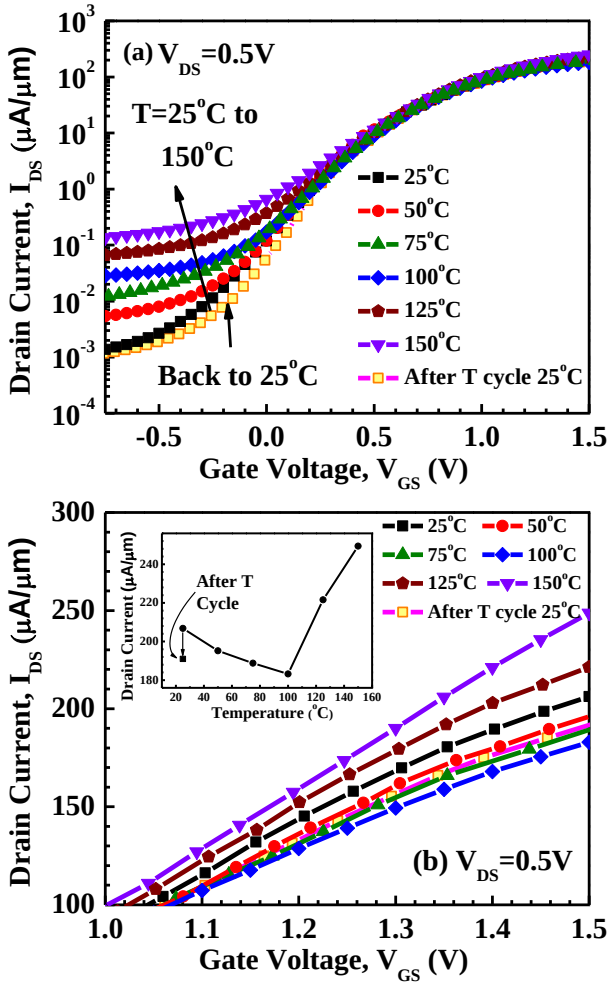

Figure 9 (a) Transfer (I_{DS}-V_{GS}) characteristics of the TFET devices at V_{DS} = 0.5V with I_{DS} in a log scale from 25°C to 150°C. (b) I_{DS} (V_{GS} from 1.0V to 1.5V) of the TFET devices at V_{DS} = 0.5V with I_{DS} in a linear scale from 25°C to 150°C. The inset shows the changing trend of I_{DS} with temperature at V_{GS} = 1.5V. Similar I_{DS} changing trend with temperature was observed as that with V_{DS} = 0.05V.

Knoch *et al.* [30], the tunnel junction acts as a band-pass filter allowing only carriers with energies around the Fermi level in an energy window $\Delta\phi = E_V^{Source} - E_C^{Channel}$ to tunnel from source to channel. With increasing temperature, more electrons will be excited to higher energy states, which lead to the decrease in electrons with energies around Fermi level within ΔΦ, which further results in the reduction of I_{DS} with increasing temperature. Moreover, the source region of TFET is highly degenerated due to heavily p-type doping, which can be seen from Fig. 1 (b). Thus, the degeneracy reduces the number of electrons available for tunneling which reduces the ON-state current and degraded the SS [2], [31]. In addition, due to the temperature dependence of the Fermi tail caused by heavily p-type doping, the degradation of ON-state current will be more pronounced at high temperature that leads to additional ON-state current loss. However, at higher temperature of greater than 100°C, the energy window ΔΦ will be enlarged by the decrease of bandgap energies of the source/channel materials [15]. Furthermore, according to Kane's model [32], the I_{DR} of TFET is directly related to the BTBT generation rate G_{BTBT}, which is exponentially related to $-(E_G)^{3/2}$. The exponential factor of E_G predominantly determines the G_{BTBT} on E_G and contributes to the increase of I_{DR} with rising temperature from 100°C to 150°C. The increased I_{DR} due to reduction of E_G of active region materials may dominant over variation of Fermi distribution from 100°C to 150°C. In addition, the E_{beff} will also reduce due to the reduction of bandgap [16], which may provide extra increase in I_{DR} at higher temperature of operation.

Figure 9 (a) shows the transfer characteristics of the same TFET device measured at V_{DS}=0.5V with different temperature. As shown in this figure, I_{DR} is about 1 order higher than that with V_{DS}=0.05V (as shown in Fig. 8a), as expected, at each temperature step, which is due to the enhanced electrical field at the tunneling junction brought by higher drain voltage. Similarly, at V_{DS}=0.5V, the OFF-state leakage floor showed strong temperature dependence and the I_{DR} displayed weak temperature dependence, which indicate that the SRH G-R mechanism and the BTBT processes, respectively, dominated the OFF-state and ON-state transport of the TFET device. In order to gain better insight into the

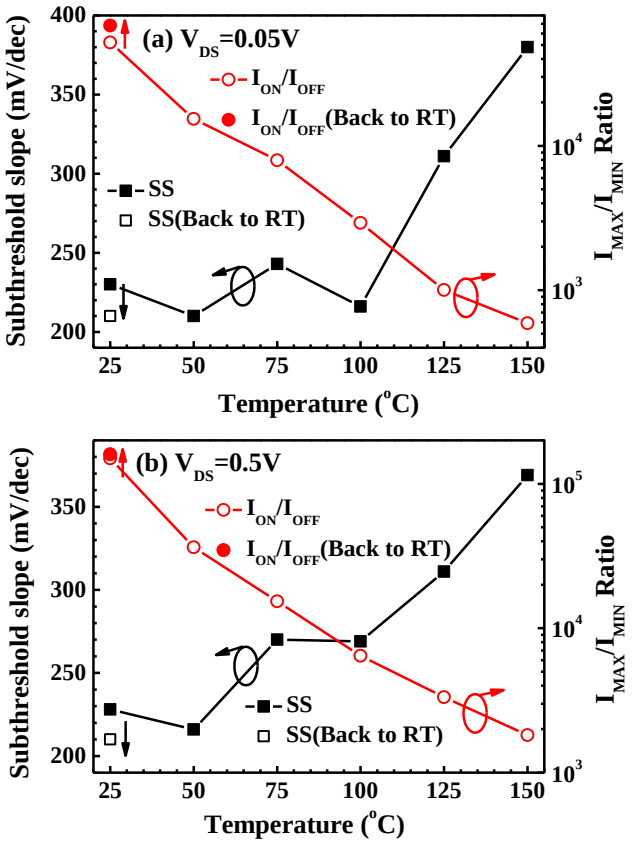

Figure 10 Changing of subthreshold slope and I_{MAX}/I_{MIN} ratio of the TFET devices with temperature for (a) V_{DS} = 0.05V and (b) V_{DS} = 0.5V. The strong temperature dependence of SS at high temperature (> 100°C for V_{DS} = 0.05V and > 75°C for V_{DS} = 0.5V) may be caused by trap-assisted tunneling by mid-gap traps. The I_{MAX}/I_{MIN} ratio decreased from ~ 10^5 at 25°C to ~ 10^3 at 150°C. This degradation of device performance was mainly caused by the high leakage current at high temperature.

impact of temperature on I_{DR}, the I_{DS}-V_{GS} characteristics of the TFET device was re-plotted in Fig. 9 (b) with V_{GS} from 1.0V to 1.5V in a linear scale. The inset of Fig. 9 (b) shows the changing trend of I_{DS} with temperature at V_{GS} = 1.5V. Nearly identical changing trend of I_{DR} with temperature at V_{DS} = 0.5V and V_{DS} = 0.05V was obtained, indicating that the temperature has similar effect on the transport mechanism at 0.05V and 0.5V drain voltages. The I_{DS} is not increasing exponentially with temperature from 100°C to 150°C, different with the case of V_{DS}=0.05V. This might be due to an enhanced electrical field inside the channel brought by the higher drain voltage. Moreover, the enhanced electrical field leads to a larger voltage drop over the channel due to increased channel resistance at a higher temperature of >100°C. As a result, the exponential increase trend of I_{DS} dominated by the reduction of E_G is not as remarkable as that with V_{DS} = 0.05V. Furthermore, the I_{DS}-V_{GS} measurements on the same device at 25°C showed similar performance before and after temperature cycle operation both at V_{DS} = 0.05V and 0.5V. It also suggests that no significant structural properties change, such as strain relaxation, inter-diffusion etc., took place during high temperature operation up to 150°C within the TFET structure. The I_{OFF} of the TFET device was reduced after the temperature cycle due to the removal of some trap states. It should be noted that, in this study, the fabricated device geometry has not been scaled significantly (T_{body} = 500nm and T_{oxe} = 2nm), and I_{DS} at V_{GS} = 0.5V is limited to 10μA/μm. Further scaling in device geometry and interface states density (D_{it}) will enable high I_{DS} with V_{GS} = 0.5V [5]. Thus, in order to investigate the influence of temperature on the drive current of TFETs, the large overdrive voltage of V_{GS} = 1.5V is used in this study.

Figure 10 (a) and (b) showed the SS and I_{MAX}/I_{MIN} ratio (I_{MAX} is I_{DS} at V_{GS} = 1.5V and I_{MIN} is I_{DS} at V_{GS} = -0.5V) of the TFET device as a function of temperature for V_{DS}=0.05V and 0.5V, respectively. The value of SS was not sub-60mV/dec due to high mid-gap traps and surface charges at the channel/high-κ oxide interface. These interface traps and surface charges can retard the Fermi-level movement of the intrinsic channel controlled by V_{GS}, and they can also result in TAT and the subsequent thermal emission [16], [28], all of which will degrade SS. For both V_{DS} = 0.05V and 0.5V, SS was almost constant with temperature up to 100°C, but increases sharply at temperature greater than 100°C and it has a strong positive temperature dependent coefficient from 100°C to 150°C. The strong temperature dependence of SS, which was also reported by other researchers [8], [16], [28], is caused by TAT in the subthreshold region, in which the electrons in the valence band of p^+ $GaAs_{0.35}Sb_{0.65}$ source tunneled into the mid-gap traps and followed by a subsequent thermal emission into the conduction band of $In_{0.7}Ga_{0.3}As$ channel, which gives rise to the strong temperature dependence as well as deterioration of SS. In order to improve the SS, surface chemical passivation is essential to suppress these dominant mid-gap traps and surface charges. In addition, SS was improved after temperature cycle for both V_{DS}=0.5V and 0.05V and it is due to the reduction of trap states during the long duration of annealing. The I_{MAX}/I_{MIN} ratio decreases exponentially with increasing temperature for both V_{DS}=0.05V and 0.5V. This can be explained by the combined effects of exponential dependence of I_{OFF} with temperature and the weak temperature dependence of I_{DR}. The I_{MAX}/I_{MIN} ratio decreased from ~ 10^5 at 25°C to ~ 10^3 at 150°C. This degradation of device performance was mainly due to the high leakage current at higher temperature (> 100°C). Moreover, the I_{MAX}/I_{MIN} ratio recovered to its initial level when the device was cooled down to 25°C after temperature cycle, which indicates that the high temperature operation was not destructive to the TFET structure up to 150°C.

IV. Conclusion

The high temperature reliability of the structural properties and device performances of the mixed As/Sb staggered gap tunnel FETs were comprehensively studied from 25°C to 150°C. Nearly identical strain relaxation states from each layer of the active region were determined by XRD measurements at each temperature step, indicating no additional strain relaxation was observed up to 150°C. Symmetric two dimensional crosshatch patterns on the surface of the structure both before and after temperature cycle were obtained by AFM

studies. The well maintained crosshatch pattern and similar surface morphology after the temperature cycle suggested the stability of the structural properties of this TFET structure. Besides, no extra inter-diffusion occurred at each heterointerface during the high temperature operation of 150°C as confirmed by SIMS investigation. The fabricated mixed As/Sb staggered gap tunnel FET device showed distinguished features with higher operating temperature. The leakage current of the reverse-biased p^+-i-n^+ diode was increased exponentially with increasing temperature due to Shockley-Read-Hall G-R mechanism. The ON-state drive current of the TFET devices exhibited weak temperature dependence. It was decreased with temperature from 25°C to 100°C due to the variation of Fermi distribution and the increase in channel resistance, but increased from 100°C to 150°C due to the reduction of bandgap energies of the active region materials and the decrease in effective tunneling barrier height. The SS has a strong positive temperature coefficient due to the trap-assistant tunneling process. The I_{MAX}/I_{MIN} ratio was decreased from ~ 10^5 at 25°C to ~ 10^3 at 150°C due to the increase in leakage current at higher temperature. Together, the study of structural and device performances of mixed As/Sb staggered gap tunnel FET structure at high operating temperature will provide a path ways to achieve high performance TFET devices at higher temperature of operation for future low-power logic applications.

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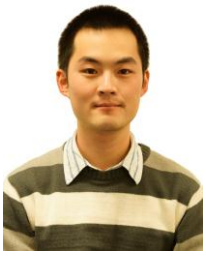

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