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Design, fabrication, and analysis of p-channel arsenide/antimonide hetero-junction tunnel transistors

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In this paper, we demonstrate InAs/GaSb hetero-junction (hetJ) and GaSb homo-junction (homJ) p-channel tunneling field effect transistors (pTFET) employing a low temperature atomic layer deposited high-κ gate dielectric. HetJ pTFET exhibited drive current of 35 μA/μm in comparison to homJ pTFET, which exhibited drive current of 0.3 μA/μm at $V_{DS} = -0.5$ V under DC biasing conditions. Additionally, with pulsing of 1 μs gate voltage, hetJ pTFET exhibited enhanced drive current of 85 μA/μm at $V_{DS} = -0.5$ V, which is the highest reported in the category of III-V pTFET. Detailed device characterization was performed through analysis of the capacitance-voltage characteristics, pulsed current-voltage characteristics, and x-ray diffraction studies. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4862042]

I. INTRODUCTION

The switching slope in a metal oxide semiconductor field effect transistor (MOSFET) is limited to 60 mV/decade at room temperature. As a result, threshold voltage scaling in a MOSFET will lead to an exponential increase in off–state leakage current (I_{OFF}), thus limiting supply voltage scaling.[1,2] Tunneling field effect transistors (TFETs) based on band-to-band generation of carriers can achieve sub-60 mV/decade switching slope at room temperature,[1,2] which would allow reduction of the supply voltage and thus the overall power dissipation in the circuit. However, the on-state current (I_{ON}) of a TFET device needs to be enhanced in order to outperform MOSFET at low supply voltages.[3,4] III-V semiconductor based TFETs have gained wide interest due to the wide range of available compositionally tunable effective barrier heights (Eb_{eff}).[5] Further, direct band-gap of these materials and lower effective mass of tunneling carriers increase the tunneling efficiency, thereby enhancing the device performance. Furthermore, these hetero-structures can be grown on either GaSb or InP substrates metamorphically using solid source molecular beam epitaxy (MBE) with *in-situ* source doping, thus realizing abrupt source-channel junctions, another important factor determining the performance of TFETs.[6] III-V semiconductors based n-channel TFETs (nTFET) have already been demonstrated with sub-60 mV/decade subthreshold slope (SS)[7] and with high I_{ON}.[8,9] However, realization of TFETs in complimentary logic application requires a p-channel TFET (pTFET) with symmetrical performance. There are several challenges that need to be overcome prior to the demonstration of a high performance pTFET within the III-V semiconductor based material system. The first challenge is the integration of a high quality high-k dielectric on the $GaAs_{1-y}Sb_y$ channel (Figure 1). Antimony (Sb) dangling bonds introduce defect states near the valence band edge in GaSb.[10] In fact, it was recently been demonstrated that for HfO_2/GaSb interfaces, gallium (Ga) dangling bonds and Sb–Sb antibonding states are located inside the GaSb conduction band, which is in contrast to the well-studied high-κ/GaAs in which Fermi level pinning is attributed to presence of Ga dangling bonds and As–As dimers.[11,12] Furthermore, higher interfacial oxide content is found to be beneficial in reducing the gap states.[12] A second challenge arises from the density of states (DOS) mismatch between the conduction band and the valence band. In n^+ heavily doped source region of p-channel III-V TFETs, the Fermi level is degenerate and located far away from the conduction band edge, thereby preventing efficient energy filtering of conduction band holes as they tunnel from conduction band states into the valence band states in the channel. This results in a fundamental tradeoff between I_{ON} and the switching slope in p-channel TFETs.[13,14]

In this work, InAs-GaSb hetero-junction (hetJ) pTFET is experimentally demonstrated using a low temperature atomic layer deposited (ALD) high-κ dielectric. For comparison, a GaSb homo-junction (homJ) pTFET is also fabricated in this study. The device design details are discussed in Sec. II. The experimental details are covered in Sec. III. Capacitance–voltage characteristics of metal oxide semiconductor capacitors (MOSCAPs) fabricated on GaSb are systematically analyzed in Sec. IV. In Sec. V, the electrical and material characteristics of the pTFET are discussed. Sec. VI benchmarks the performance of pTFET demonstrated in this work with the reported III-V pTFETs. Sec. VII summarizes the key results from this work.

II. DEVICE DESIGN

Atomistic simulations[15] were performed using the non-equilibrium green function method on ultra-thin body double

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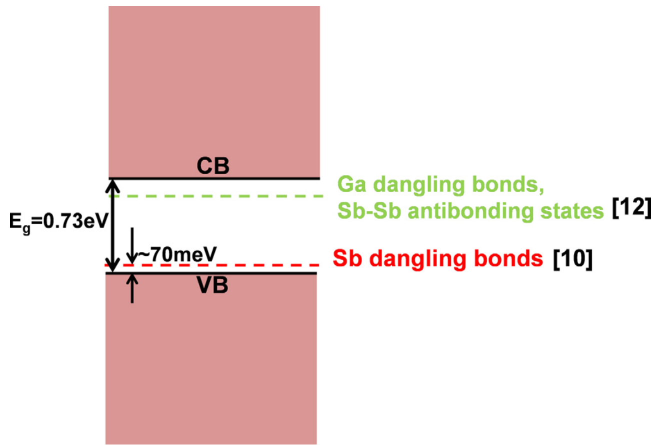

FIG. 1. Schematic illustration of the high-κ/GaSb interface states.

gate TFET structure with body thickness (T_{body}) of 7 nm, equivalent oxide thickness (EOT) of 1 nm, and gate length (L_{gate}) of 32 nm (Figure 2(a)). Figure 2(b) shows the transfer characteristics (I_{DS}–V_{GS}) of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ and InAs/GaSb TFETs for varying values of source doping (N_S). The gate metal work-functions were adjusted so that I_{OFF} is matched to 5 nA/μm in all the simulations. InAs/GaSb TFET exhibits superior characteristics compared to $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ due to smaller Eb_{eff}. InAs/GaSb nTFET with $N_S = 8 \times 10^{19} cm^{-3}$ exhibits high I_{ON} of 320 μA/μm at $V_{GS} = 0.5$ V, $V_{DS} = 0.3$ V and exhibits sub-60 mV/decade SS. InAs/GaSb pTFET, on the other hand, shows degraded SS for higher N_S due to the low DOS of the conduction band in InAs as discussed in Sec. I. Figure 2(c) shows I_{ON} of InAs/GaSb pTFET as a function of N_S for different V_{GS}. At $V_{GS} = 0.5$ and 0.4 V, in order for InAs/GaSb pTFET to deliver half the I_{ON} of InAs/GaSb nTFET, N_S of $5 \times 10^{18} cm^{-3}$ is desired. However, at $V_{GS} = 0.3$ V, higher N_S of $1 \times 10^{19} cm^{-3}$ results in lower I_{ON}. This is due to the degraded SS of the pTFET. Hence, depending on the operating voltage, N_S needs to be optimized, such that the pTFET delivers enough I_{ON} to complement the performance of nTFET. In this work, N_S of $1 \times 10^{19} cm^{-3}$ is adopted for InAs/GaSb hetJ as well as GaSb homJ pTFET.

III. EXPERIMENTAL PROCEDURES

Figs. 3(a) and 3(b) show the schematic layer structures of InAs-GaSb hetJ pTFET and GaSb homJ, respectively, which were grown on GaSb substrates using MBE. AlSb/AlAs super-lattice was used as lattice matched isolation buffer for each structure. The pTFET fabrication starts with sputtering 300 nm of Molybdenum on the MBE grown samples. For the GaSb homJ sample, 60 nm of Titanium was evaporated prior to Molybdenum sputtering in order to facilitate the self-aligned gate deposition as explained later in this section. Titanium/Chromium hard mask was created on top of Molybdenum after patterning using electron beam lithography. Using Titanium/Chromium as etch mask, Molybdenum (Molybdenum+Titanium in case of homJ sample) and the semiconductor region comprising of source, channel, drain were etched to form a vertical pillar-like structure. In the case of hetJ sample, citric acid based solution was used to selectively wet etch InAs with respect to Molybdenum and create undercut required to form a self-aligned gate.[16] Selective wet etching of GaSb with respect to Molybdenum is difficult. Hence, in the case of GaSb homJ sample, Titanium was selectively wet etched using dilute HF acid solution ($HF:H_2O = 1:100$) to create the required undercut. The pTFET samples were then treated in concentrated HCl solution ($HCl:H_2O = 1:1$) for 5 min followed by rinse in isopropyl alcohol (IPA). A bi-layer gate oxide comprising of 1 nm Al_2O_3 and 3.5 nm HfO_2 was immediately deposited using ALD. Gate metal (Palladium) was vertically evaporated after patterning to form a self-aligned gate. Drain contact was then defined, oxide removed using dry-etch and

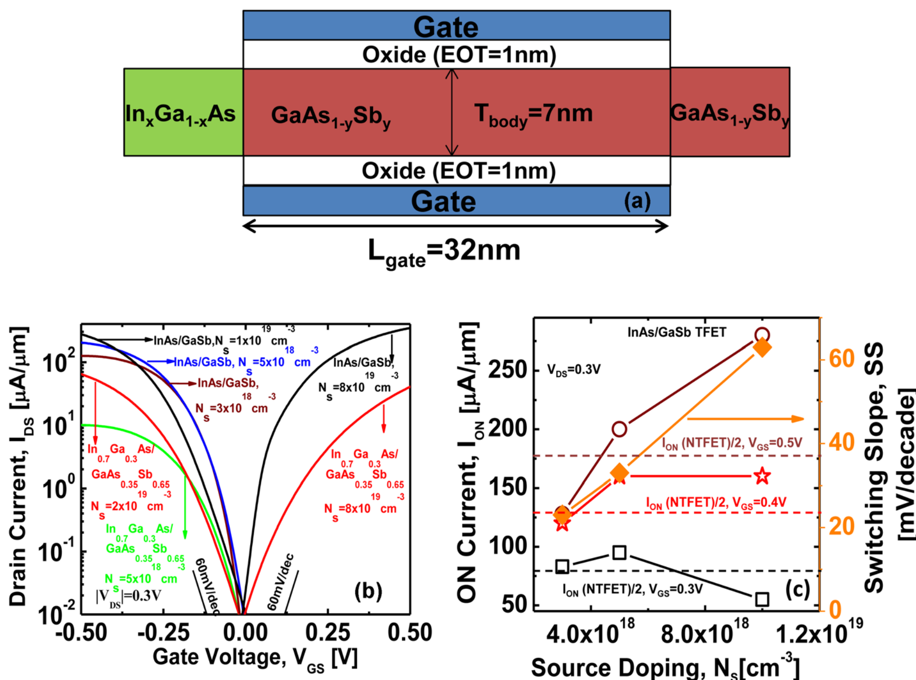

FIG. 2. (a) Schematic of ultra-thin body pTFET simulated. (b) Transfer characteristics of InAs/GaSb and $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ pTFET as a function of the source doping. (c) I_{ON} as a function of N_S in InAs/GaSb pTFET.

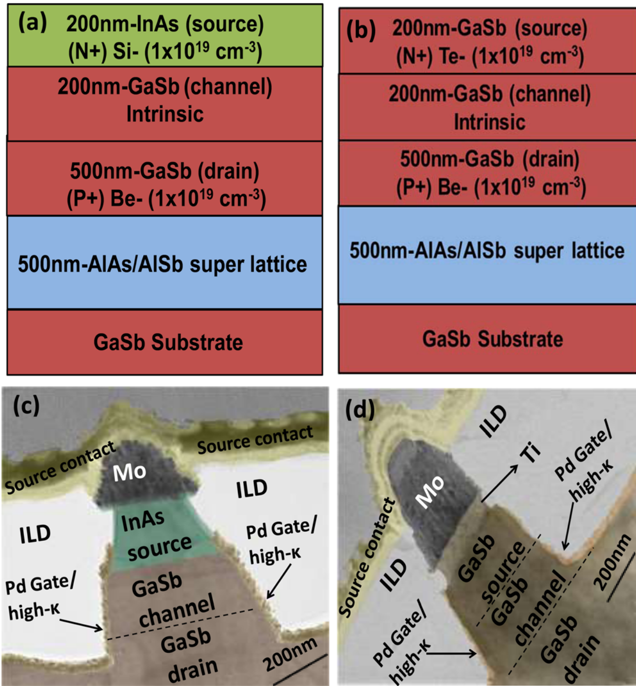

FIG. 3. (a) Schematic of MBE grown InAs-GaSb hetJ layer structure (b) Schematic of MBE grown GaSb homJ layer structure. (c) False colored cross section TEM of the fabricated InAs-GaSb hetJ. (d) False colored cross section TEM of the fabricated GaSb homJ pTFET.

Ti/Pd/Au metal stack evaporated. The samples were then baked in an inter-layer dielectric (ILD) for 60 min and then etched back in Oxygen plasma until the top of Molybdenum was exposed. Source contact was then defined and Titanium/Palladium/Gold metal stack evaporated. Finally, ILD was etched off from the active regions of the device. Figs. 3(c) and 3(d) show the false colored cross-section transmission electron micrograph (TEM) images of the fabricated hetJ and homJ pTFETs. For MOSCAP fabrication, samples were degreased in acetone and methanol for 5 min each and rinsed in IPA, followed by a dip in concentrated HCl solution ($HCl:H_2O = 1:1$) for 5 min and an IPA rinse. The samples were immediately loaded into the ALD chamber and gate oxide comprising of 1 nm of Al_2O_3 and 3.5 nm HfO_2 was deposited. Following patterning the gate pad using electron-beam lithography, Palladium/Gold metal stack was evaporated to form gate contact on the MOSCAP samples. The current voltage characteristics of the pTFETs were measured using an HP parameter analyzer. Capacitance–voltage (C–V) and conductance–voltage (G–V) measurements were obtained using a HP 4285 A precision *LCR* meter type. Keithley 4200 Semiconductor Characterization System with a dual channel 4225 Pulse Measure Unit (PMU) was used for pulsed-I_{DS}–V_{GS} measurements. X-ray reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu Kα-1 as an x-ray source. Both the symmetric (004) and asymmetric (115) RSMs were recorded from the hetJ pTFET structure.

IV. OPTIMISATION AND CHARACTERISATION OF HIGH-κ/GaSb INTERFACE

A low temperature ALD has been shown to improve the high-κ/$GaAs_{0.35}Sb_{0.65}$ interface resulting in improved Fermi level movement efficiency.[17] The improvement in the high-κ/ $GaAs_{0.35}Sb_{0.65}$ stems from the presence of Sb-oxide at low ALD temperature (110 °C).[17] We have adopted a similar approach in the optimization of the high-κ/GaSb interface. Figure 4(a) shows the C–V characteristics of ALD deposited on undoped GaSb at deposition temperatures (T_{dep}) of 110 °C, 150 °C, and 200 °C, measured at T = 300 K. As T_{dep} is reduced, C–V characteristics show improved modulation. Hence, ALD deposition temperature of 110 °C was used for pTFET fabrication. The high frequency capacitance density in accumulation is close to 1.1 μF/cm^2 which corresponds to an EOT of 3.4 nm. Figure 4(b) shows the C–V characteristics of ALD deposited at 110 °C measured at T = 300 K and 150 K. At T = 150 K, reduced frequency dispersion and enhanced modulation is seen in the C–V characteristics attributed to suppression of trap response at lower temperature. The equivalent-circuit modeling technique was used to model the measured C–V and G–V characteristics and extract D_{it} and trap response time. In this approach, C–V and G–V characteristics are simulated as a function of frequency for various interface state density (D_{it}) and trap response time values until the error between measured and modeled values are minimized.[18,19] This method is advantageous when the traps extend into the oxide and, thus, mask the conductance peaks. Traps extending 1 nm into the oxide were taken into consideration for modeling.[19] The distribution of traps as a function of distance 'x' away from the high-κ/GaSb interface is given by

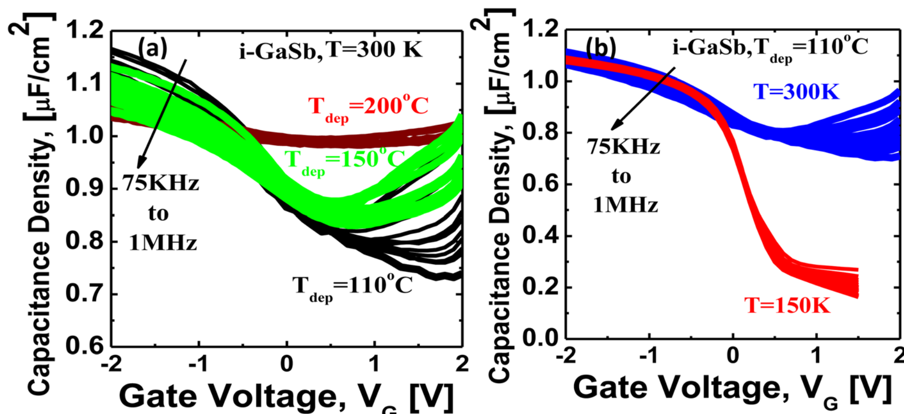

FIG. 4. (a) C–V characteristics of Al_2O_3/HfO_2 deposited on p-type GaSb in the frequency range of 75 KHz to 1 MHz measured at 300 K as a function of deposition temperature. (b) C–V characteristics of Al_2O_3/HfO_2 deposited 110 °C and measured at T = 300 K and T = 150 K.

$$N_{it} = N_{it}(0)\exp\left(\frac{-x}{x_{DIGS}}\right),$$

where $N_{it}(0)$ is the trap density at high-κ/GaSb interface, x_{DIGS} is the characteristic decay length which is used as a fitting parameter ($x_{DIGS} = 1$Å) in the equivalent circuit model. The response time of the traps in the oxide increases exponentially as follows:

$$\tau = \tau_0(E_t)\exp(2kx),$$

where $\tau_0(E_t)$ is the trap response time at $x = 0$ and at a given energy level E_t, and k is the wave vector for holes tunneling from the valence band in GaSb to the traps given by

$$k = \sqrt{2m^* \Delta E_V/\hbar^2},$$

where m* is the hole effective mass, and ΔE_V is the valence band offset between high-κ and GaSb.

Using $\Delta E_V = 3.4$ eV (Ref. 20) and $m^* = 0.044$ eV (Ref. 21), k is calculated to be 0.2/Å. Figures 5(a) and 5(b) show the measured and modeled C–V, G–V characteristics which are in good agreement with each other. Figure 5(c) shows the extracted D_{it} as a function of gate voltage and integrated over various depths into the oxide. As more traps extending into the oxide are taken into account, the net integrated D_{it} measured increases. Traps beyond $x = 0.4$ nm do not contribute to the net integrated trap density since $x_{DIGS} = 1$Å and due to exponential decaying nature of the interface traps with increasing distance into the oxide, as discussed above. Figure 5(d) shows the extracted trap response time as a function of gate voltage for various trap depths into the oxide. The response time for traps increase exponentially as the distance from the interface increases. However, it should be noted that the factor *k* is assumed to be independent of gate voltage. This might introduce some error in the calculation of trap time constants as a function of trap position in the oxide. Nevertheless, within the limits of the model used, the trap response time expected for this high-κ gate stack on GaSb should be faster than 1μs, since traps beyond $x = 0.4$ nm do not contribute to the overall D_{it}. Figure 5(e) shows D_{it} as a function of energy location in the bandgap (Eg) of GaSb for T_{dep} of 110 °C and 200 °C. With $T_{dep} = 200$ °C, the Fermi level is pinned near the valence band edge possibly due to thermal decomposition of Sb-oxide leading to formation of Sb dangling bonds which

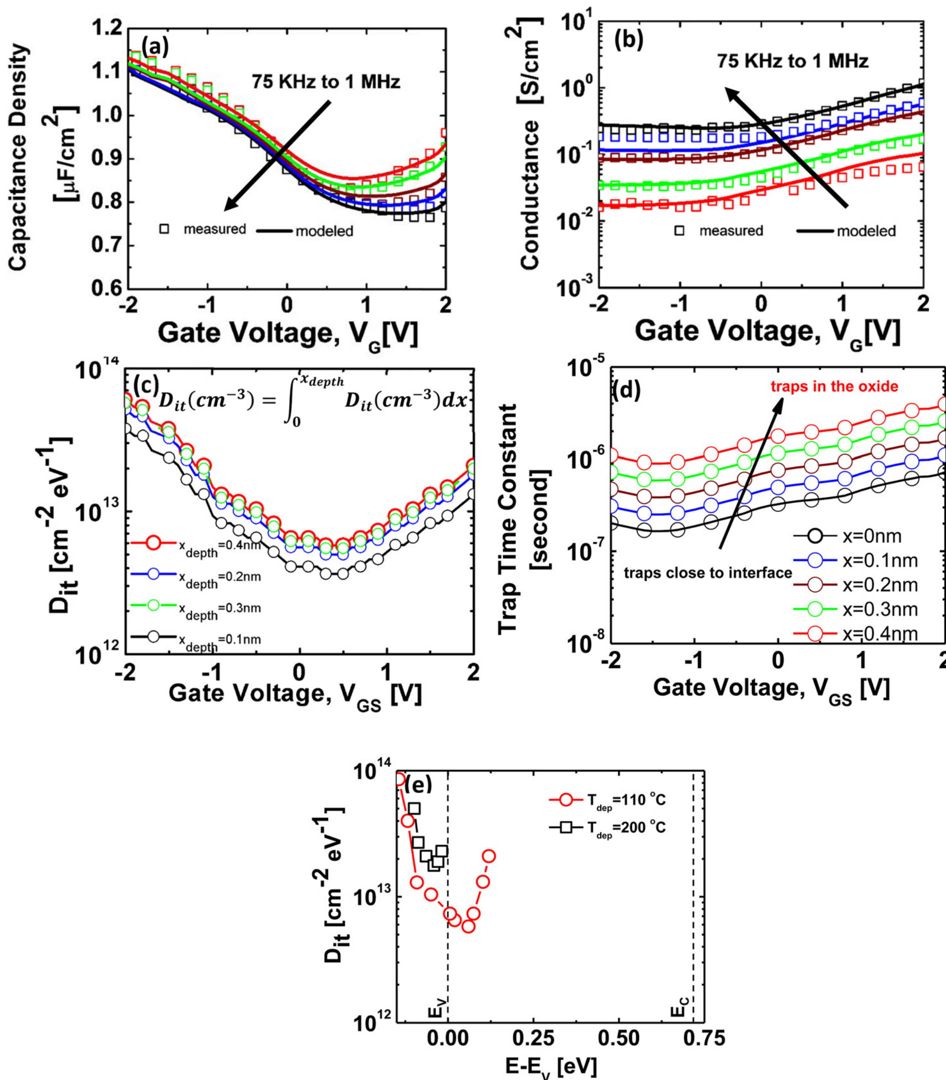

FIG. 5. (a) Measured and modeled CV characteristics at $T = 300$ K as a function of frequency. (b) Measured and modeled GV characteristics at $T = 300$ K as a function of frequency. (c) Extracted D_{it} as a function of gate voltage taking into account traps distributed into the oxide. (d) Extracted trap response time as a function of gate voltage taking into account traps distributed into the oxide. (e) D_{it} as a function of energy location in the bandgap for $T_{dep} = 110$ °C and 200 °C.

introduces high D_{it} near valence band (Figure 2). With $T_{dep} = 110\,°C$, lower density of Sb dangling bonds could be expected due to the presence of Sb-oxide,[17] and thus, the Fermi level movement improves to roughly 0.125 eV away from the valence band edge.

V. ELECTRICAL AND MATERIAL CHARACTERISATION OF pTFET

Figures 6(a) and 6(b) show the I_{DS}–V_{GS} characteristics of InAs/GaSb hetJ and GaSb homJ pTFETs, respectively, at T = 300 K, 150 K and for $V_{DS} = -0.05$ V and -0.5 V. HetJ pTFET exhibits I_{ON} of 35 μA/μm at $V_{DS} = 0.5$ V at T = 300 K. GaSb homJ pTFET in comparison exhibits I_{ON} of 0.3 μA/μm at $V_{DS} = 0.5$ V and T = 300 K. The difference in I_{ON} is attributed to change in Eb_{eff} from 0.73 eV in GaSb homJ to -0.15 eV in hetJ pTFET.[22] Reduction in I_{ON} at T = 150 K is attributed to increase in band-gap with decreasing temperature and thereby, increasing the barrier for tunneling from the conduction band in the source to valence band in the channel. I_{OFF} in hetJ pTFET is 1 μA/μm, which is much higher than $I_{OFF} = 3$ nA/μm in GaSb homJ pTFET. High I_{OFF} in hetero-junction material system compared to a homo-junction material system has been reported in nTFETs and attributed to defects at the hetero-interface.[9] It is possible that the hetJ pTFET suffers from high defect density at the hetero-interface leading to high I_{OFF}. I_{OFF} in hetJ pTFET was found to scale with the device cross-section area (product of width and body thickness), which confirms that I_{OFF} is caused by bulk conduction (not shown). At T = 150 K, I_{OFF} reduces substantially and I_{ON}/I_{OFF} improves to $\sim 10^4$ in both hetJ, as well as homJ pTFET. The reduction in I_{OFF} could be attributed to: (1) Reduction in the Shockley–Read–Hall generation-recombination current, which is a strong function of temperature[23] and (2) suppression of D_{it} response, which improves the Fermi-level movement efficiency (Figure 3(b)). Figure 6(c) shows the SS as a function of drain current for both homj and hetJ pTFETs. HetJ pTFET not only exhibits lower SS but the minimum SS is observed at higher drain current. Further, hetJ pTFET shows lower drain induced barrier thinning (DIBT) in comparison to homj pTFET measured at $I_{DS} = 1$ nA/μm and T = 150 K (Figure 6(d)). Lower SS and DIBT in hetJ pTFET stems from the reduced E_{beff} compared to homJ pTFET which results in interband-generation occurring closer to the source/channel interface and resulting in improved electrostatics.[24] Figure 7(a) shows the I_{DS}–V_{GS} characteristics of hetJ pTFET at $V_{DS} = 0.5$ V for varying gate voltage pulse widths. With a gate voltage pulse width of 1 μs, I_{ON} increases to 85 μA/μm which corresponds to more than 2× improvement over I_{ON} measured under DC bias conditions. Interestingly, with a gate voltage pulse width of 10 μs, I_{ON} increases to 70 μA/μm which is roughly 2× of the I_{ON} under DC bias conditions. Figure 7(b) shows the SS of hetJ pTFET as function of drain current for varying gate pulse widths. With 1 μs gate pulsing, a minimum SS of 500 mV/decade is achieved compared to ~1000 mV/decade under DC biasing conditions. Further, with 10 μs gate pulsing, a minimum SS of ~600 mV/decade is achieved. As discussed in Sec. III, the trap response time for high-κ on GaSb was calculated to be faster than 1 μs. However, since the model used for C–V and G–V modeling has certain limitations discussed in Sec. III, for additional confirmation, 10 μs gate pulsing was carried out and I_{DS}–V_{GS} characteristic measured in homJ pTFET. HomJ pTFETs exhibit negligible change in I_{ON} as well as SS (Figures 7(c) and 7(d)). To further understand the anomalous

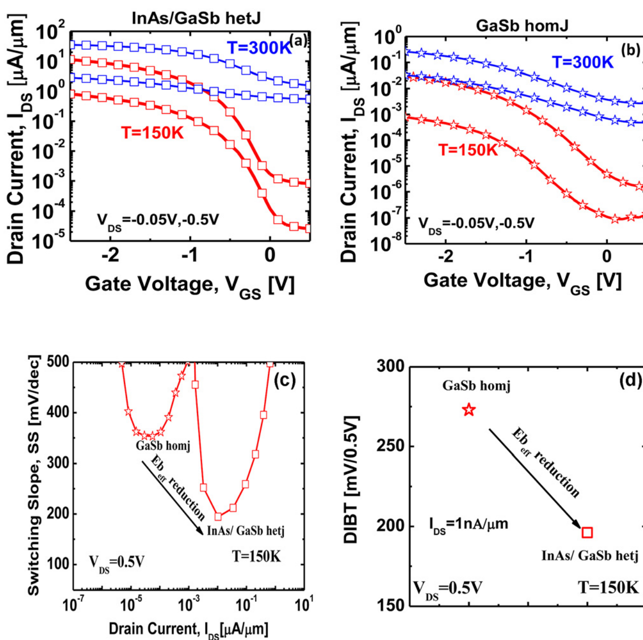

FIG. 6. (a) and (b) I_{DS}–V_{GS} characteristics of hetJ and homJ pTFETs at T = 300 K and 150 K. (c) SS as a function of drain current at T = 150 K showing lower SS in hetJ compared to homJ pTFET. (d) hetJ pTFET exhibits lower DIBT compared to homJ pTFET at $I_{DS} = 1$ nA/μm, T = 150 K.

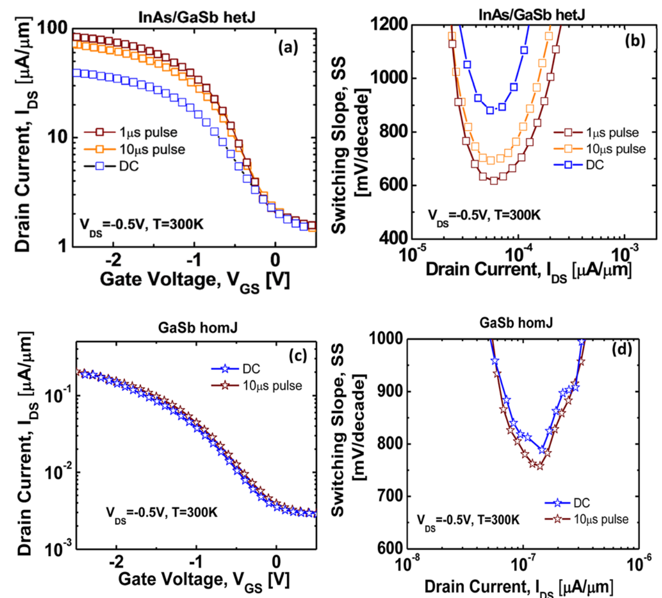

FIG. 7. (a) I_{DS}–V_{GS} characteristics of hetJ for varying gate voltage pulse widths. (b) SS of hetJ pTFET as a function of drain current for varying gate voltage pulse widths. (c) I_{DS}–V_{GS} characteristics of homJ pTFET show negligible change in I_{ON} with 10 μs gate voltage pulsing compared to DC bias conditions. (d) SS of homJ pTFET shows negligible change in I_{ON} with 10 μs gate voltage pulsing compared to DC bias conditions.

response to gate voltage pulsing in InAs/GaSb pTFETs, detailed material characterization was performed.

The relaxation state and residual strain of epilayers within the InAs/GaSb hetJ pTFET structure were obtained from RSMs. Figures 8(a) and 8(b) show the symmetric (004) and asymmetric (115) RSMs from this structure. All layers with measured compositions were labeled to the corresponding reciprocal lattice points (RLPs). As shown in Figures 8(a) and 8(b), four distinct RLP maxima were found in RSMs of this structure, corresponding to (1) GaSb substrate as well as the GaSb channel/drain layers, (2) InAs source layer, (3) the satellite peaks from AlAs/AlSb super lattice, and (4) an extra $GaAs_{1-y}Sb_y$ layer which is not expected from this structure. The composition of As in this layer was determined to be ∼2.2%. As an additional confirmation, cross-section TEM of the pTFET structure was taken as shown in Figure 8(c). The presence of an amorphous layer at the hetero-junction was found, which corresponds to the $GaAs_{0.022}Sb_{0.978}$ layer detected in the XRD experiment. The $GaAs_{0.022}Sb_{0.978}$ layer may be introduced during the switching from GaSb channel layer to InAs source. A proper switching sequence of III/V elements is critical for engineering an abrupt hetero-interface during the growth of mixed As/Sb materials,[25–27] otherwise the intermixing between As and Sb atoms will result in uncontrolled layer composition at the hetero-interface, which will cause the change of strain relaxation properties of the epilayer grown on this interface.[28] The change of strain relaxation properties may introduce high density dislocations at the hetero-interface and within the InAs source layer, which explains the high I_{OFF} in the fabricated hetJ pTFET. Besides, the formation of $GaAs_{0.022}Sb_{0.978}$ layer at the hetero-interface will change the band alignment of source/channel, which leads to the increase of tunneling distance and degrade the device performance. Furthermore, the $GaAs_{0.022}Sb_{0.978}$ interfacial layer between InAs source and GaSb channel may also introduce unexpected interface states with the high-κ due to the change of strain relaxation properties, and these trap states could lead to different D_{it} response for the device and might explain the anomalous pulsed I_{DS}–V_{GS} response in hetJ pTFETs.

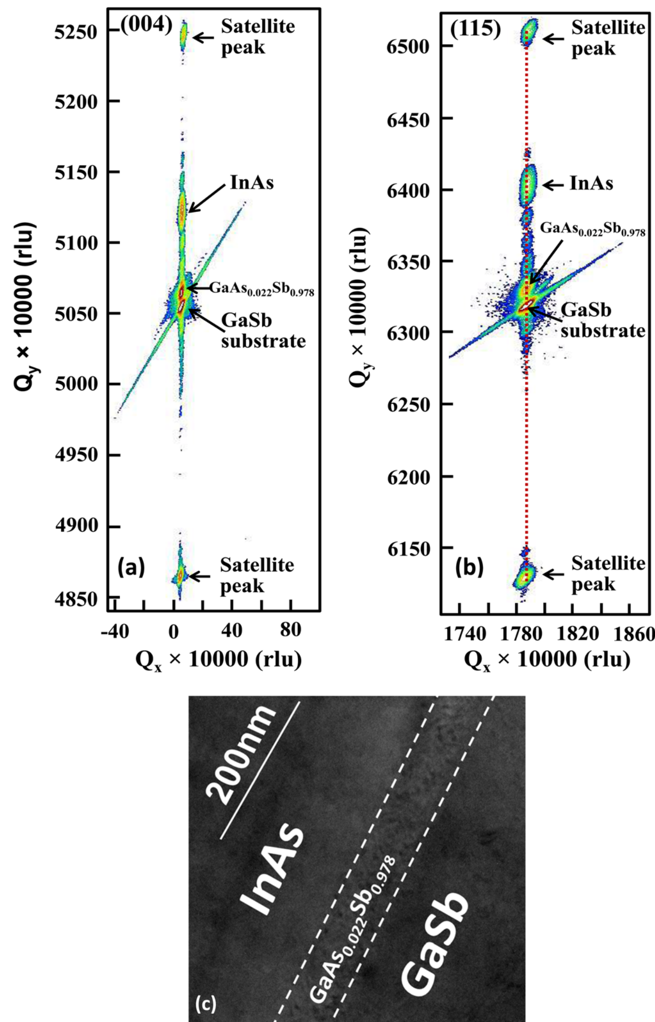

FIG. 8. (a) and (b) Symmetric and asymmetric RSM of InAs/GaSb structure showing the presence of $GaAs_{0.022}Sb_{0.978}$ at the hetero-junction. (c) Cross-section TEM of the InAs/GaSb structure confirming the presence of an amorphous layer of $GaAs_{0.022}Sb_{0.978}$ at the hetero-junction.

TABLE I. Benchmarking of I_{ON} against experimentally demonstrated pTFET till date.

Material	EOT (nm)	Eb_{eff} (eV)	V_{DS} (V)	I_{ON} (μA/μm)	Reference
InAs-Si	3.65	-	−0.5	0.1	Ref. 29
$In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$	3.4	0.25	−0.5	5	Ref. 17
GaSb	3.4	0.73	−0.5	0.3	This work
InAs/GaSb	3.4	−0.15	−0.5	85	This work

VI. BENCHMARKING

Table I shows the performance comparison of the reported pTFETs within the III-V material system. The gate voltage is chosen sufficiently high enough to account for the stretch out in the I_{DS}–V_{GS} characteristics due to the presence of D_{it}. InAs/GaSb hetJ pTFET exhibits drive current of 85 μA/μm which is the highest reported in the category of III-V pTFET. With the scaling of EOT and the reduction in D_{it}, the device characteristics are expected to improve further.

VII. CONCLUSIONS

InAs/GaSb hetero-junction and GaSb homo-junction pTFET were grown and fabricated using a low temperature ALD high-κ gate dielectric. The hetJ pTFET exhibits I_{ON} of 35μA/μm at $V_{DS} = 0.5$ V under DC biasing conditions. Through modeling of C–V and G–V characteristics of MOSCAPs fabricated on GaSb substrate, D_{it} and trap response time were calculated as a functions of the extent of traps into the oxide. With 1 μs gate voltage pulsing, I_{ON} increased to 85 μA/μm at $V_{DS} = 0.5$ V in hetJ pTFET. Further, even with 10 μs gate voltage pulsing, I_{ON} as well as SS improved significantly compared to the DC bias conditions. RSM study on the InAs/GaSb hetero-junction layer revealed the presence of $GaAs_{0.022}Sb_{0.978}$ layer at the hetero-interface which could explain the presence of slow

interface traps in the hetJ pTFET. Improvement in the device performance can be achieved through: (a) Optimized MBE growth conditions to reduce the defects at the hetero-junction combined with reduction in body thickness which would translate to low I_{OFF}, (b) low values of D_{it} to improve Fermi level movement efficiency and improve SS, and (c) scaled EOT to improve I_{ON} as well as SS. In addition, density of state engineering would also be required in InAs/GaSb pTFET in order to realize TFET based complimentary logic.

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