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Tensile-Strained Nanoscale Ge/$In_{0.16}Ga_{0.84}As$ Heterostructure for Tunnel Field-Effect Transistor

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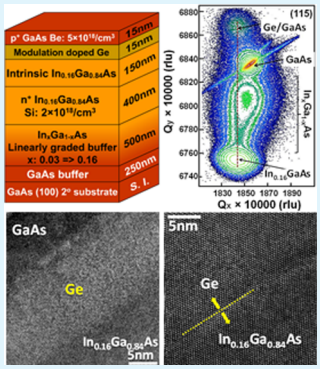
Supporting Information

ABSTRACT: Tensile strained Ge/$In_{0.16}Ga_{0.84}As$ heterostructure was grown in situ by molecular beam epitaxy using two separated growth chambers for Ge and III−V materials. Controlled growth conditions led to the presence of 0.75% in-plane tensile strain within Ge layer. High-resolution transmission electron microscopy confirmed pseudomorphic Ge with high crystalline quality and a sharp Ge/$In_{0.16}Ga_{0.84}As$ heterointerface. Atomic force microscopy revealed a uniform two-dimensional cross-hatch surface morphology with a root-mean-square roughness of 1.26 nm. X-ray photoelectron spectroscopy demonstrated reduced tunneling-barrier-height compared with Ge/GaAs heterostructure. The superior structural properties suggest tensile strained Ge/$In_{0.16}Ga_{0.84}As$ heterostructure would be a promising candidate for high-performance and energy-efficient tunnel field-effect transistor applications.



KEYWORDS: *tensile strain, Ge/$In_{0.16}Ga_{0.84}As$ heterostructure, high crystalline quality, sharp heterointerface, tunnel field-effect transistor, molecular beam epitaxy*

The tunnel field-effect transistor (TFET) is a promising device candidate to replace the conventional metal-oxide-semiconductor field-effect-transistor (MOSFET) for low power logic applications.[1−3] By exploiting the gate modulated band-to-band tunneling (BTBT) phenomenon, the subthreshold slope (SS) of TFETs is not restricted to the lower limit of 60 mV/dec as MOSFETs at 300 K.[2−8] The steeper SS of TFETs guarantees higher ON-state to OFF-state current ratio (I_{ON}/I_{OFF} ratio), which allows significant reduction of the supply voltage and power consumption in a transistor.[2,3,6] To achieve high BTBT tunneling probability and high I_{ON}, small band gap materials such as germanium (Ge) and III−V materials should be employed.[3,4,7−15] In past few decades, Ge has been actively investigated because of its high intrinsic carrier mobility, small band gap energy, and silicon (Si) compatible process flow.[15−17] In addition, tensile strained Ge exhibited further reduction in band gap energy and enhanced electron and hole mobility,[16−18] making it a highly promising material for low power TFET applications. For further improvement, the band alignment engineering is essential to improve the I_{ON} and reduce the SS of TFET devices. Heterojunction TFET structure as a replacement for homojunction has been used to efficiently reduce the effective tunneling barrier height (E_{beff}) between the source and the channel[2,4,6−11] that resulted in additional enhancement of TFET device performances. In this aspect, the Ge/InGaAs heterostructure satisfies the requirements for low band gap material system in a TFET design. More importantly, by carefully controlling the alloy composition in InGaAs material, the magnitude of tensile strain inside the Ge layer can be tailored, such that the E_{beff} between the Ge source and the InGaAs channel can also be well-modulated, both of which will facilitate the further optimization of TFET structure. Simulations predicted[19] and experiments demonstrated[13] that wide range of In composition from 0% to 53% can be used in Ge/InGaAs heterostructures for TFET applications, providing various selection of tensile strain values inside of Ge and different band alignments at the Ge/InGaAs heterointerface. To reduce the tunneling distance and increase the tunneling current, a high quality Ge/InGaAs heterostructure with a sharp heterointerface between the tensile strained Ge source and the InGaAs channel is indispensable.[11,13,20] As a result, there is a great demand for the growth of high quality tensile strained Ge/InGaAs heterostructures to fully explore the benefits of low power TFET applications. Control of the tensile strain magnitude in the heterostructure provides an additional parameter toward tuning the transistor behavior.

To date, all reported Ge/InGaAs heterostructures have been grown by metal−organic chemical vapor deposition (MOCVD).[13,16] However, solid-source molecular beam epitaxy (MBE) is now receiving interest for TFET applications because of its extreme precision and growth uniformity, since it provides an opportunity to investigate and potentially optimize in situ grown tensile strained Ge on InGaAs within a very different growth regime compared to MOCVD. Using MBE, we have recently reported superior quality of GaAs/Ge/GaAs and Ge/

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GaAs heterostructures.[17,18] This paper reports the first comprehensive study of in situ grown tensile strained Ge/InGaAs heterostructures by MBE. Detailed structural analysis provided here will facilitate the application of this heterostructure for TFET design and optimization of device performance.

In this study, high quality tensile strained Ge/$In_{0.16}Ga_{0.84}As$ heterostructure was grown by solid source MBE using two separated growth chambers for Ge and III−V materials. These two growth chambers were connected via ultrahigh vacuum transfer chamber. The separation of Ge growth chamber from III−V growth chamber reduces the diffusion of arsenic (As) atoms into Ge, decreasing excess As point defects inside the Ge layer,[17,18] and preserving the sharp heterointerface between Ge and InGaAs. The reduction of As point defect will reduce the trap-assisted tunneling access and the abrupt Ge/InGaAs heterointerface will shorten the tunneling distance of carriers from Ge source to InGaAs channel, both of which are critical for reducing the SS and improving I_{ON} of TFETs. By utilizing the in situ MBE growth process and carefully optimizing the growth parameters, the presence of 0.75% in-plane tensile strain was identified by X-ray diffraction (XRD) within the 15 nm Ge layer deposited on $In_{0.16}Ga_{0.84}As$. The tensile strained nature of Ge layer and a sharp Ge/$In_{0.16}Ga_{0.84}As$ heterointerface was confirmed by high-resolution transmission electron microscopy (TEM) analysis. TEM specimens were prepared using standard grinding and ion-milling method. FEI Titan 300 microscope was used for conducting TEM studies. The demonstration of high quality tensile strained Ge/$In_{0.16}Ga_{0.84}As$ heterostructure by MBE will offer new opportunities to utilize this structure for high performance and low standby power TFET applications.

The Ge/$In_{0.16}Ga_{0.84}As$ TFET heterostructure was grown on offcut (100) epi-ready semi-insulating GaAs substrate (2° offcut toward ⟨110⟩ direction). Substrate oxide desorption was done at ∼680 °C under arsenic overpressure of $\sim 1 \times 10^{-5}$ Torr in the III−V growth chamber. In situ reflection high energy electron diffraction (RHEED) was used to monitor the oxide desorption process, as well as the surface reconstruction of each epilayer. An initial 250 nm undoped GaAs buffer layer was deposited at 650 °C under a stabilized As_2 flux with a V/III ratio of 25. To accommodate the lattice mismatch between $In_{0.16}Ga_{0.84}As$ active layer and the GaAs substrate, 500 nm linearly graded $In_xGa_{1-x}As$ buffer was grown with indium (In) composition increasing from 3% to 16%. Then, the 400 nm Si-doped n^+ $In_{0.16}Ga_{0.84}As$ drain layer with doping concentration of $2 \times 10^{18}/cm^3$ was deposited followed by 150 nm intrinsic $In_{0.16}Ga_{0.84}As$ channel layer. The $In_xGa_{1-x}As$ linearly graded buffer and the $In_{0.16}Ga_{0.84}As$ channel/drain layers were grown at a substrate temperature of 560 °C. After that, the wafer was slowly cooled down below 150 °C with arsenic overpressure and transferred to the Ge growth chamber through high vacuum transfer chamber. A 15 nm tensile strained Ge layer was grown on top of intrinsic $In_{0.16}Ga_{0.84}As$ channel at 400 °C using a low growth rate of 20 nm/h. To protect the surface of tensile strained Ge layer, as well as to form the p-type source contact, the wafer was transferred once again to III−V growth chamber under high vacuum and a 15 nm p^+ GaAs was deposited with beryllium (Be) doping concentration of $5 \times 10^{18}/cm^3$. The growth temperature of the top p^+ GaAs cap layer was 350 °C for the first 3 nm utilizing migration-enhanced-epitaxy (MEE) growth technique followed by 12 nm p^+ GaAs with growth temperature of 500 °C. The low temperature MEE growth is confirmed to efficiently reduce the interdiffusion between the Ge and the GaAs, as well as to suppress the antiphase-domain as evident in earlier studies.[17,18] All temperatures referred in this paper represent the thermocouple temperature and the V/III ratio represents the V/III beam-equivalent-pressure ratio. It should be noted that the further improvement of TFET performance can be expected by in situ doped p-type Ge source layer. However, in this study, by utilizing the modulation doping effect from p^+ GaAs top layer to Ge, high hole sheet concentration of $\sim 1 \times 10^{13}/cm^2$ was confirmed in the Ge layer by Hall effect measurement using Van der Pauw technique. The schematic of layer structure for this work is shown in Figure 1, where the source, channel, and drain regions were labeled in the figure. The strain relaxation properties of this Ge/$In_{0.16}Ga_{0.84}As$ TFET structure were investigated by high-resolution XRD. Both rocking curve (RC, $\omega/2\theta$ scan) and reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu Kα-1 line-focused X-ray source. To minimize the measurement error caused by the XRD system, before each XRD measurement, a 2θ scan was performed to align the detector to its zero position (the direct beam position). Then, ω and z scans were repeated to align the sample stage to compensate all offset values caused by instrumental misalignment. The zero ω position was determined by moving the goniometer to the center of gravity of the peak. The height of the stage with mounted sample (z position) was adjusted until the intensity of the X-ray beam is 1/2 the direct beam intensity, within ±3%. The spectral purity of the Cu X-ray tube is <1%. The system was calibrated by Si (100) substrate with (004) $\omega-2\theta$ scan using triple-axis detector. The Si (004) ω peak position was determined to be 34.56° and full with at half-maximum value of 22.5 arcsec. The defect properties, crystallinity, and interface quality of this structure were characterized by cross-sectional TEM. TEM samples were prepared by conventional mechanical thinning procedure followed by Ar^+ ion milling. The contact mode atomic force microscopy (AFM) was used to analyze the surface morphology of this structure. The band alignment of Ge/$In_{0.16}Ga_{0.84}As$ heterostructure was investigated by X-ray photoelectron spectroscopy (XPS) on a PHI Quantera SXM system using a monochromatic Al Kα (1486.7 eV) X-ray source. All XPS measurements were performed using pass energy of 26 eV and an exit angle of 45°. Curve fitting was performed by CasaXPS 2.3.14 using a Lorentzian convolution with a Shirley-type background.

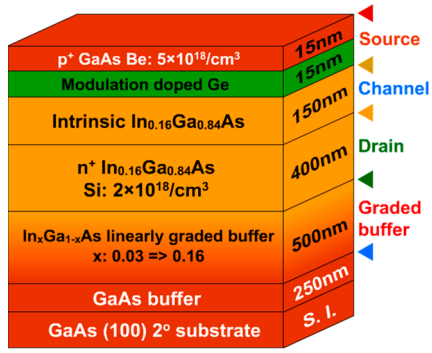

Figure 1. Schematic layer diagram of the strained Ge/$In_{0.16}Ga_{0.84}As$ tunnel FET structure. The source, channel, and drain regions are labeled in this figure.

The surface reconstruction of strained Ge was investigated by RHEED. Figure 2 shows the RHEED pattern of the Ge surface

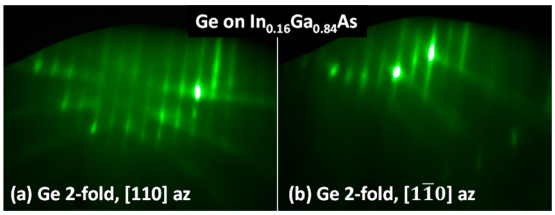

Figure 2. RHEED patterns from the surface of 15 nm Ge on $In_{0.16}Ga_{0.84}As$ along (a) [110] and [1$\bar{1}$0] azimuth. The RHEED patterns exhibited a (2 × 2) Ge surface reconstruction. The sharp and streak RHEED patterns indicate a high-quality Ge layer with smooth surface morphology.

for the in-plane [110] and [1$\bar{1}$0] azimuths. The sharp and streaky (2 × 2) RHEED patterns indicate a high-quality Ge layer with smooth surface morphology. The RHEED patterns exhibited a (2 × 2) Ge surface reconstruction, which was also observed in our early studies from in situ growth of Ge on (100) GaAs.[17,18] The symmetric (004) rocking curve, symmetric (004) and asymmetric (115) RSMs from this structure are shown in Figure 3a, b, and c, respectively, with each layer labeled to its corresponding peak or reciprocal lattice point (RLP). As can be seen from Figure 3a, different from the XRD spectra of Ge grown on GaAs (shown in Supporting Information Figure S1 and references 17 and 18), the Ge peak

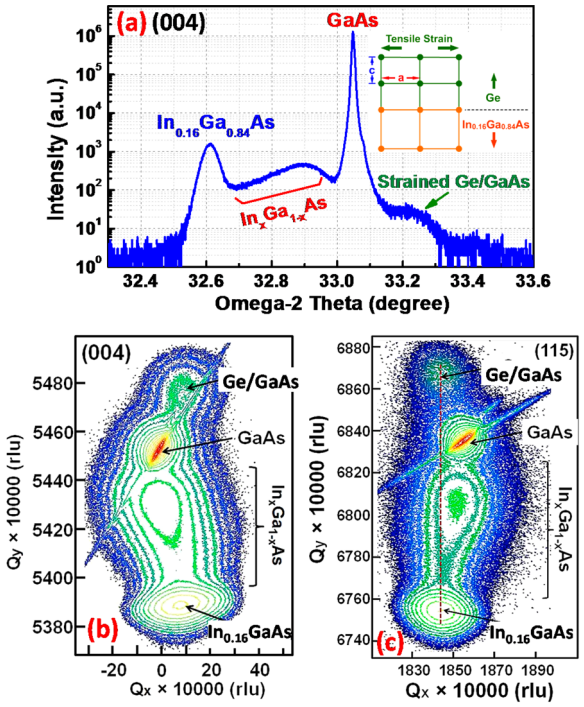

Figure 3. (a) Symmetric (004) rocking curve ($\omega/2\theta$ scan) of the Ge/$In_{0.16}Ga_{0.84}As$ structure. The Ge peak shows a larger Bragg angle than GaAs substrate, indicating a smaller out-of-plane lattice constant, suggesting the presence of in-plane tensile strain in the Ge layer. The insect shows the schematic of tensile strained Ge lattice on $In_{0.16}Ga_{0.84}As$. (b) Symmetric (004) and asymmetric (115) reciprocal space maps of the TFET structure. The in-plane tensile strain value inside of Ge layer is determined to be 0.75% and the relaxation state of Ge with respect to $In_{0.16}Ga_{0.84}As$ is limited to be ~9%.

in this study shows a larger Bragg angle than the GaAs substrate peak, relating to a smaller out-of-plane lattice constant, indicating the presence of in-plane tensile strain in the Ge layer. As shown in the inset of Figure 3a, because of the larger lattice constant of $In_{0.16}Ga_{0.84}As$ layer, the in-plane lattice constant of Ge layer grown on $In_{0.16}Ga_{0.84}As$ was stretched to match the in-plane lattice constant of $In_{0.16}Ga_{0.84}As$, resulting in a tensile strained Ge layer with expanded in-plane lattice constant (labeled as a) and reduced out-of-plane lattice constant (labeled as c). The detailed analysis of the tensile strain values and relaxation state of Ge was conducted by accounting for the symmetric (004) and asymmetric (115) RSMs as shown in Figure 3b and c, respectively. From these RSMs, the in-plane lattice constant (a) and out-of-plane lattice constant (c) of Ge and $In_{0.16}Ga_{0.84}As$ were extracted. The relaxed lattice constants (a_r) of each layer were calculated using a and c together with the Poisson's ratio of each material.[10,20] Table 1 summarizes the values of extracted in-plane, out-of-

Table 1. Summary of Out-of-Plane, In-Plane, and Relaxed Lattice Constants of $In_{0.16}Ga_{0.84}As$ and Ge Layers[a]

	lattice constants (Å)		
material	out-of-plane (c)	in-plane (a)	relaxed (a_r)
$In_{0.16}Ga_{0.84}As$	5.7201	5.7123	5.7164
Ge	5.6275	5.7121	5.6698

[a]The in-plane tensile strain of Ge is $\varepsilon = (a - a_r)/a_r = 0.75\%$.

plane, and relaxed lattice constant of $In_{0.16}Ga_{0.84}As$ and Ge layers. Using the relaxed lattice constant of InGaAs and Vegard's law, the In composition in InGaAs channel/drain layers was determined to be 15.7%, which is consistent with the designed value. Besides, the $In_{0.16}Ga_{0.84}As$ layer was ~90% relaxed with respect to the GaAs substrate, indicating that the $In_xGa_{1-x}As$ linearly graded buffer efficiently accommodates the lattice mismatch induced strain between the $In_{0.16}Ga_{0.84}As$ channel/drain layers and the GaAs substrate. Detailed strain relaxation calculations using the lattice constants as summarized in Table 1 show the residual strain inside of $In_{0.16}Ga_{0.84}As$ layer is <0.1%. The detailed strain relaxation analysis methods can be found in ref 10. and 20. In addition, in-plane tensile strain of 0.75% was determined within the Ge layer. The relaxation state of Ge with respect to $In_{0.16}Ga_{0.84}As$ is only limited to be ~9%, suggesting the pseudomorphic nature of the Ge layer. Furthermore, it can also be found from the asymmetric (115) RSM as shown in Figure 3c that the Ge RLP is aligned in a vertical line [fully strained line, red dashed line in Figure 3c] with $In_{0.16}Ga_{0.84}As$, which additionally confirms the pseudomorphic properties of the Ge layer. The 0.75% tensile strain within the Ge layer can reduce the band gap energy of Ge[14,16] and prevent the generation of misfit dislocations, all of which are desirable to improve the performance of TFET devices.

Further insight into the crystalline quality and the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface is provided by high resolution cross-sectional TEM analysis. For the sake of confirmation, TEM analysis was conducted on various spots and the representative results are shown in Figure 4. Figure 4a shows the cross-sectional TEM micrograph of the Ge/$In_{0.16}Ga_{0.84}As$ TFET structure with a low magnification and all layers are labeled in this figure. It can be seen that the $In_xGa_{1-x}As$ linearly graded buffer layer effectively accommodates the lattice mismatch between the $In_{0.16}Ga_{0.84}As$ channel/drain layers and the GaAs substrate by formation of dislocations. Most of the

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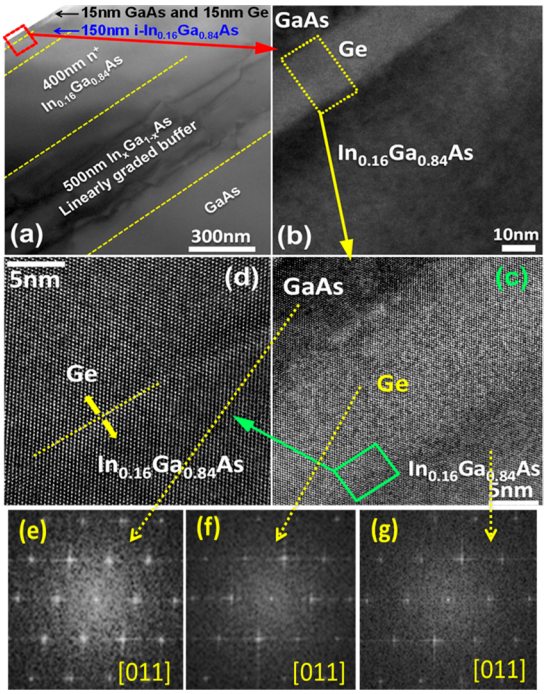

Figure 4. (a) Cross-sectional TEM micrograph of the TFET structure with each layer labeled in this figure. The $In_xGa_{1-x}As$ linearly graded buffer effectively accommodates the lattice mismatch between $In_{0.16}Ga_{0.84}As$ channel/drain layers and the GaAs substrate. No dislocations are observed in the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ active layers at this magnification. (b) High magnification TEM micrograph of the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ heterointerfaces. Uniform thickness of the Ge layer with a smooth Ge/$In_{0.16}Ga_{0.84}As$ heterointerface was observed in this figure in a relative long-range. A sharp Ge/$In_{0.16}Ga_{0.84}As$ heterointerface was also shown in this figure, indicating minimal atoms interdiffusion. (c) High-resolution TEM micrograph of the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ heterointerfaces. No dislocations were observed at the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface and within the Ge layer, suggesting the pseudomorphic of the Ge layer. (d) A zoomed-in view of the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface. A defect free interface with well aligned lattice indexing is shown in this figure. (e and f) fast Fourier transform patterns (FFT) corresponding to various layers marked with arrows in panel c.

dislocations were confined within the linearly graded $In_xGa_{1-x}As$ buffer. The $In_{0.16}Ga_{0.84}As$ channel/drain layers and the lattice matched GaAs/Ge source region has a minimal dislocation density which cannot be detected at this magnification. As the linearly graded buffer relaxed most of the lattice mismatch induced strain, the residual strain within the top $In_{0.16}Ga_{0.84}As$ channel/drain layers is small (<0.1%), which is in agreement with the XRD analysis. The graded buffer provided a high-quality "virtual" substrate for the active layers (GaAs/Ge/$In_{0.16}Ga_{0.84}As$) of the TFET structure. Further investigation of the tensile strained Ge layer and the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface were performed using a high magnification TEM micrograph as shown in Figure 4b. Uniform thickness of the Ge layer with a smooth Ge/$In_{0.16}Ga_{0.84}As$ heterointerface was observed in Figure 4b in a relative long-range. Figure 4b also shows high contrast between the Ge/$In_{0.16}Ga_{0.84}As$, as well as the GaAs/Ge heterointerfaces. The sharp Ge/$In_{0.16}Ga_{0.84}As$ heterointerface is also benefited to reduce the effective tunneling barrier width and increase in tunneling current of TFET devices.[2−7,21] High-resolution TEM micrograph of the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ heterointerfaces as indicated in the dashed box of Figure 4b is shown in Figure 4c. No dislocations were observed at the heterointerfaces, as well as within the Ge layer at this magnification, suggesting the pseudomorphic nature of the Ge which is consistent with the results from the XRD measurement. A selected high magnification view of the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface is shown in Figure 4d. A defect free interface with atomic scale periodicity can be observed in this figure. Figure 4e−g shows Fast Fourier Transform (FFT) patterns corresponding to the region marked with arrows in Figure 4(c). The indexing of these FFT patterns indicates that the electron beam was parallel to [011] orientation. It can also be observed that the FFT patterns recorded from various layers are similar with the same zone axis. Moreover, the FFT patterns obtained from both the interfacial areas are the same (Supporting Information Figure S2) with absence of any spot splitting or satellite peaks, which further indicates high quality epitaxial growth with coherent interfaces. The high-resolution TEM analysis of the Ge/$In_{0.16}Ga_{0.84}As$ heterostructure shows a sharp Ge/$In_{0.16}Ga_{0.84}As$ interface and dislocation free GaAs/Ge/$In_{0.16}Ga_{0.84}As$ active layers. The results from the TEM analysis indicate the high quality of the films with atomic smoothness reflecting the overall defect-free structure. This optimization of the growth parameters in conjunction with the atomic scale imaging is significant achievement toward demonstrating the correlated synthesis, structure−property behavior. In conjunction with the presence and control of the resulting tensile strain in Ge layer the intended property was obtained in terms of the band diagram.

Characterization of the surface morphology is another important metric for metamorphic structures due to the development and propagation of 60° $a/2$ ⟨110⟩ {111} misfit dislocations within the linearly graded buffer during the relaxation of strain.[22−24] These dislocations glide along {111} planes and thread at 60° angle toward the surface along ⟨110⟩ directions, resulting in a cross-hatch pattern on the sample surface.[22−24] Figure 5 shows the 20 μm × 20 μm AFM micrograph of the TFET structure, which shows the anticipated two-dimensional (2D) cross-hatch surface morphology. The 2D cross-hatch patterns are well-developed and quite uniform along the [110] and [1$\bar{1}$0] directions, as labeled in this figure. Line profiles in the two orthogonal ⟨110⟩ directions are also included in this figure, showing a low a peak-to-valley height of less than 5 nm. The uniform distribution of the cross-hatch pattern along [110] and [1$\bar{1}$0] directions suggests a symmetric strain relaxation of the linearly graded buffer layer. Besides, the AFM analysis shows a smooth surface with a root-mean-square (rms) roughness of 1.26 nm. The well-developed 2D cross-hatch pattern indicates ideal strain relaxation of the linearly graded buffer and low surface rms roughness suggests high crystalline quality of the TFET structure. Besides, the 2D cross-hatch pattern also confirm the strained nature of the Ge layer, otherwise, this cross-hatch pattern will be sheltered by dislocations and a grainy texture with much higher rms roughness will appear on the surface.[10]

The band alignment properties of the Ge/$In_{0.16}Ga_{0.84}As$ heterostructure were determined using XPS by measuring the binding energy from core levels (CL) of Ge3d/As3$d_{5/2}$ and valence band maxima (VBM) of Ge and $In_{0.16}Ga_{0.84}As$, respectively. XPS spectra were collected from three samples: (1) 15 nm Ge/150 nm $In_{0.16}Ga_{0.84}As$ was used to measure the CL and VBM binding energy of Ge; (2) 150 nm $In_{0.16}Ga_{0.84}As$ without the top Ge layer was used to measure the CL binding

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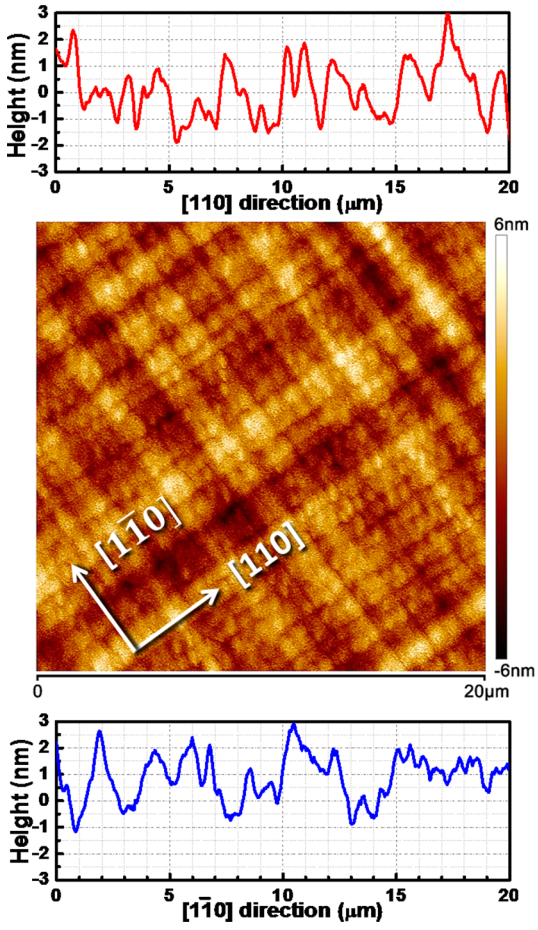

Figure 5. 20 μm × 20 μm AFM micrograph of the TFET structure shows anticipated two-dimensional cross-hatch patterns. Line profiles in the two orthogonal ⟨110⟩ directions are also included. The uniform distribution of the cross-hatch pattern along [110] and [1$\bar{1}$0] directions suggests a symmetric strain relaxation of the linearly graded buffer. The well-developed two-dimensional cross-hatch patterns suggest the pseudomorphic nature of the Ge layer. The AFM analysis shows a smooth surface morphology of the TFET structure with a root-mean-square (rms) roughness of 1.26 nm.

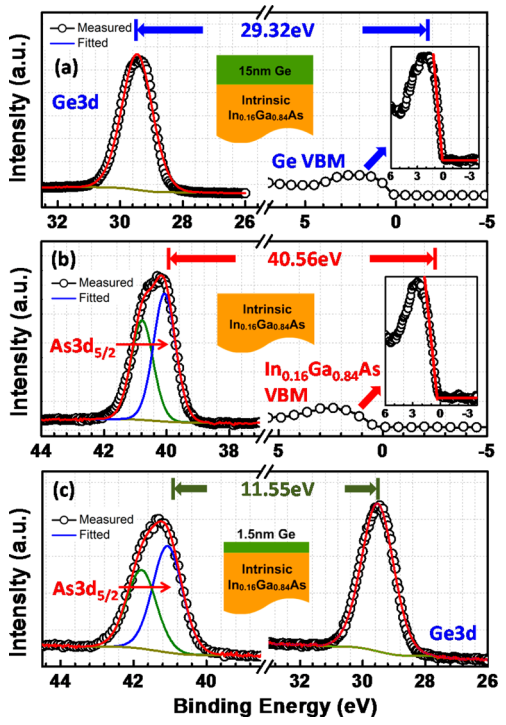

Figure 6. XPS spectra of (a) Ge3d core level and valence band from 15 nm Ge/150 nm $In_{0.16}Ga_{0.84}As$ sample, (b) As3d core level and $In_{0.16}Ga_{0.84}As$ valence band from 150 nm $In_{0.16}Ga_{0.84}As$ without the Ge layer, and (c) As3d and Ge3d core level from 1.5 nm Ge/150 nm $In_{0.16}Ga_{0.84}As$ measured at the interface. The inset shows the schematic layer diagram of the sample used in each measurement. The valence band offset value at Ge/$In_{0.16}Ga_{0.84}As$ heterointerface is determined to be 0.31 ± 0.05 eV using the measured XPS spectra.

energy of As and VBM of $In_{0.16}Ga_{0.84}As$; (3) 1.5 nm Ge/150 nm $In_{0.16}Ga_{0.84}As$ was used to measure CL binding energy of Ge and As at the heterointerface. Native oxide on the surface of each sample was removed using wet etching process.[18] The valence band offset (VBO) between Ge and $In_{0.16}Ga_{0.84}As$ can be determined by Kraut's[25] method:

$$\Delta E_V = (E^{Ge}_{Ge3d} - E^{Ge}_{VBM}) - (E^{InGaAs}_{As3d_{5/2}} - E^{InGaAs}_{VBM}) + \Delta E_{CL}(i) \quad (1)$$

where E^{Ge}_{Ge3d} and $E^{InGaAs}_{As3d_{5/2}}$ are CL binding energy of $In_{0.16}Ga_{0.84}As$ and Ge; E_{VBM} is the VBM of corresponding materials. E_{VBM} is determined by linearly fitting the leading edge of the VB spectra to the baseline.[21,25−29] $\Delta E_{CL}(i) = E^{InGaAs}_{As3d_{5/2}}(i) - E^{Ge}_{Ge3d}(i)$ is the CL binding energy difference between $As3d_{5/2}$ and Ge3d measured at the heterointerface. The conduction band offset (CBO) can be estimated by[21,25−29]

$$\Delta E_C = E^{InGaAs}_G - \Delta E_V - E^{Ge}_G \quad (2)$$

where E^{InGaAs}_G and E^{Ge}_G are the band gap energies of $In_{0.16}Ga_{0.84}As$ and Ge, respectively. Figure 6a−c shows the CL and VB spectra from each sample. The insect shows the schematic layer diagram of the sample used for each measurement. All measured binding energy values are summarized in Table 2. From the XPS measurements, the values of $E^{Ge}_{Ge3d} - E^{Ge}_{VBM}$, $E^{InGaAs}_{As3d_{5/2}} - E^{InGaAs}_{VBM}$, and $\Delta E_{CL}(i)$ are determined to be 29.32, 40.56, and 11.55 eV, respectively. The VBO is determined to be 0.31 ± 0.05 eV using eq 1. The uncertainty value is from the scatter of VB data with respect to the fitting in VBM position. The CBO value is determined using eq 2. The bandgap energy of intrinsic $In_{0.16}Ga_{0.84}As$ at 300 K is found to be ∼1.19 eV by the commonly used equation given by Nahory et al.[30] The reduced Ge indirect bandgap energy of 0.64 eV was used due to the splits of energy levels for the light hole and heavy hole bands at the VBM point caused by 0.75% tensile strain.[16,31] Using these data, the CBO is calculated to be ∼0.24 eV. Figure 7a shows the schematic band alignment diagram of the Ge/$In_{0.16}Ga_{0.84}As$ heterojunction

Table 2. Summary of Measured XPS CL and VBM Values from Different Samples

sample	states	binding energy (eV)
15 nm Ge/150 nm $In_{0.16}Ga_{0.84}As$	Ge3d	29.45
	VBM	0.13
150 nm $In_{0.16}Ga_{0.84}As$	$As3d_{5/2}$	41.05
	VBM	0.49
1.5 nm Ge/150 nm $In_{0.16}Ga_{0.84}As$	Ge3d	41.08
	$As3d_{5/2}$	29.53

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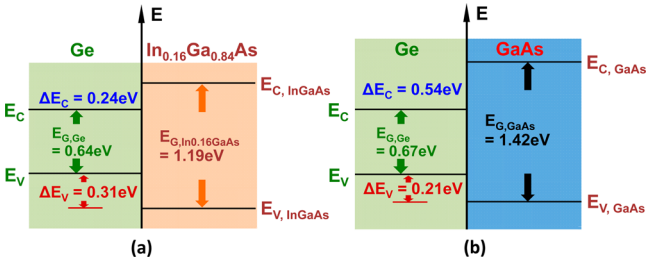

Figure 7. (a) Schematic energy band diagram of the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface in the TFET structure and (b) band diagram of the Ge/GaAs heterostructure. The conduction band offset was much reduced in the Ge/$In_{0.16}Ga_{0.84}As$ heterostructure by utilizing tensile strain inside of Ge.

based on the present result above. In addition, a Ge/GaAs TFET was also grown using the same in situ MBE growth process to compare the band alignment difference. The layer diagram of this structure is shown in the insect of Figure S1 in the Supporting Information. The band alignment properties of this structure were also investigated by XPS. The detailed XPS spectra can be found in Figure S3 of the Supporting Information and the energy band diagram of this structure is shown in Figure 7(b). The VBO and CBO values of Ge/GaAs TFET heterostructure were determined to be ~0.21 and ~0.54 eV, respectively. Compared with the measured band offset values from the Ge/$In_{0.16}Ga_{0.84}As$ structure (~0.31 eV for VBO and ~0.24 eV for CBO), it can be seen that the VBO value increased with the increase of In composition but the CBO value decreased. Besides, preliminary band alignment studies of a Ge/$In_{0.53}Ga_{0.47}As$ heterostructure showed further reduction of CBO and a staggered band alignment, which can be found in Figure S5–S7 of the Supporting Information. The increase of In composition in InGaAs layer will reduce the bandgap energy of InGaAs material, increase the amount of in-plane tensile strain of the Ge layer deposited on InGaAs and decrease the effective tunneling barrier height ($E_{beff} = E_{G,Ge} + \Delta E_C$), all of which will improve the performance of TFET devices. However, further increase of In composition in InGaAs layer will drastically reduce the critical layer thickness of Ge (e.g., the critical thickness of Ge on $In_{0.16}Ga_{0.84}As$ is ~25 nm and it reduced to ~7.6 nm if the In composition is increased to 53%) and thus potentially introduce defects at the heterointerface and inside the Ge layer,[13] which is detrimental for device performances.[10,13,26] As a result, a balance of Indium composition is essential to obtain a tensile strained Ge layer with defect-free high crystalline quality.

In summary, tensile strained Ge/$In_{0.16}Ga_{0.84}As$ TFET heterostructure was grown in situ by molecular beam epitaxy using two separated growth chambers for Ge and III–V materials connected by high vacuum transfer chamber. Symmetric (004) and asymmetric (115) X-ray reciprocal space maps show 0.75% in-plane tensile strain within Ge layer. The relaxation of Ge layer with respect to $In_{0.16}Ga_{0.84}As$ is limited to 9%. High-resolution TEM studies confirmed the pseudomorphic nature of the Ge layer with high crystalline quality as well as a sharp and defect-free Ge/$In_{0.16}Ga_{0.84}As$ heterointerface. Uniform two-dimensional cross-hatch surface morphology was revealed by atomic force microscopy with a smooth surface root-mean-square roughness of 1.26 nm. X-ray photoelectron spectroscopy measurements show a reduced effective tunneling barrier height compared with the Ge/GaAs TFET structure, indicating higher tunneling current in fabricated devices. The high quality tensile strained Ge/$In_{0.16}Ga_{0.84}As$ heterostructure showed superior structural properties that would provide a new path for high performance and low standby power tunnel field-effect transistor applications.

■ ASSOCIATED CONTENT

Supporting Information

Details of the Ge/GaAs TFET structure used for comparison are provided. X-ray rocking curve of this structure along with XPS spectra and band alignment measurements are also included in the Supporting Information. The preliminary band alignment study of a Ge/$In_{0.53}Ga_{0.47}As$ structure is also shown in the Supporting Information.This material is available free of charge via the Internet at http://pubs.acs.org.

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The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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