Applied Physics Express **8**, 025501 (2015)
http://dx.doi.org/**10.7567/APEX.8.025501**

Mixed-anion $GaAs_{1-y}Sb_y$ graded buffer heterogeneously integrated on Si by molecular beam epitaxy

Mantu K. Hudait*, Yan Zhu, Patrick Goley, Michael Clavel, and Nikhil Jain

Advanced Devices and Sustainable Energy Laboratory (ADSEL), Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA 24061, U.S.A.
E-mail: mantu.hudait@vt.edu

Received November 25, 2014; accepted December 19, 2014; published online January 16, 2015

The growth, strain relaxation, and defect properties of a step-graded mixed-anion $GaAs_{1-y}Sb_y$ buffer with a lattice misfit of >12% on a 6° off-cut (100) Si substrate grown by molecular beam epitaxy (MBE) have been investigated. This metamorphic graded buffer exhibited efficient strain relaxation and low threading dislocation densities of $\leq 10^7$ cm^{-2} in the investigated range of misfits. High-resolution X-ray diffraction measurement demonstrated nearly ideal strain relaxation behavior with a surface rms roughness of ~3.5 nm, which is attributed in part to dislocation glide. Thus, MBE-grown $GaAs_{1-y}Sb_y$ anion-graded buffers are a promising "virtual substrate" technology for extending the performance and application of 6.1 Å device technology.

The mixed-anion graded buffer, $GaAs_{1-y}Sb_y$ with a tailor-made antimony composition heterogeneously integrated on Si is a promising material for both low-power tunnel transistor and solar cell applications owing to their wide range of bandgap energies from 0.70 to 1.42 eV. Mixed arsenide/antimonide-based $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ heterostructures with an abundance of internally lattice-matched combinations as a result of varying the concentrations of both antimony (Sb) and indium (In) can be achieved in a tunnel field effect transistor (TFET) configuration with adjustable effective tunnel barrier height.[1–4] Moreover, $GaAs_{1-y}Sb_y$ alloys are also of interest for compositionally graded metamorphic buffer applications, where the span of lattice constants between GaAs and GaSb provides an opportunity for generating a "virtual substrate" on the Si substrate to support a wide variety of lattice-mismatched devices based on $InAs_{1-y}P_y$, $In_xGa_{1-x}As$, and $In_xAl_{1-x}As$.[4–9] Very recently, heterojunction TFET structures based on the $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ system, where the Sb and In compositions required for optimal TFET performance is in the range of 0.5 to 1, have enabled band alignment from the staggered to broken gap configurations that generate a significant lattice mismatch with respect to the Si substrate.

At present, the graded $In_xAl_{1-x}As$ buffer on InP is considered to bridge the lattice constant from the InP substrate to the required In composition in the $In_xGa_{1-x}As$ ($x > 0.53$) layer for a mixed As/Sb-based TFET device structure.[1–4] However, no clear heterogeneous integration scheme was established for such a TFET structure on a Si substrate. Using a graded $GaAs_{1-y}Sb_y$ buffer layer on Si, one can integrate the $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ tunnel FET structure, in which the uppermost constant composition of the $GaAs_{1-y}Sb_y$ buffer can be internally lattice matched with the $In_xGa_{1-x}As$ layer and this buffer layer can also serve as a drain layer in the n-channel TFET structure. In such a case, the use of an anion (group-V)-mixed alloy, $GaAs_{1-y}Sb_y$, as the compositionally graded buffer on Si, compared with more common graded-buffer alloy choices such as $In_xAl_{1-x}As$ with a GaAs intermediate layer, offers a potential advantage since the control of growth rate (Ga flux) is independent of the control of the layer composition (As/Sb flux ratio). In fact, Sb can help reduce the number of dislocations due to the surfactant-mediated growth of the $GaAs_{1-y}Sb_y$ graded buffer on Si and thus has a potential advantage of enabling the design of a metamorphic TFET device structure. However, measures must be taken during the molecular beam epitaxy (MBE) growth of such a material owing to a strong competition between the different incorporation rates of anions (As and Sb) due to their dissimilar sticking coefficients.[5,6,10] In this paper, we focus on the first study of the solid-source MBE growth, and structural and strain relaxation properties of the graded metamorphic $GaAs_{1-y}Sb_y$ buffer with an Sb alloy composition of up to 55% heterogeneously integrated on Si. The strain relaxation properties of this $GaAs_{1-y}Sb_y$ buffer were evaluated by high-resolution X-ray diffraction measurement. Cross-sectional transmission electron microscopy (TEM) was used to investigate the defect properties, and the surface morphology was analyzed by atomic force microscopy (AFM).

The $GaAs_{1-y}Sb_y$ graded buffer was grown by Veeco Gen-II solid-source MBE on a (100) Si substrate with a 6° off-cut towards the ⟨110⟩ direction, and the Sb flux was provided by a low-temperature 125 cm^3 Sb effusion cell. A valve cracker arsenic source with a 900 °C cracker temperature ensured a consistent As_2 flux was used during growth. The Ga beam equivalent pressure was kept at 2.92×10^{-7} Torr, corresponding to a growth rate of ~0.5 µm/h, as determined from reflection high-energy electron diffraction (RHEED) intensity oscillation. The fixed As_2/Ga ratio of 10 and Sb/Ga ratios of 1, 2, and 6.16 were used for $GaAs_{1-y}Sb_y$ growth on Si at a substrate temperature of 440 °C, measured using a thermocouple. Since the final Sb alloy composition of ~50% in $GaAs_{1-y}Sb_y$ was needed to be lattice matched with InP, the targeted Sb/Ga ratio was carefully selected to provide the final Sb composition of ≥50% in the graded $GaAs_{1-y}Sb_y$ buffer. The thickness of each step was fixed to 500 nm. The alloy composition and strain relaxation properties of the $GaAs_{1-y}Sb_y$ layer were characterized by measuring the $\omega/2\theta$ scan and reciprocal space maps (RSMs) using a Panalytical X'pert Pro system with Cu Kα_1 as the X-ray source. The structural and defect properties of the $GaAs_{1-y}Sb_y$ step-graded buffer were analyzed by cross-sectional TEM using a Philips EM420 microscope. The electron-transparent foil of thin-film cross sections of $GaAs_{1-y}Sb_y$/GaAs/Si were prepared by standard mechanical polishing followed by Ar^+ ion milling.

Figure 1 shows the schematic of the step-graded $GaAs_{1-y}Sb_y$ buffer on Si, and Fig. 2 shows the corresponding (004)

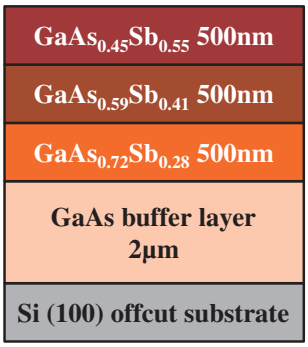

Fig. 1. Schematic of the $GaAs_{1-y}Sb_y$ graded-buffer layer structure on Si.

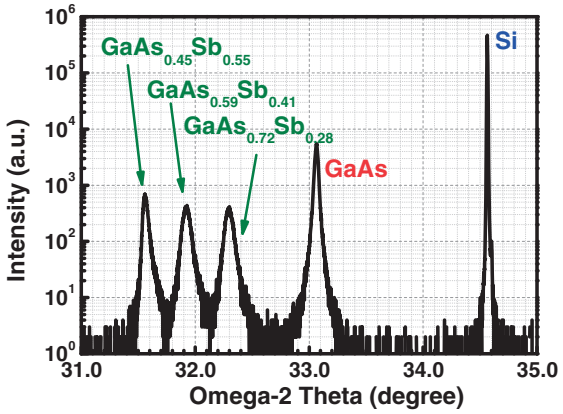

Fig. 2. $\omega/2\theta$ scan of the $GaAs_{1-y}Sb_y$ graded-buffer layer structure on Si substrate. The measured Sb composition of each layer is given at the corresponding peak position.

$\omega/2\theta$ scan of this structure. The three-step $GaAs_{1-y}Sb_y$ graded-buffer layer was grown on the Si substrate using an intermediate GaAs layer, and the Sb alloy composition measured from each layer peak is labeled in this figure. It can be seen from Fig. 2 that by varying the Sb/Ga ratio with a fixed As_2/Ga ratio and substrate temperature, the Sb composition can be precisely controlled in a wide range between 28 and 55%. More recently, we have demonstrated a wide range of Sb compositions from 15 to 62% in the graded $GaAs_{1-y}Sb_y$ layer grown on GaAs by varying growth parameters such as the As_2/Ga ratio, Sb/Ga ratio, and the substrate temperature during MBE growth using the same Sb effusion cell and arsenic valve cracker source.[11] The Sb alloy composition can be well controlled in accordance with application and device-specific requirements, such as (i) a low Sb composition of 15% in $GaAs_{1-y}Sb_y$ used in dislocation filters in multijunction solar cells,[12] (ii) 25% Sb for a 1.55 μm InAs quantum dot laser,[8,9] (iii) 35% Sb for p–i–n detectors,[6] (iv) 50% Sb for lattice matching with InP for TFETs,[13] and (v) an Sb composition >60% for a metamorphic mixed As/Sb-based InGaAs/GaAsSb heterostructure TFET.[1–4]

The strain relaxation state in each step of the $GaAs_{1-y}Sb_y$ graded buffer was analyzed using symmetric (004) and asymmetric (115) RSMs. Figure 3 shows the (a) symmetric (004) and (b) asymmetric (115) RSMs, and reciprocal lattice points (RLPs), corresponding to $GaAs_{1-y}Sb_y$ materials with different Sb compositions, are indicated in this figure. From the measured RSMs, the out-of-plane lattice constant c (from

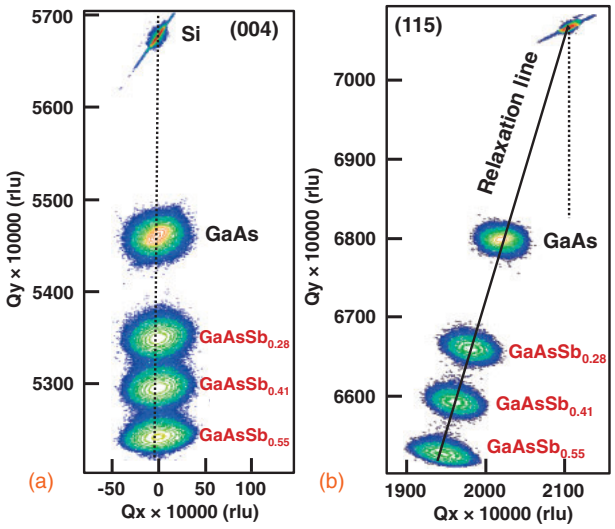

Fig. 3. (a) Symmetric (004) and (b) asymmetric (115) RSMs of the $GaAs_{1-y}Sb_y$ graded-buffer layer structure on Si. The measured Sb composition is indicated at each reciprocal lattice point. Each layer in the metamorphic step-graded $GaAs_{1-y}Sb_y$ buffer is fully relaxed with respect to the Si substrate.

the symmetric 004 reflection) and the in-plane lattice constant a (from the asymmetric 115 reflection) were determined. The relaxed lattice constant a_r and strain relaxation values were extracted by the method described in Ref. 14. The near complete relaxation of each step in the $GaAs_{1-y}Sb_y$ and GaAs layers on Si was achieved, which demonstrates the metamorphic nature of the graded buffer. From the measured alloy compositions, it can be seen that the Sb composition is directly dependent on the Sb/Ga flux ratio. One can also find, from the RSMs in Fig. 3, that the RLP for each layer in the graded $GaAs_{1-y}Sb_y$ buffer is almost centered on the line extending between the Si substrate RLP and the $Q = 0$ line, indicating that each layer in the graded buffer possesses a minimum lattice tilt with respect to the Si substrate. Moreover, all the RLPs lie on the complete-relaxation line, as shown in Fig. 3(b), which further indicates the fully relaxed state of the metamorphic-graded $GaAs_{1-y}Sb_y$ layer.

To gain further insight into the structural quality and defect properties, cross-sectional TEM was performed. Figures 4(a) and 4(b) show a cross-sectional TEM micrograph and a high-resolution TEM micrograph of the $GaAs_{1-y}Sb_y$ graded buffer on Si, respectively. The thickness of each layer is indicated in these figures. In this work, the Ga beam flux (2.92×10^{-7} Torr) was kept constant for a growth rate of ~0.5 μm/h during the entire GaAsSb graded-buffer layer growth. The Sb fluxes were (i) 2.9×10^{-7} Torr (425 °C Sb effusion cell temperature), (ii) 6.0×10^{-7} Torr (at 444 °C), and (iii) 1.8×10^{-6} Torr (at 465 °C) for 28% Sb, 41% Sb, and 55% Sb alloy compositions, respectively. The GaAs buffer layer thickness was targeted to be 2 μm at a growth rate of 2.8 Å/s on the basis of RHEED oscillation results. The cross-sectional TEM measurement exhibited a thickness of 2.09 μm, which corresponds to a growth rate of 2.9 Å/s. The thicknesses of the graded GaAsSb buffer layer were 553, 519, and 507 nm for Sb compositions of 28, 41, and 55%, respectively, as shown in Fig. 4(b). A growth rate of 1.4 Å/s was targeted by adjusting the Ga flux for each Sb composition, and the growth rates of 1.54 Å/s for 28% Sb composition, 1.44 Å/s

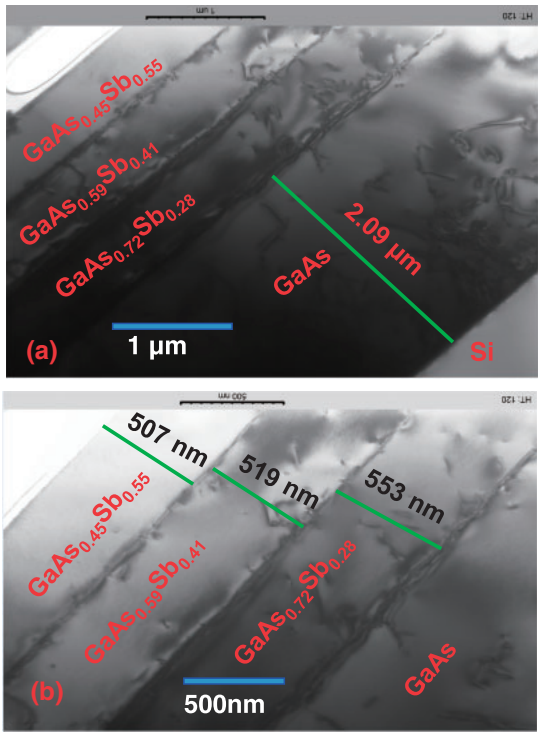

Fig. 4. (a) Cross-sectional TEM micrograph of the full layer structure on Si and (b) TEM micrograph of the step-graded metamorphic $GaAs_{1-y}Sb_y$ buffer on Si having Sb compositions of 28, 41, and 55%. The thickness of each layer is indicated in (b). The threading dislocations are well controlled in the step-graded buffer and graded $GaAs_{1-y}Sb_y$ buffer with the uppermost composition serving as a "virtual" substrate platform for the TFET or mismatch device applications. Moreover, sharp heterointerfaces are observed between $GaAs_{1-y}Sb_y$ stepped-composition epilayers.

for 41% Sb composition, and 1.41 Å/s for 55% Sb composition, respectively, were achieved, as measured from the TEM micrograph shown in Fig. 4(b). The slight change in thickness set on the basis of RHEED intensity oscillations and measured on the cross-sectional TEM image, could be due to the pause in growth at each interface of GaAsSb to change the Sb effusion cell temperature for the adjustment of the required flux for subsequent layer growth or due to the minimal decrease in the growth rate owing to antimony flux. However, these TEM micrographs show a high contrast at the graded buffer layer interfaces owing to misfit dislocations, with no threading dislocations observable in the $GaAs_{0.45}Sb_{0.55}$ uppermost layer at this magnification scale, indicating a threading dislocation density (TDD) in the $GaAs_{0.45}Sb_{0.55}$ layer on the order of or below $\sim 10^7\,cm^{-2}$. In order to achieve TDD lower than $10^7\,cm^{-2}$, the defect density inside the GaAs layer must be low. Two possible ways to achieve this are to incorporate thermal cycle annealing during the growth of the GaAs layer[15] or to incorporate a strained layer[16] to reduce the number of dislocations prior to the growth of the GaAsSb layer. The maximum-Sb-composition $GaAs_{0.45}Sb_{0.55}$ layer can be lattice matched with the $In_xGa_{1-x}As$ layer with 66% indium alloy composition, and the $GaAs_{0.45}Sb_{0.55}/In_{0.66}Ga_{0.34}As$ heterostructure can be used for a staggered gap TFET device structure.

It is important to characterize the surface morphology of the metamorphic structure because of the expected cross-hatch resulting from ideal strain relaxation with a minimum concentration of threading dislocations, as this is an important

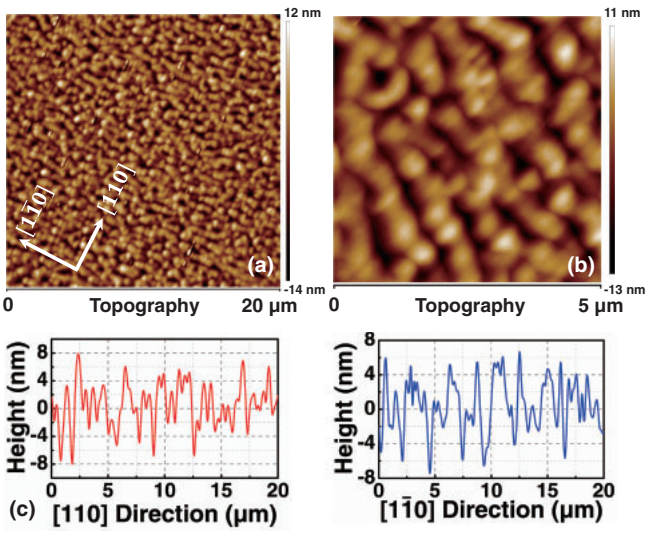

Fig. 5. AFM micrographs of the surface of $GaAs_{0.45}Sb_{0.55}$ in (a) 20×20 and (b) $5 \times 5\,\mu m^2$ area scans. The rms roughness values were determined to be approximately 3.7 nm from the $20 \times 20\,\mu m^2$ scan and 3.5 nm from the $5 \times 5\,\mu m^2$ area scan. Line profiles along the two orthogonal ⟨110⟩ directions are also taken from the $20 \times 20\,\mu m^2$ scan and are shown in (c).

figure of merit for a metamorphic buffer on Si. Figure 5 shows the AFM micrographs of the surface of $GaAs_{0.45}Sb_{0.55}$ in (a) 20×20 and (b) $5 \times 5\,\mu m^2$ area scans. Line profiles along the two orthogonal ⟨110⟩ directions are also taken from the $20 \times 20\,\mu m^2$ scan and are shown in Fig. 5(c). This uniform pattern from the surface of the graded $GaAs_{1-y}Sb_y$ buffer on Si is an indication of full relaxation, which is in complete agreement with the X-ray and analytical results presented above. Moreover, the uniform surface pattern predicts a lower defect density, which is supported by the TEM analytical results. The rms roughness of the $GaAs_{0.45}Sb_{0.55}$ layer is $\sim$3.7 nm measured over the $20 \times 20\,\mu m^2$ area and $\sim$3.5 nm for the $5 \times 5\,\mu m^2$ area, indicating film uniformity on Si. This surface morphology corresponds to the strain relaxation properties of the graded buffer layers, which is in agreement with the literature.[11,17,18] The surface roughness of the GaAsSb graded buffer can be lowered by using an antimony valve cracker source during MBE growth, since Sb_2 species have higher surface adatom mobilities than Sb_4 species. These surface roughness values are rather high, although they are comparable to the reported results for metamorphic graded buffers with lattice mismatch in the range from 4 to 8%.[1,19–25] In this study, the lattice mismatch of the uppermost $GaAs_{0.45}Sb_{0.55}$ layer is >12% with respect to the Si substrate, and the lattice-mismatch-induced surface roughness cannot be avoided for metamorphic growth. However, the defect control within the buffer and the uppermost $GaAs_{0.45}Sb_{0.55}$ layer of interest is an important design criterion for a lattice-mismatch system and can severely impact the device performance. In order to accommodate the lattice-mismatch-induced defects between the top $GaAs_{0.45}Sb_{0.55}$ layer and the Si substrate, a two-step-graded GaAsSb buffer layer with different Sb compositions was incorporated. Superior device (quantum well transistors, FETs, tunnel diodes, and TFETs)[1,19–25] performances were achieved when the surface rms roughness was similar to or higher than the results reported in this work. Therefore, one can achieve excellent metamorphic device performance on this virtual substrate.

In conclusion, the growth, strain relaxation behavior, and defect properties of MBE-grown, compositionally graded mixed-anion $GaAs_{1-y}Sb_y$ buffer grown on an off-cut (001) Si substrate with a lattice misfit >12% were investigated. Nearly ideal compressive strain relaxation behavior was observed with low surface rms roughness, which correlates with low threading dislocation density in the buffer. We attribute this behavior in part to dislocation glide. Therefore, MBE-grown mixed-anion $GaAs_{1-y}Sb_y$ step-graded buffers are a promising virtual substrate technology for extending the performance and application of 6.1 Å device technology, since they enable various combinations of bandgaps and band alignment while maintaining the high material quality.

Acknowledgments This work is supported in part by Intel Corporation. Y.Z. and M.C. acknowledge the financial support from NSF under grants number ECCS-1028494 and ECCS-1348653, respectively. P.G. acknowledges support from the National Science Foundation Graduate Research Fellowship under grant number DGE 0822220. The authors would like to acknowledge NCFL — Institute for Critical Technology and Applied Sciences (ICTAS) and Virginia Tech Nanofabrication Facilities for materials characterization.

1) Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, J. Appl. Phys. **112**, 024306 (2012).
2) Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, Appl. Phys. Lett. **101**, 112106 (2012).
3) B. Rajamohanan, D. Mohata, Y. Zhu, M. Hudait, Z. Jiang, M. Hollander, G. Klimeck, and S. Datta, J. Appl. Phys. **115**, 044502 (2014).
4) Y. Zhu and M. K. Hudait, Nanotechnol. Rev. **2**, 637 (2013).
5) A. Bosacchi, S. Franchi, P. Allegri, V. Avanzini, A. Baraldi, R. Magnanini, M. Berti, D. De Salvador, and S. K. Sinha, J. Cryst. Growth **201–202**, 858 (1999).
6) S. Xiaoguang, W. Shuling, J. S. Hsu, R. Sidhu, X. G. Zheng, X. Li, J. C. Campbell, and A. L. Holmes, IEEE J. Sel. Top. Quantum Electron. **8**, 817 (2002).
7) H. Shimizu and S. Saravanan, Appl. Phys. Lett. **88**, 041119 (2006).
8) Y. Qiu, T. Walther, H. Y. Liu, C. Y. Jin, M. Hopkinson, and A. G. Cullis, in *Microscopy of Semiconducting Materials 2007*, ed. A. G. Cullis and P. A. Midgley (Springer, Dordrecht, 2008) Vol. 120, p. 263.
9) H. Y. Liu, Y. Qiu, C. Y. Jin, T. Walther, and A. G. Cullis, Appl. Phys. Lett. **92**, 111906 (2008).
10) S. P. Bremner, G. M. Liu, N. Faleev, K. Ghosh, and C. B. Honsberg, J. Vac. Sci. Technol. B **26**, 1149 (2008).
11) Y. Zhu, M. Clavel, P. Goley, and M. K. Hudait, J. Appl. Phys. **116**, 134304 (2014).
12) O. Morohara, H. Geka, Y. Moriyasu, and N. Kuze, 40th IEEE Photovoltaic Specialists Conf., 2014.
13) D. K. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu, and S. Datta, IEDM Tech. Dig., 2011, p. 781.
14) M. K. Hudait, Y. Lin, and S. A. Ringel, J. Appl. Phys. **105**, 061643 (2009).
15) T. Soga, T. Kato, M. Umeno, and T. Jimbo, J. Appl. Phys. **79**, 9375 (1996).
16) Y. Takano, M. Hisaka, N. Fujii, K. Suzuki, K. Kuwahara, and S. Fuke, Appl. Phys. Lett. **73**, 2917 (1998).
17) D. Lubyshev, J. M. Fastenau, Y. Qiu, A. W. K. Liu, E. J. Koerperick, J. T. Olesberg, D. Norton, N. N. Faleev, and C. B. Honsberg, Proc. SPIE **8704**, 870412 (2013).
18) D. Wang, Y. Lin, D. Donetsky, G. Kipshidze, L. Shterengas, G. Belenky, S. P. Svensson, W. L. Sarney, and H. Hier, Proc. SPIE **8704**, 870410 (2013).
19) M. K. Hudait, G. Dewey, S. Datta, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit, and R. Chau, IEDM Tech. Dig., 2007, p. 625.
20) M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, IEDM Tech. Dig., 2009, p. 319.
21) N. Mukherjee, J. Boardman, B. Chu-Kung, G. Dewey, A. Eisenbach, J. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, M. Radosavljevic, T. Stewart, H. W. Then, P. Tolchinsky, and R. Chau, IEDM Tech. Dig., 2011, p. 821.
22) I. García, J. F. Geisz, R. M. France, J. Kang, S.-H. Wei, M. Ochoa, and D. J. Friedman, J. Appl. Phys. **116**, 074508 (2014).
23) Y.-S. Lin, Y.-C. Ma, and Y.-T. Lin, J. Electrochem. Soc. **158**, H305 (2011).
24) R. J. W. Hill, C. Park, J. Barnett, J. Price, J. Huang, N. Goel, W.-Y. Loh, J. Oh, C. E. Smith, P. Kirsch, P. Majhi, and R. Jammy, IEDM Tech. Dig., 2010, p. 130.
25) Y. Zhu, D. K. Mohata, S. Datta, and M. K. Hudait, IEEE Trans. Device Mater. Reliab. **14**, 245 (2014).