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Integration of $SrTiO_3$ on Crystallographically Oriented Epitaxial Germanium for Low-Power Device Applications

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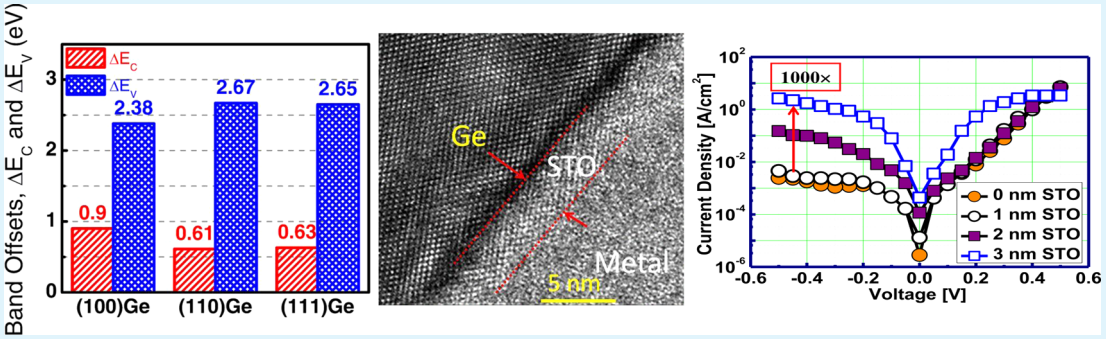
Supporting Information



ABSTRACT: $SrTiO_3$ integration on crystallographic oriented (100), (110), and (111) epitaxial germanium (Ge) exhibits a potential for a new class of nanoscale transistors. Germanium is attractive due to its superior transport properties while $SrTiO_3$ (STO) is promising due to its high relative permittivity, both being critical parameters for next-generation low-voltage and low-leakage metal-oxide semiconductor field-effect transistors. The sharp heterointerface between STO and each crystallographically oriented Ge layer, studied by cross-sectional transmission electron microscopy, as well as band offset parameters at each heterojunction offers a significant advancement for designing a new generation of ferroelectric-germanium based multifunctional devices. Moreover, STO, when used as an interlayer between metal and n-type (4×10^{18} cm^{-3}) epitaxial Ge in metal–insulator–semiconductor (MIS) structures, showed a 1000 times increase in current density as well as a decrease in specific contact resistance. Furthermore, the inclusion of STO on n-Ge demonstrated the first experimental findings of the MIS behavior of STO on n-Ge.

KEYWORDS: *germanium, strontium titanate, epitaxy, molecular beam epitaxy, heterostructure*

INTRODUCTION

Shrinking feature sizes of Si nanoscale transistors have enabled an increase in transistor densities, resulting in an increase in the power consumption of high-density integrated circuits. This trend in increasing transistor density has been central to realizing cost-effective, powerful computing systems for several decades. However, further downscaling of Si transistors faces several critical issues due to the increasing difficulty in reducing supply voltage (V_{DD}), and an increase in leakage current that degrades the switching current ratio between the ON and OFF states. Lowering V_{DD} can reduce dynamic power quadratically and leakage power linearly; however, the lower operating electric field also results in a lower carrier velocity and, hence, reduced transistor ON current. The decrease in gate voltage also increases the leakage power due to a lower voltage range available in which to turn off the transistor. One enticing approach is to change the transistor architecture from planar to fin field-effect transistors (FinFETs), where the "fin" design allows the gate to control the channel from three sides as opposed to one.[1,2] In parallel, crystallographically oriented (100) and (110) low band gap, high-mobility germanium (Ge) is substituted as the channel material,[3] allowing for device operation below 0.5 V V_{DD} while maintaining high performance. Ge has great potential due to its low-field bulk mobility gains of up to 2× for electrons and 4× for holes when compared with Si. Indeed, the hole mobility in (110)Ge channels oriented along the ⟨110⟩ direction exhibits a 2.3× mobility increase compared with (100)Ge, while the electron mobility in (111)-oriented Ge is 1.8× higher than both (100) Ge and (110)Ge orientations.[4−8] Furthermore, with continued transistor scaling, high electron mobility channel materials and device architectures based on $In_xGa_{1-x}As$ ($0.53 \leq x \leq 1$) were demonstrated on Si substrates, while for complementary CMOS logic application, high hole mobility and high-

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performance p-channel materials are mandatory. In this regard, Ge has received a great deal of attention as a p-channel material for next-generation low-power transistors due to its higher bulk hole mobility than Si or any of the III−V materials.

Epitaxial lattice matched Ge with different surface orientations can be tailor-made on different oriented GaAs substrates.[9] Considering several material choices, Ge epitaxial films grown on a large band gap GaAs material is of immense interest due to their lattice matched nature (mismatch ~0.07%) which ensures larger critical layer thickness, lower dislocation density, and a strain-free Ge epitaxial film.[9] Very recently, the epitaxial growth of Ge on Si with a large band gap AlAs/GaAs buffer layer was demonstrated,[10] which provides a larger valence band offset for carrier confinement, eliminates parallel conduction to the Ge channel, prevents interdiffusion, and creates a common buffer layer platform for both n- and p-channel transistor structures on Si for the realization of ultra-low-power and high-speed CMOS logic applications.

To date, Si nanoscale transistors utilize HfO_2 as a gate dielectric. The introduction of new channel materials, such as Ge and InGaAs, for next-generation nanoscale transistors warrants a need for complex oxides with higher dielectric constants (referred to as high-k dielectrics) that have the potential to decrease the electrical equivalent oxide thickness (EOT) below 1 nm. In the past, several complex oxides[11−14] such as $SrTiO_3$, $BaTiO_3$, $MgAl_2O_4$, $PbZr_xTi_{1-x}O_3$, and $La_xSr_{1-x}MnO_3$ have been explored as a replacement for SiO_2 in Si transistors to overcome the fundamental physical limitations of EOT as well as act as an effective insulator for Si metal−oxide−semiconductor field effect transistors (MOSFETs). Among all reported complex oxides, the perovskite-type complex oxide $SrTiO_3$ (STO) has been widely studied for integration with Si[14−19] and GaAs.[20−24] The combination of STO and crystallographically oriented epitaxial Ge merges the rich properties of perovskite oxides[25−29] with the superior transport properties of Ge, resulting in a new class of heterostructures with novel materials properties that offer the potential for a range of multifunctional devices, including optoelectronics, nanoelectronics, and memory.[30−34] The experimental band offset data for the STO/Ge heterointerface with epitaxial (100)Ge, (110)Ge, and (111)Ge has not been reported yet and it is important to know this information to determine the functional range of STO on Ge. The functionalities include the use of STO as a gate dielectric as well as for forming low- resistance ohmic contacts to n-type Ge, which is essential in achieving higher transistor drive current at low V_{DD}. To achieve a low specific contact resistance to n-type Ge via metal−insulator−semiconductor (MIS) contacts, a thin STO layer with a low conduction band offset (ΔE_C) with respect to Ge is essential. Very recently, a unified model was proposed to achieve a low specific contact resistance on n-type Ge from a series of insulating materials, in which STO was found to be one of the promising candidates[35] due to its higher dielectric constant. However, the conduction band offset results of each STO/Ge heterojunction depend primarily on the ability to accurately determine the band gap of STO.

In this paper, we demonstrate the growth, band alignment properties, MIS contact behavior, and specific contact resistance studies of pulsed laser deposited STO on epitaxial (100)Ge, (110)Ge, and (111)Ge layers grown using molecular beam epitaxy. The valence and conduction band discontinuities, ΔE_V and ΔE_C, for each STO/Ge heterojunction were larger than 2 and 0.5 eV, respectively, which is sufficient to serve as a blocking barrier for holes and electrons in low-power device applications, i.e., if the driving voltage of the transistor is less than 0.5 V. Furthermore, the thin STO layer can also facilitate low specific MIS contact resistance, as suggested in ref 35. In addition, the 1000× increase in current density after the insertion of a 3 nm STO layer between the titanium (Ti) metal and n-type (~6×10^{16} cm^{-3}) bulk Ge layer is indicative of a lower Schottky barrier height, resulting in contact resistivity on the order of 1×10^{-3} Ω-cm^2 on n-type (4×10^{18} cm^{-3}) epitaxial (100)Ge and (110)Ge layers, thus establishing STO as a favorable candidate in next-generation low-power Ge nanoscale devices.

RESULTS AND DISCUSSION

Material Characterization. Figure 1 shows the high-resolution triple-axis (004) symmetric X-ray rocking curve from the 200 nm Ge epilayer grown on a (100)GaAs substrate. The peak separation between the Ge epilayer and the GaAs substrate is approximately 180 arc-sec, as shown in Figure 1. The X-ray rocking curve also shows the appearance of strong Pendellösung oscillation fringes on both sides of the Ge/GaAs peaks, implying the presence of a parallel and sharp heterointerface. In reality, the strong interference fringes can only be observed in a structure that has near ideal parallel boundaries. Similar X-ray rocking curves from (110)Ge and (111)Ge orientations were reported earlier.[9] The reciprocal space map (RSM) exhibits two distinct reciprocal lattice point maxima corresponding to the GaAs substrate and the Ge epilayer (not shown here). When translated into the RSM, the thickness of the fringes shown in Figure 1 become contours of intensity.[9] The degree of relaxation of the Ge epilayer was found to be less than 5% with respect to the GaAs substrate. Such minimal relaxation is expected due to the quasi-lattice matched nature (~0.07% lattice mismatch) of the Ge/GaAs heterostructure.

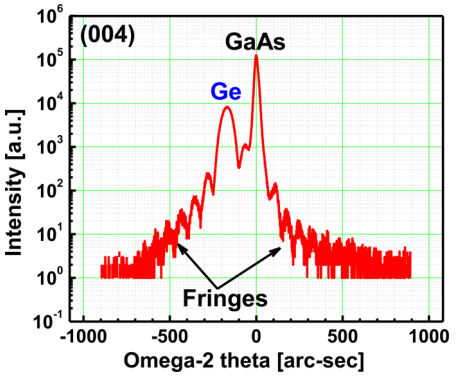

Figure 1. X-ray rocking curve from the 200 nm thick Ge grown on (100)GaAs substrate showing the Pendellösung oscillation fringes indicating a superior quality Ge layer and Ge/GaAs heterointerface.

Figure 2a−d shows the cross-sectional transmission electron microscopy (TEM) micrographs of the STO/(110)Ge/(110)GaAs structure showing the interface of STO/(110)Ge/(110)GaAs. The relative uniformity of the STO/Ge interface is visible in the high-resolution TEM micrograph of the STO/(110)Ge and STO/(100)Ge heterojunctions, respectively. These micrographs also demonstrate the sharp nature of the heterointerfaces. Furthermore, the TEM results demonstrate the high degree of coherency of the pulse laser deposited ~15

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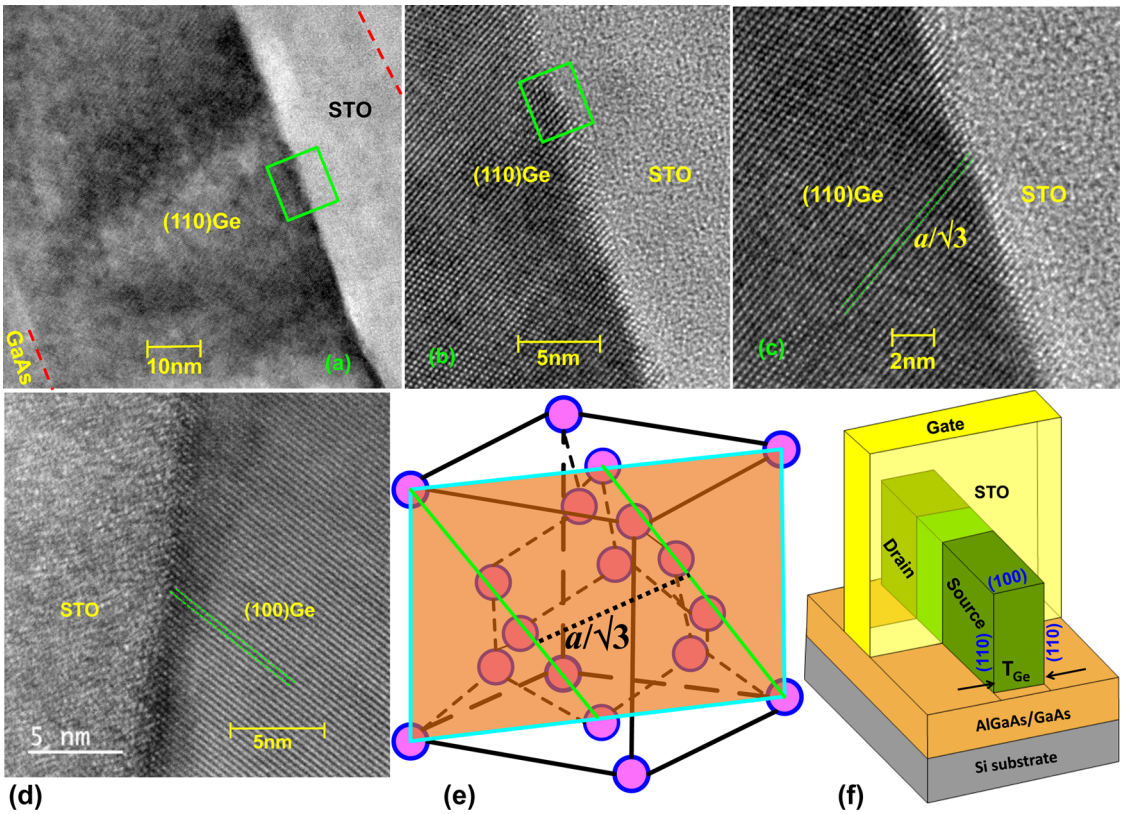

Figure 2. . (a) Cross-sectional TEM micrograph of a $SrTiO_3$ layer deposited on epitaxial (110)Ge grown on (110) GaAs substrate. (b) Uniform thickness of $SrTiO_3$ in a relatively long range. (c) High-resolution TEM micrograph at the $SrTiO_3$/(110)Ge interface. (d) High-resolution TEM micrograph of $SrTiO_3$/(100)Ge interface. (e) Schematic of the (110)Ge surface and (f) Ge-based nanoscale FinFET device with $SrTiO_3$ as a gate dielectric. Sharp heterointerfaces between STO/(110)Ge, $SrTiO_3$/(100)Ge, and Ge/(110)GaAs were demonstrated.

nm thick amorphous STO layer grown on these Ge layers. Moreover, the interface between the amorphous STO and the Ge layer is uniform, which is indispensable in minimizing interface scattering for carrier transport from source to drain in a nanoscale Ge transistor. Figure 2e shows a schematic of the (110)Ge surface and the distance, $(a/\sqrt{3}) = 3.27$ Å, between the two lines indicated in this figure is in agreement with the measured results shown in parts (c) or (d) of Figure 2. In a next-generation nanoscale Ge FinFET transistor structure, shown in Figure 2f, where the (100) and (110)Ge surfaces are the carrier transport planes, a smooth, uniform, and conformal oxide layer on these crystallographically oriented Ge hetero-interfaces is essential. With use of these STO/Ge hetero-interfaces, one can achieve superior transport characteristics in terms of lower interface states, minimal or no frequency dispersion, lower capacitance–voltage hysteresis, and targeted equivalent oxide layer thickness,[8] all essential for ultra-low-power Ge transistors.

Band Gap. The band gap of thin amorphous STO is essential in determining the conduction band offset of STO on crystallographically oriented Ge layers. The band gap of the STO layer has been reported in the literature from 3.2 to 3.91 eV.[15,24,36,37] The absorption coefficient, α, is related to the band gap energy, E_g as $(\alpha h\nu)^2 = A(h\nu - E_g)$, where A is a constant and $h\nu$ is the incident photon energy. Figure 3a shows the experimental $(\alpha h\nu)^2$ versus $h\nu$ Tauc plot for 30 nm amorphous STO layer deposited on a fused silica substrate using pulsed laser ablation (PLD). By extrapolating the linear region at the absorption edge to the x-axis of the graph, a band gap energy of 3.95 eV was determined, which is consistent with results

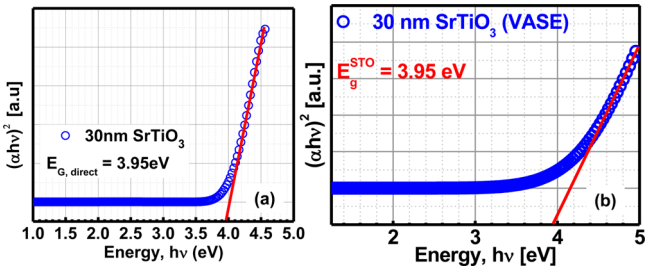

Figure 3. . (a) Experimental absorption coefficient as a function of photon energy near the energy gap of 30 nm $SrTiO_3$ measured by transmission method. (b) Experimental absorption coefficient as a function of photon energy near the energy gap of 30 nm $SrTiO_3$ measured by variable angle spectroscopic ellipsometry. The amorphous $SrTiO_3$ band gap of 3.95 eV was determined from these plots.

reported in the literature.[37] To further confirm the band gap of amorphous STO on epitaxial Ge, variable angle spectroscopic ellipsometry (VASE) was utilized to extract the optical band gap of STO on epitaxial (110)Ge from reflectance measurements of a 30 nm STO thin film. Figure 3b shows the Tauc plot of the absorption coefficient as a function of photon energy extracted from the VASE data fitting. Extrapolation of the linear region at the onset of photon absorption results in a band gap of ~3.95 eV, in excellent agreement with the STO band gap via transmission measurements on silica substrates. It is well-known that amorphous STO is an insulating material with a resistivity of more than 10^3 Ω-cm and an electron mobility of epitaxial STO less than 10 $cm^2/V{\cdot}s$ at room temperature.[27,38] In

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ACS Appl. Mater. Interfaces XXXX, XXX, XXX−XXX

addition, $SrTiO_3$ exhibits high resistivity as it does not have any transitions near room temperature and can therefore act as an effective insulator for Ge-based nanoscale transistors.

Band Offset. The energy band alignment between STO and the crystallographically oriented Ge in STO/Ge heterojunctions is of great importance, as on one hand, a sufficient barrier for electrons and holes is needed to suppress the tunneling leakage current in nanoscale transistors utilizing STO as a gate dielectric, while on the other hand, a lower conduction band offset is essential in achieving lower specific contact resistance. Thus, there is a trade-off between the band offset values and the requirement for having a low contact resistance. Furthermore, the energy band alignment can also provide a possibility for STO to be used as a common gate dielectric for both n- and p-channel Ge nanoscale transistors. The valence band offset, ΔE_V, at each STO/Ge heterojunction was measured using X-ray photoelectron spectroscopy (XPS) and angle integrated photoelectron energy distribution curves for the valence band maximum (VBM). Using these methods, Ge 3d and Sr $3d_{5/2}$ core level (CL) spectra were recorded and the binding energy was corrected by adjusting the carbon 1s CL peak position to 285.0 eV for each sample surface. Figures 4, 5, and 6 show XPS spectra of (i) Sr $3d_{5/2}$ ($E^{Sr}_{Sr3d_{5/2}}$) core level and VBM (E^{Sr}_{VBM}) from a 15 nm thick STO film, (ii) Ge 3d core level (E^{Ge}_{Ge3d}) and VBM (E^{Ge}_{VBM}) each oriented Ge layer, and (iii) Ge 3d core level (E^{Ge}_{Ge3d}) and Sr $3d_{5/2}$ core level ($E^{Sr}_{Sr3d_{5/2}}$) spectra from 1.5 nm STO on (100)Ge, (110)Ge, and (111)Ge interfaces,

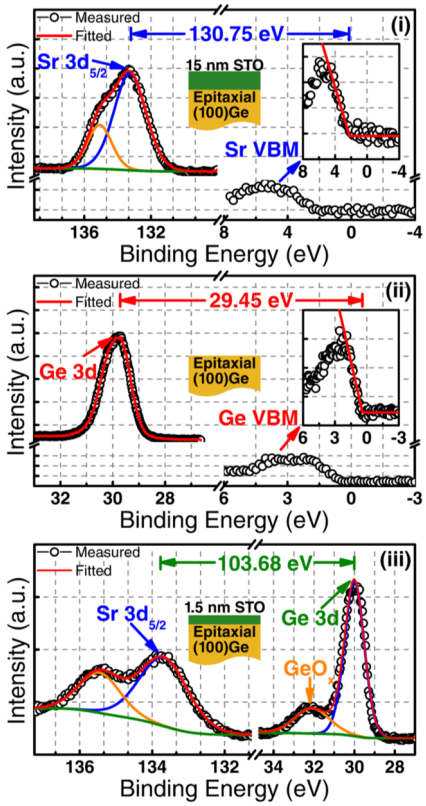

Figure 4. XPS spectra of (i) Sr $3d_{5/2}$ ($E^{Sr}_{Sr3d_{5/2}}$) core level, VBM (E^{Sr}_{VBM}) from 15 nm $SrTiO_3$ film, (ii) Ge 3d core level (E^{Ge}_{Ge3d}) and valence band maximum, VBM (E^{Ge}_{VBM}) of (100)Ge film, and (iii) Sr $3d_{5/2}$ ($E^{Sr}_{Sr3d_{5/2}}$), Ge 3d (E^{Ge}_{Ge3d}) core levels from 1.5 nm $SrTiO_3$ film/(100)Ge interface, respectively.

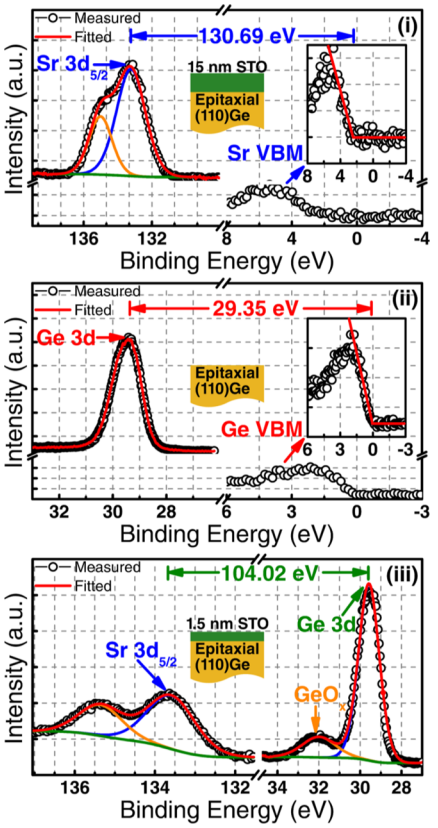

Figure 5. XPS spectra of (i) Sr $3d_{5/2}$ ($E^{Sr}_{Sr3d_{5/2}}$) core level, VBM (E^{Sr}_{VBM}) from 15 nm $SrTiO_3$ film, (ii) Ge 3d core level (E^{Ge}_{Ge3d}) and valence band maximum, VBM (E^{Ge}_{VBM}) of (110)Ge film, and (iii) Sr $3d_{5/2}$ ($E^{Sr}_{Sr3d_{5/2}}$), Ge 3d (E^{Ge}_{Ge3d}) core levels from 1.5 nm $SrTiO_3$ film/(110)Ge interface, respectively.

respectively. Figure 7 shows the corresponding band alignment and histogram of the band offset distribution obtained from STO on crystallographically oriented epitaxial Ge layers, respectively. The ΔE_V for each STO/Ge heterojunction was determined from the following equation[39] using the recorded CL spectra,

$$\Delta E_V = (E^{Ge}_{Ge3d} - E^{Ge}_{VBM})^{Ge} - (E^{Sr}_{Sr3d_{5/2}} - E^{Sr}_{VBM})^{15nmSTO} - (E^{Ge}_{Ge3d} - E^{Sr}_{Sr3d_{5/2}})^{1.5nmSTO/Ge\_interface}$$

Finally, the conduction band offset, ΔE_C, for each STO/Ge heterojunction was determined using the relationship, $\Delta E_C = E^{STO}_g - E^{Ge}_g - \Delta E_V$, where E^{STO}_g and E^{Ge}_g are the band gaps of STO and Ge, respectively. Using the measured data and the equation above, the measured values of ΔE_V for STO on (100)Ge, (110)Ge, and (111)Ge heterointerfaces were 2.38 ± 0.05, 2.67 ± 0.05, and 2.65 ± 0.05 eV, respectively. The calculated ΔE_C for each STO/Ge heterojunction on (100)Ge, (110)Ge, and (111)Ge was 0.9 ± 0.1, 0.61 ± 0.1, and 0.63 ± 0.1 eV, respectively, using the measured 3.95 eV band gap of STO as shown in Figure 3 and 0.67 eV as the band gap of Ge tabulated in Table 1. One can find that the measured ΔE_V is well above 2 eV, required for confining hole carriers inside the p-channel Ge to reduce the leakage current. However, the lower ΔE_C distribution on (100) and (110)Ge can facilitate MIS contact to n-Ge that can lead to lower specific contact resistance. These ΔE_C values would be lowered if one were to select the literature-reported band gap of 3.2 eV for bulk STO;

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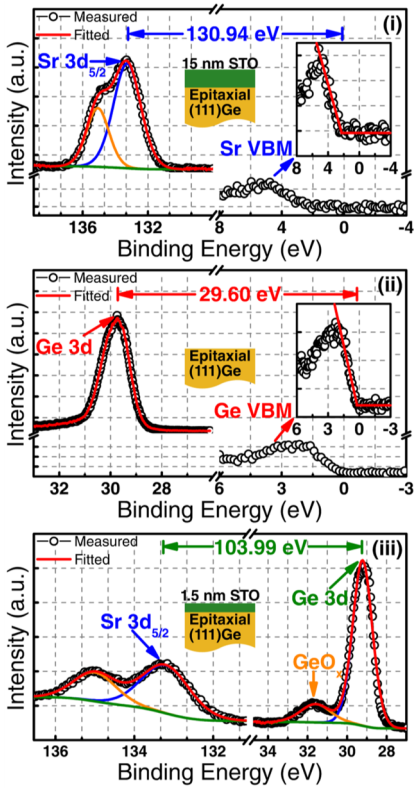

Figure 6. XPS spectra of (i) Sr $3d_{5/2}$ ($E^{Sr}_{Sr3d_{5/2}}$) core level, VBM (E^{Sr}_{VBM}) from 15 nm $SrTiO_3$ film, (ii) Ge 3d core level (E^{Ge}_{Ge3d}) and valence band maximum, VBM (E^{Ge}_{VBM}) of (111)Ge film, and (iii) Sr $3d_{5/2}$ ($E^{Sr}_{Sr3d_{5/2}}$), Ge 3d (E^{Ge}_{Ge3d}) core levels from 1.5 nm $SrTiO_3$ film/(111)Ge interface, respectively.

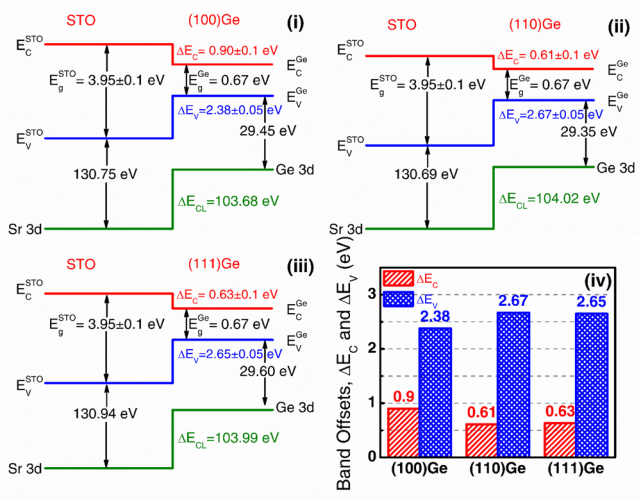

Figure 7. Energy-band alignment of (i) $SrTiO_3$/(100)Ge, (ii) $SrTiO_3$/(110)Ge, (iii) $SrTiO_3$/(111)Ge, and (iv) histogram of band offset distribution obtained from STO on crystallographically oriented epitaxial Ge layers, respectively.

however, the requirement for thin gate dielectric or insulating contact layers forces one to account for the thickness dependency of the STO band gap in the nanoscale regime. The observed difference in ΔE_V values between each STO/Ge heterojunctions can be explained due to the difference in surface reconstruction of the crystallographically oriented Ge epilayers.[40]

Table 1. Band Offset Values of $SrTiO_3$ on Crystallographic Oriented Epitaxial Ge Layers[a]

	(100)	(110)	(111)
ΔE_V (eV)	2.38 ± 0.05	2.67 ± 0.05	2.65 ± 0.05
ΔE_C (eV)	0.9 ± 0.1	0.61 ± 0.1	0.63 ± 0.1

[a]Band gaps of $SrTiO_3$ and Ge are 3.95 and 0.67 eV, respectively, and are considered for determination of conduction band offset.

The determination of the band offset at the semiconductor/semiconductor heterojunction was developed by Kraut et al.[39] using XPS and is widely used to determine ΔE_V at the dielectric and semiconductor heterojunction. However, measures must be taken to compensate the positive changes generated during XPS measurements, especially for oxides.[41,42] Unless these positive charges are neutralized during the XPS measurement by flowing electrons through the sample, there could be positive charge accumulation over the sample surface that potentially affects the band bending due to insufficient compensation of electron loss. In this differential charging effect, the photoelectrons emitted from the semiconductor are compensated by flowing electrons through the sample holder. During our XPS measurements, a continuous flow of electrons was utilized to minimize the binding energy shift caused by the charging effect. Also, the CL and VBM were shifted by the same amount such that the difference between these binding energy values has a less significant effect on the ΔE_V of STO on Ge. Besides, all measured CLs and valence band binding energy values were corrected by shifting C 1s core level peak to 285.0 eV. Thus, the influence of the charging effect on the measured ΔE_V between the STO and the crystallographic oriented Ge is minimized.

The presence of GeO_X would alter the electronic properties of the STO/Ge heterointerface. In the case of PLD deposited STO on epitaxial crystallographic oriented Ge, the GeO_X formation is due to the ambient O_2 atmosphere throughout the deposition process, resulting in the formation of ultrathin, interfacial GeO_X prior to the STO deposition. This creates an ultrathin interlayer that could passivate Ge dangling bonds at the interface and present an increased energy barrier for carriers due to the larger band gap of GeO_X compared with that of STO. Although the presence of GeO_X was detected in the binding energy (BE) spectra of the Ge 3d CL, it is not an indicator of the reduction of STO at the interface by the Ge scavenging of interfacial O^{2-} species. Rather, it is likely that interfacial GeO_X was formed due to the ambient O_2 atmosphere present throughout the PLD STO deposition. To reinforce this conclusion, Figure 8 shows the Ti 2p CL spectra taken from thick (black) and thin (maroon) STO films on (111)Ge. The BE position of the bulk Ti $2p_{3/2}$ peak, 458.40 eV, was found to be in excellent agreement with previously reported Ti $2p_{3/2}$ BE values measured for stoichiometric $SrTiO_3$.[43,44] Moreover, the symmetric nature of the Ti $2p_{3/2}$ peak measured from the thin STO sample indicates that only a single peak fitting is possible, which would not be the case if reduction of Ti species resulted in several Ti^+ states at the interface. The lack of convoluted Ti 2p spectra at the interface therefore suggests that the shift in BE is due *only* to band bending at the interface and not the reduction of $SrTiO_3$ via Ge oxide scavenging. Thus, the band alignment values are from the STO on crystallographically oriented epitaxial Ge.

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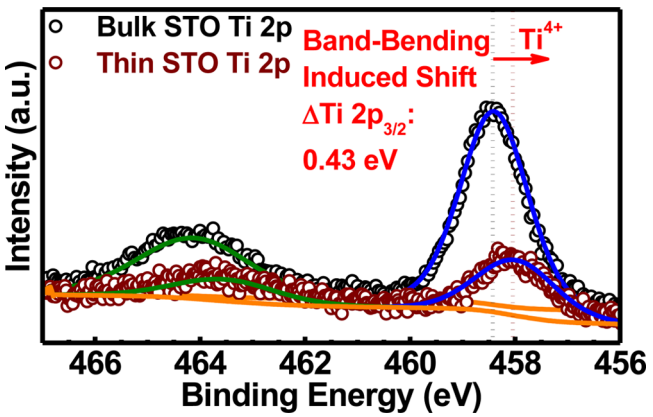

Figure 8. Ti 2p CL spectra as a function of binding energy collected from 15 nm thick and 1.5 nm thin STO films deposited on (111)Ge layers.

MIS Contact. Figure 9a–g shows the schematic of the fabricated MIS diodes on n-Ge, high-resolution TEM micrograph of Ti metal/STO/Ge, current density versus voltage characteristics of MIS contacts to (100) n-Ge (6×10^{16} cm^{-3}) with varying STO thicknesses from 0 to 3 nm, cross-sectional schematic of the fabricated rectangular transfer length measurement (TLM) of Au/Ti/STO/n-Ge/GaAs structures, TEM micrograph of the structure, specific contact resistivity on n+-(100)Ge and (110)Ge (4×10^{18} cm^{-3}) as a function of STO thickness, and specific contact resistivity as a function of sample number evaluated on (100)Ge and (110)Ge, respectively. The current density–voltage (J–V) characteristics of the Au/Ti/3 nm STO/n-Ge MIS contact show a 1000 times increase in current density, indicating a low effective barrier height with ohmic characteristics due to the modulation of the Fermi level by insertion of a thin STO layer. The barrier height drastically decreases with increasing STO thickness, and at a 3 nm STO layer, the J–V characteristics exhibited ohmic behavior with a low effective barrier height due to Fermi level unpinning. The specific contact resistance, ρ_c, obtained from transfer length measurement (TLM) decreases with increasing STO layer thickness and it was found to be lower on the (110)Ge orientation as compared with that on the (100)Ge orientation. The doping concentration of the (100)Ge and (110)Ge layer is about 4×10^{18} cm^{-3}. A ρ_c value of $\sim 1 \times 10^{-3}$ Ω-cm^2 was achieved either on (110)Ge orientations. This specific contact resistance value was higher than it was predicted in ref 35, owing to the Ge doping concentration of 2×10^{19} cm^{-3} used in the simulation as well as the lack of any available conduction band offset data. The cross-sectional TEM micrographs of this Au/Ti/3 nm STO/(110)Ge structure exhibited a uniform and sharp interface, prerequisite for achieving a superior lower contact resistance as well for future nanoscale transistors. In fact, it is well-documented that dielectrics used for MIS contacts are not suitable for use as transistor gate dielectrics since it increases the gate leakage current. To validate this, we have fabricated Al/STO/Ge metal–oxide–semiconductor (MOS) capacitor with and without interfacial layers inserted between the STO and the n-Ge, the results of which are presented in the Supporting Information. It has been concluded that STO can only be used as a MIS contact to the source/drain of n-Ge and is not suitable as a standalone gate dielectric to n-Ge.

CONCLUSIONS

In summary, the pulsed laser deposited perovskite dielectric, $SrTiO_3$, on epitaxial crystallographically oriented Ge opens the opportunity for a new class of nanoscale transistors. Sharp heterointerfaces between amorphous $SrTiO_3$ and the epitaxial (100)Ge or (110)Ge layers as well as between the Ge and the GaAs substrate were achieved. A band gap of 3.95 eV was measured for the amorphous $SrTiO_3$ layers. The valence band offset relation of $\Delta E_V(110) \geq \Delta E_V(111) > \Delta E_V(100)$ and conduction band offset relation of $\Delta E_C(110) \leq \Delta E_C(111) <$

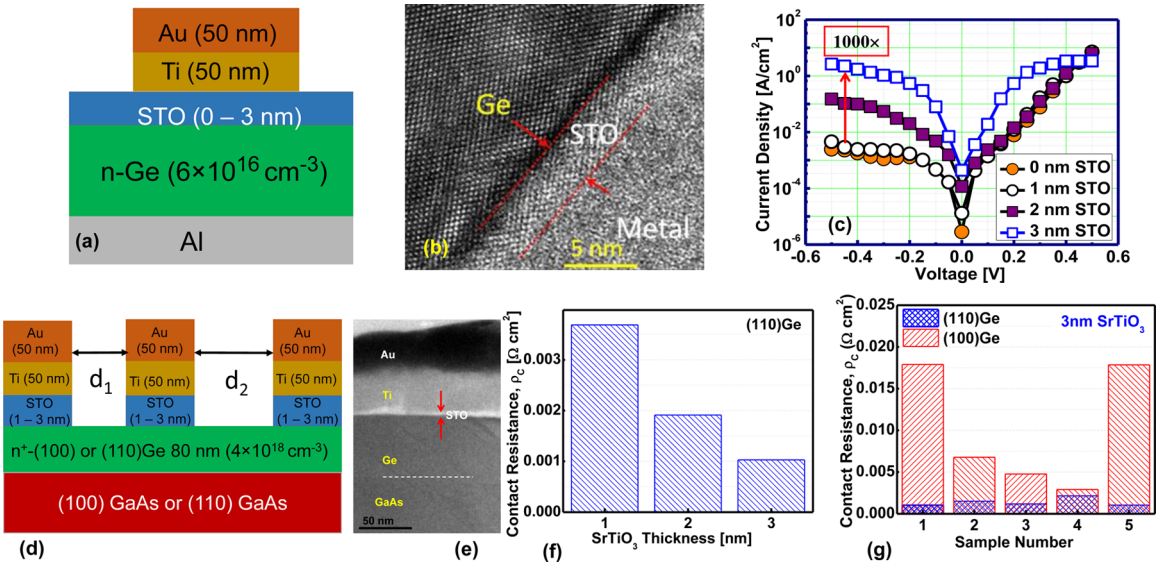

Figure 9. (a) Cross-sectional schematic of the fabricated MIS diodes on Ge, (b) high-resolution cross-sectional TEM micrograph of Ti metal/STO/Ge, (c) current density versus voltage characteristics of MIS contact on bulk n-Ge (6×10^{16} cm^{-3}) as a function of $SrTiO_3$ thicknesses, (d) cross-sectional schematic of the fabricated rectangular TLM of Au/Ti/$SrTiO_3$/n-Ge/GaAs structures, (e) TEM micrograph of the structure in (d), (f) specific contact resistivity on n+-Ge (4×10^{18} cm^{-3}) as a function of $SrTiO_3$ thicknesses on (110)Ge, and (g) specific contact resistivity as a function of sample number tested on (100)Ge and (110)Ge, respectively.

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ACS Appl. Mater. Interfaces XXXX, XXX, XXX–XXX

ΔE_C(100) were demonstrated. A ΔE_V > 2 eVand ΔE_C > 0.5 eV suggests that $SrTiO_3$ could be integrated as part of a composite high-k gate dielectric for Ge nanoscale transistors. The lower ΔE_C at the n-(100)Ge demonstrates an unpinning of the Fermi level with a reduced barrier height enabling a specific contact resistance of 1×10^{-3} Ω-cm^2 on n-type (4×10^{18} cm^{-3}) (110)Ge. It has been reported that the Ge substrate doping has an exponential effect on the specific contact resistance of the MIS contact to n-Ge,[45] while experimental results have strongly differed from the theoretical predictions.[35] Moreover, with increased doping concentration in Ge from ~4×10^{18} cm^{-3} (in this work) to 1×10^{19} cm^{-3}, the specific contact resistance is expected to decrease substantially when using STO as an interlayer for MIS contacts to n-Ge. This is the first experimental study of MIS contacts to n-Ge using STO as an interlayer dielectric. Furthermore, the inclusion of interlayer between STO and n-Ge enables a ~10^8 reduction in leakage current density as compared with the standalone STO gate dielectric. Therefore, the $SrTiO_3$/Ge band offset parameters, role of $SrTiO_3$ as an interlayer for reducing the barrier height and lowering contact resistance, and composite gate dielectric for enhancing the transistor drive current, paves the way for designing Ge-based nanoscale devices.

MATERIALS AND METHODS

Material Synthesis. The undoped epitaxial 80−200 nm thick Ge layers were grown using an in situ growth process on epi-ready polar (100)GaAs, nonpolar (110)GaAs, and polar (111)A GaAs substrates using separate solid source molecular beam epitaxy growth chambers for the Ge and III−V materials, connected via an ultrahigh vacuum transfer chamber. The growth temperature and growth rate of epitaxial Ge were 400 °C and 0.1 Å/s, respectively. The details of the growth procedure are reported elsewhere.[9,10] Epitaxial (100)Ge, (110)Ge, and (111)Ge layers were cleaned using NH_4OH:H_2O_2:H_2O (2:1:1000 volume ratio) for 5 s prior to loading into the PLD chamber for the STO deposition. The queue time was minimized between the cleaning of each Ge layer and STO deposition. The 1.5 and 15 nm STO films were deposited by PLD using a KrF excimer laser (λ = 248 nm) on epitaxial (100)Ge, (110)Ge, and (111)Ge layers in separate runs at a deposition rate of ~0.5 Å/s. A stoichiometric STO target was synthesized by a conventional mixed-oxide processing route and the powder X-ray diffraction from this target is shown in Supporting Information, Figure S1. The focused laser beam irradiates the rotating target at 89 rpm, with a laser energy density of ~2.5 J/cm^2 at a repetition rate of 10 Hz. The STO deposition on each epitaxial crystallographically oriented Ge layer was made using a vacuum chamber with an oxygen pressure of 100 mTorr during the deposition to maintain the stoichiometry of the STO layer. During the STO deposition, the substrate temperature of all Ge films was kept constant at 250 °C.

Materials Characterization. To determine the structural quality and the relaxation state of STO on epitaxial Ge layers, high-resolution triple-axis X-ray rocking curves and reciprocal space maps were recorded. Cross-sectional high-resolution transmission electron microscopy (HR-TEM) was used to characterize the interface between the STO and the Ge epilayer. HR-TEM imaging was performed using an FEI Titan 80-300 transmission electron microscope. For this purpose, the electron transparent foils of thin film cross sections of $SrTiO_3$/(100)Ge/(100)GaAs and $SrTiO_3$/(110)Ge/(110)GaAs were prepared by a standard polishing technique, i.e. mechanical grinding, dimpling, and Ar^+ ion beam milling. The band gap of the $SrTiO_3$ layer was determined by collecting the transmittance data from the 30 nm $SrTiO_3$ layer using ultraviolet−visible−near-infrared spectrometer. Furthermore, the band gap of STO layer on (110)Ge was determined from optical dispersion collected using a J.A. Woollam variable angle spectroscopic ellipsometer. The band alignment of STO on each Ge layer was investigated using a PHI Quantera SXM XPS system with a monochromated Al Kα (energy of 1486.7 eV) X-ray source. The Ge 3d and Sr $3d_{5/2}$ CL binding energy spectra as well as Ge and Sr valence band binding energy spectra were collected with a pass energy of 26 eV and an exit angle of 45°. The binding energy was corrected by adjusting the carbon 1s CL peak position to 285.0 eV for each sample surface. Curve fitting was performed by CasaXPS 2.3.14 using a Lorentzian convolution with a Shirley-type background. The CL energy position was defined to be the center of the peak width at half of the peak height. The VBM values were determined by linear extrapolation of the leading edge to the baseline of the valence band spectra recorded for the 15 nm STO and each crystallographically oriented Ge. The VBM value is sensitive to the choice of points on the leading edge used to obtain the regression line. The uncertainty of ΔE_V and ΔE_C values were found to be in the range of 0.05−0.1 eV by the regression analysis of selected data over the linear region.

The Au/Ti/STO/(100)Ge MIS contacts with varying STO thicknesses from 1 to 3 nm were fabricated using optical photolithography and electron beam evaporation of Au and Ti metals with different contact dimensions. The linear transmission line measurement method on (100)Ge and (110)Ge layers with Au/Ti metals were implemented to measure the specific contact resistance. The detailed fabrication process is discussed in Supporting Information, Figure S2. STO/Ge MOS capacitors with different gate stacks were fabricated using optical photolithography and E-beam evaporation of high-purity Al. The interfacial layer consisting of 0.8 nm GeO_2 (regrowth using oxygen furnace) and 3 nm Al_2O_3 was deposited using atomic layer deposition in a Cambridge NanoTech system using trimethylaluminum as the Al precursor and H_2O as the oxygen source, respectively. The current−voltage characteristics and capacitance−voltage characteristics were measured using a Keithley 4200 SCS, HP4284A, and Cascade Summit 9000 probe station with Cascade DCM200 probe manipulators, shown in Supporting Information, Figure S3.

ASSOCIATED CONTENT

Supporting Information

Details of the $SrTiO_3$ material synthesis and X-ray diffraction spectrum of the STO target, detailed process flow for the fabrication of metal/STO/Ge metal−insulation−semiconductor contacts and optical micrograph of the TLM pattern, and MOS capacitor characteristics of STO/Ge with and without interfacial layer. This material is available free of charge via the Internet at http://pubs.acs.org

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ACS Appl. Mater. Interfaces XXXX, XXX, XXX−XXX

Notes

The authors declare no competing financial interest.

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